Transistor Amplifiers

Input Signal Injection Using Capacitive Coupling

Background:

A resistive voltage divider is often used to bias a transistor amplifier circuit as shown in Figure 1.1. An "ac" input signal is then injected or *superimposed* on the input node of the amplifier by using a *coupling capacitor.*

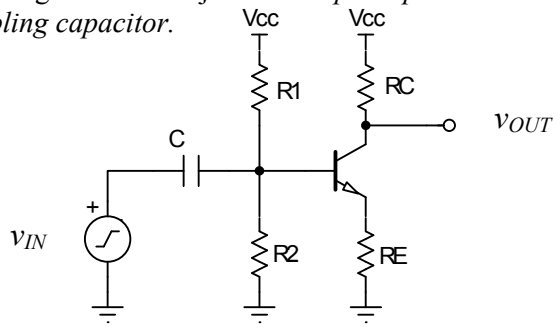

Figure 1.1 - A Typical Voltage Divider Bias Circuit

In order to understand how the input signal is injected, consider the voltage divider portion of the circuit as shown in Figure 1.2. Since there are two independent sources (one DC and one sinusoidal) and since the circuit contains linear elements, *superposition* can be used to separate the DC and "ac" analysis.

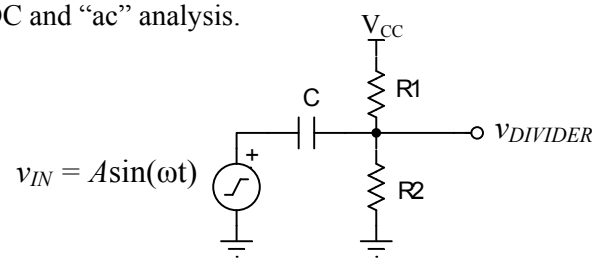

Figure 1.2 - Voltage Divider Circuit

DC Analysis:

At DC, the capacitor can be considered an "open circuit" since its reactance *(1/jωC)* would be infinite for ω=0. Therefore, the DC output voltage of the divider would simply be the voltage division produced by R1 and R2, or:

$$V_{DIVIDER\,(BIAS)} = V_{CC}\left(\frac{R2}{R1+R2}\right) \qquad \text{[Eq. 1.1]}$$

Small-Signal "ac" Analysis:

To determine the circuit response to sinusoidal inputs, V_{CC} can be set equal to zero (an "ac" ground) resulting in the small-signal model of Figure 1.3. (Note the lowercase subscripts for v_{in} and $v_{divider}$ indicating small-signal "ac" quantities.)

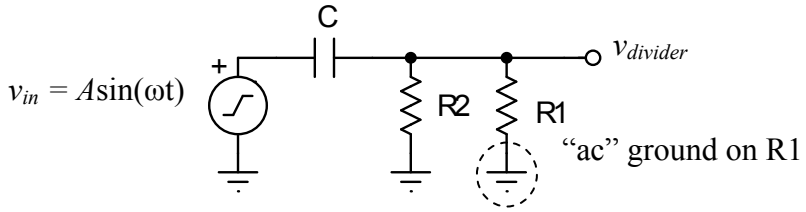

Figure 1.3 - Small-Signal Model

Transistor Amplifiers

Input Signal Injection Using Capacitive Coupling

For sinusoidal inputs, *phasor analysis* can be used to determine the small-signal response of the divider. Essentially the circuit of Figure 1.3 comprises a *First-Order High-Pass Filter* with a transfer function of:

$$H(j\omega) = \frac{1}{1 - j\left(\frac{\omega_0}{\omega}\right)} \qquad \text{[Eq. 1.2]}$$

where ω_0 is the cut-off frequency of the filter given as, $\omega_0 = 1/(R_{eq}C)$ and $Req = R_1||R_2$, the *Thevenin Resistance* of the Divider .

Therefore, for $\omega >> \omega_0$, the magnitude of the high-pass transfer function approaches unity, which means that the entire sinusoidal input signal will appear at the voltage divider node if the frequency is high enough.

Net Output Response:

Thus, the voltage divider provides the DC bias to the circuit and the capacitor couples the sinusoidal "ac" input to the node. The net divider voltage becomes:

$$v_{DIVIDER} \cong \underbrace{V_{CC} \cdot \left(\frac{R_2}{R_1 + R_2}\right)}_{\text{DC Bias}} + \underbrace{A\sin(\omega t)}_{\substack{\text{Superimposed} \\ \text{"ac" Signal}}} \qquad \text{[Eq.1.3]}$$

As long as $\omega >> \omega_0$.

Practical Values:

One practical question is, how low should the cut-off frequency be, in order for the approximation to be valid? The answer lies in considering the magnitude of the transfer function of Eq.1.2. One "rule-of-thumb" is to select a cut-off frequency *(ω_0) one order of magnitude (factor of 10) below the lowest operating frequency (ω_L) expected.* In this case, the magnitude of the transfer function would be:

$$|H(j\omega_L)| = \frac{1}{\sqrt{1 + \left(\frac{\omega_L/10}{\omega_L}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{1}{10}\right)^2}} = \frac{1}{\sqrt{1.01}} = \frac{1}{1.005} = 0.995$$

Where $\omega=\omega_L$ and $\omega_0=\omega_L/10$. As this result shows, more than 99% of the input signal amplitude is coupled to the divider, when the cut-off frequency is less than or equal to 1/10 of ω_L. Other practical ratios yield:

$\omega_0 = \omega_L/n$	$\lvert H(j\omega)\rvert$
1/1	0.707
1/2	0.894
1/4	0.970

$\omega_0 = \omega_L/n$	$\lvert H(j\omega)\rvert$
1/5	0.981
1/8	0.992
1/10	0.995

The trade-off is typically associated with the size of the coupling capacitor selected. Larger capacitors would couple more of the input signal, but would be costly and take up more space. The goal, therefore, is to select the smallest capacitor possible while still meeting design specifications.

One final note, in an actual transistor amplifier, the dynamic input resistance looking into the base of the transistor will appear in parallel with the bottom leg of the voltage divider. This dynamic resistance will reduce the Thevenin Resistance of the divider and require a larger coupling capacitor, to obtain the same low frequency cut-off predicted by this analysis.