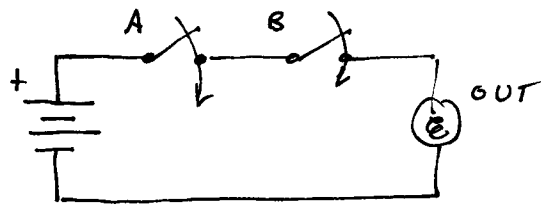
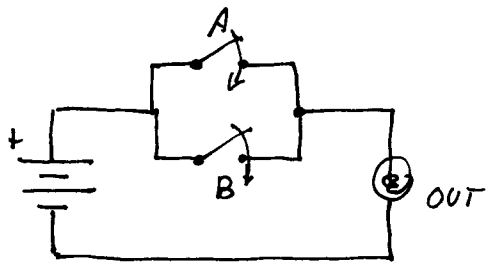
CMOS LOGIC GATES

BASIC LOGIC FUNCTIONS:

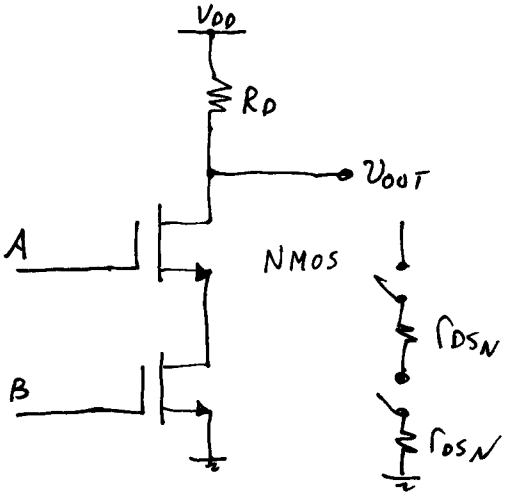


- IF A "AND" B ARE ON, LIGHT IS ON.
- "AND" IMPLIES WIRING SWITCHES IN SERIES!



- IF A "OR" B IS ON, LIGHT IS ON.
- "OR" IMPLIES WIRING SWITCHES IN PARALLEL!

UTILIZING MOSFETS (NMOS)

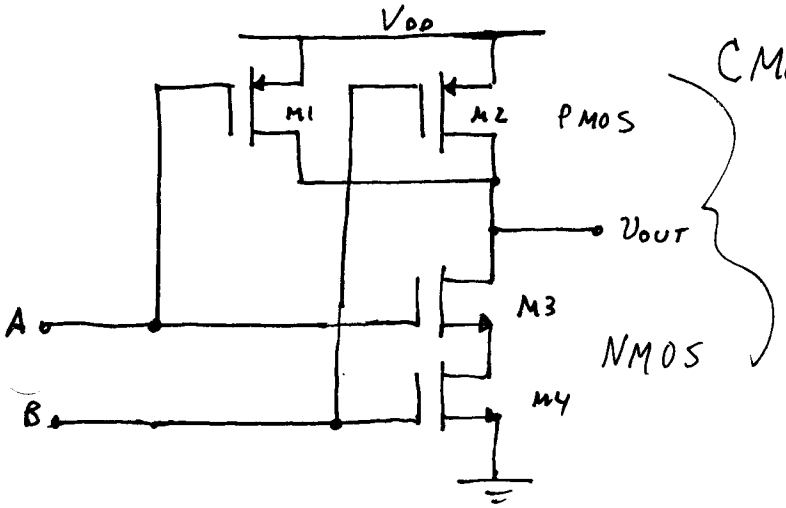


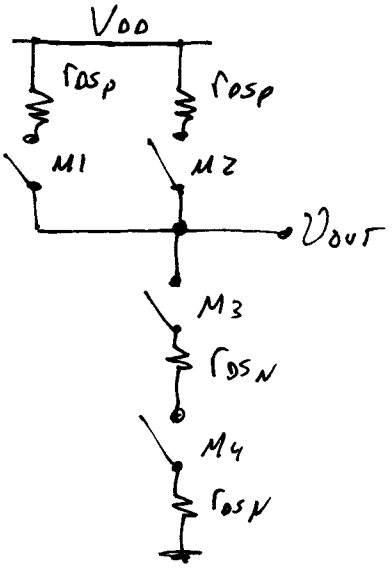
A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

THIS IS NAND!

* COULD ADD AN INVERTER TO REALIZE AND FUNCTION.

Q: CAN WE ELIMINATE THE PULL-UP RESISTOR?

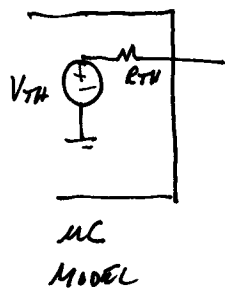




TRUTH TABLE

		PMOS		NMOS			NOTE ↙
A	B	M_1	M_2	M_3	M_4	OUT	R_{OUT}
0	0	ON	ON	OFF	OFF	1	$r_{DS_P} \| \| r_{DS_P}$
0	1	ON	OFF	OFF	ON	1	r_{DSP}
1	0	OFF	ON	ON	OFF	1	r_{DSP}
1	1	OFF	OFF	ON	ON	0	$r_{DS_N} + r_{DS_N}$

OUTPUT RESISTANCE



MC MODEL

Q: FIND R_{TH} ?

LOOSE ENDS :

1) EXPANDABLE (3 INPUT, 4? , 5? ... n?)

2) PROPAGATION DELAYS

3) WHAT IF WE WIRED PMOS IN SERIES & NMOS IN PARALLEL?

NOR

4) 3-INPUT GATES? n-INPUT GATES?