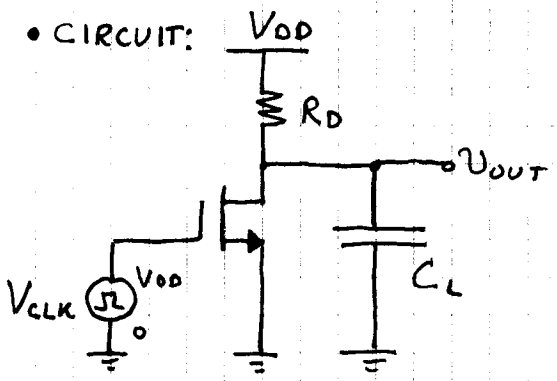
- REVIEW NMOS INVERTER w/ PULL-UP RESISTOR

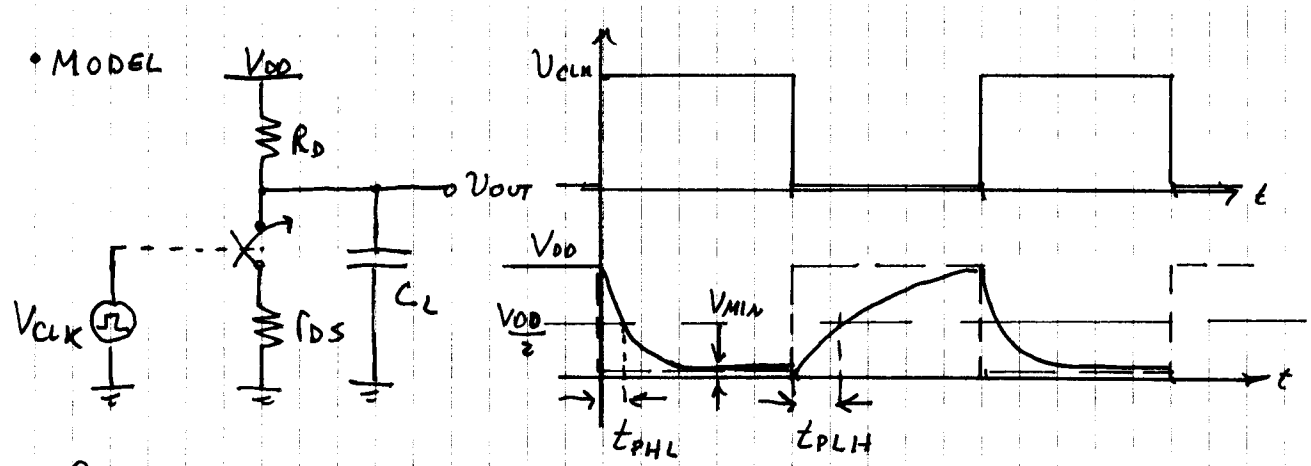
- CIRCUIT:



$$r_{DS} = \frac{1}{K_n'(W/L)(V_{GS} - V_{TH})} \quad \text{(} V_{GS} = V_{DD} \text{)}$$

$$V_{MIN} = V_{DD}\left(\frac{r_{DS}}{r_{DS} + R_D}\right)$$

- MODEL



- PROPAGATION DELAYS

(CHARGING) $t_{PLH} = \tau \ln\left(\frac{2(V_{DD} - V_{MIN})}{V_{DD}}\right) \approx \tau \ln 2$ FOR $V_{MIN} \ll V_{DD}$

$\tau = R_D C_L$

(DISCHARGING) $t_{PHL} = \tau \ln\left(\frac{V_{DD} - V_{MIN}}{V_{DD}/2 - V_{MIN}}\right) \approx \tau \ln 2$ FOR $V_{MIN} \ll V_{DD}$

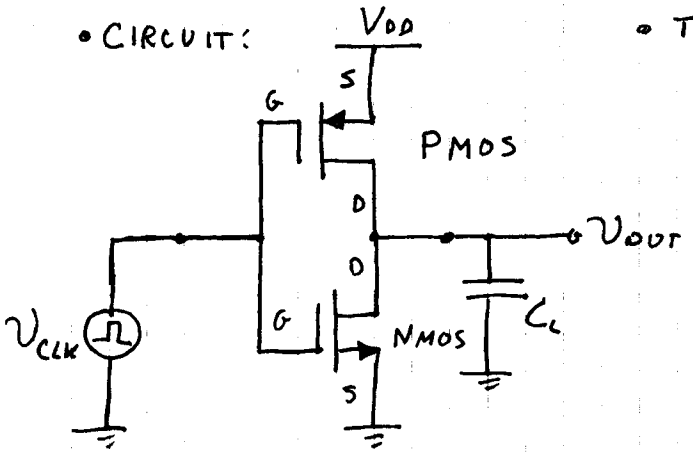
$\tau = (R_D \| r_{DS}) C_L$

- DRAWBACKS

1) ASYMMETRIC WAVEFORMS ($t_{PLH} \gg t_{PHL}$)
2) $V_{MIN} \neq 0$
3) POWER DISSIPATION WHEN OUTPUT IS AT A STATIC 2 ω.

CMOS LOGIC INVERTER

• CIRCUIT:



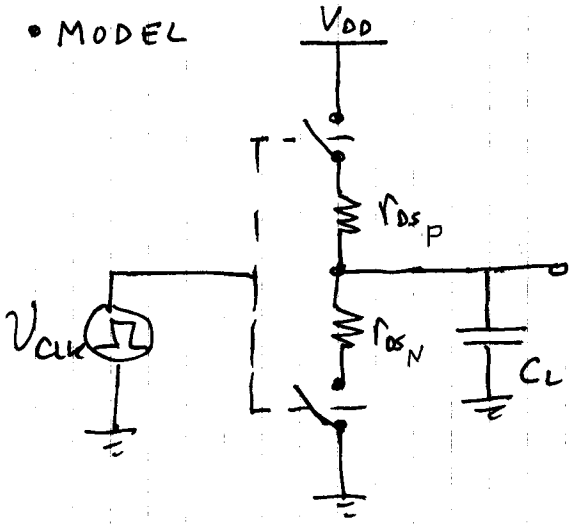
• TURN-ON RESISTANCE

$$r_{DS_P} = \frac{1}{K_P'(W/L)_P (V_{SG} - |V_{TH}|_P)}$$

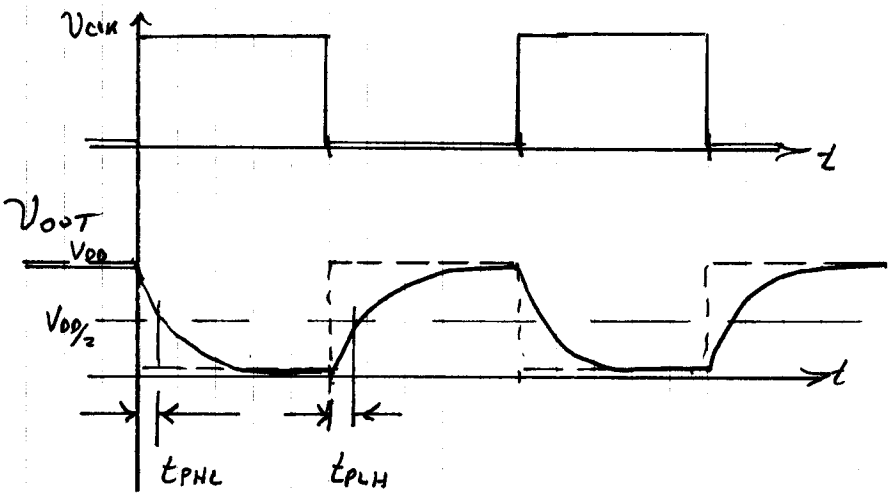
↑ NOTE

$$r_{DS_N} = \frac{1}{K_n'(W/L)_N (V_{GS} - V_{TH_N})}$$

• MODEL



• WAVEFORMS



• PROPAGATION DELAYS:

$$t_{PLH} = \tau \ln 2 = r_{DS_P} C_L \ln 2 \quad \text{(CHARGE)}$$

$$t_{PHL} = \tau \ln 2 = r_{DS_N} C_L \ln 2 \quad \text{(DISCHARGE)}$$

• FEATURES OF CMOS

1) PROPAGATION DELAYS CAN BE MADE EQUAL. ($r_{DS_N} = r_{DS_P}$) ← CAN BE — How?
2) $V_{MIN} = 0$
3) NO POWER DISSIPATION WHEN STATIC (HI OR LO)