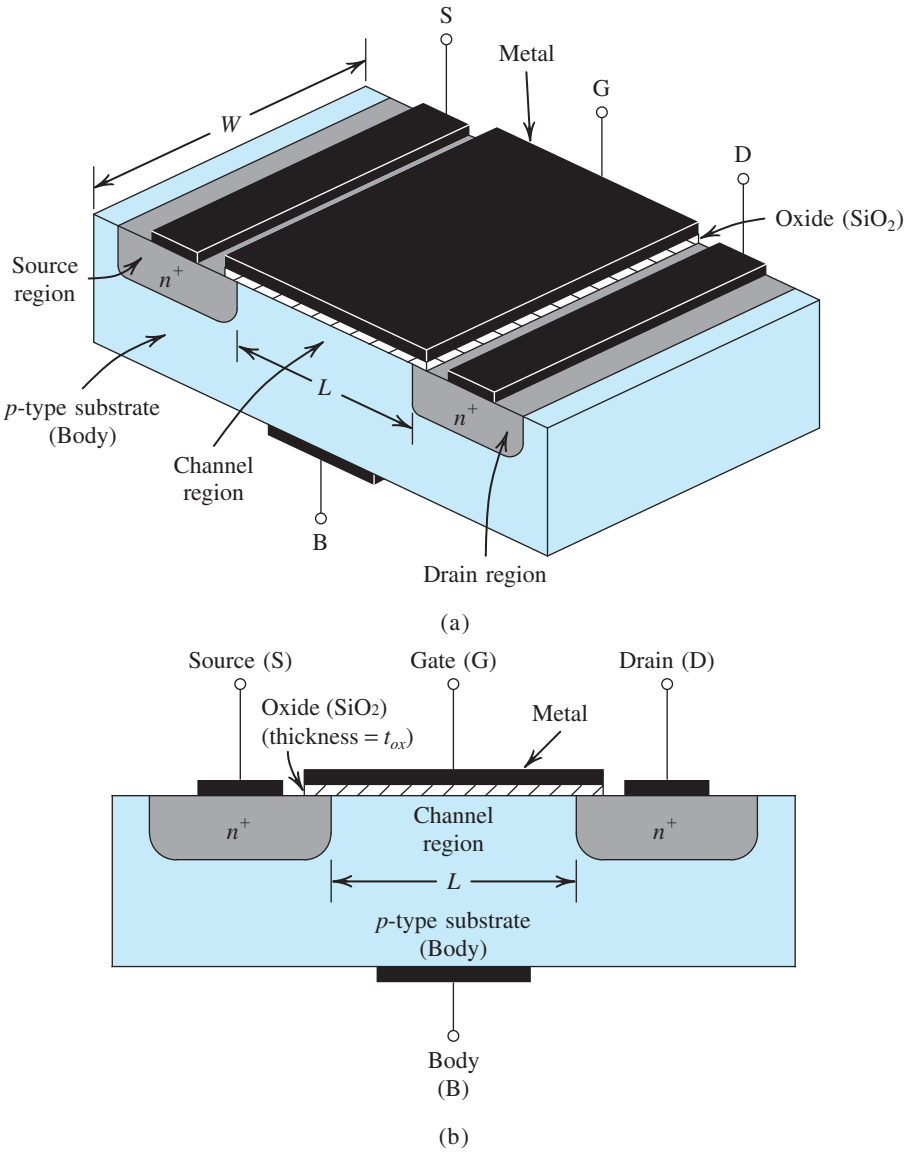

Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically $L = 0.03\ \mu m$ to $1\ \mu m$, $W = 0.05\ \mu m$ to $100\ \mu m$, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.

also made to the source region, the drain region, and the substrate, also known as the **body**.[3] Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

[3] In Fig. 5.1, the contact to the body is shown on the bottom of the device. This will prove helpful in Section 5.4 in explaining a phenomenon known as the "body effect." It is important to note, however, that in actual ICs, contact to the body is made at a location on the top of the device.