ECE 2201 – PRELAB 6

BJT COMMON EMITTER (CE) AMPLIFIER

Hand Analysis

P1. Determine the DC bias for the BJT Common Emitter Amplifier circuit of Figure 6-1 (in this lab) including the voltages V_B, V_C and V_E, as well as the currents I_B, I_C and I_E. Assume that $\beta = 100$.

P2. For the input signal $v_{in} = 0.1\sin(2\pi ft)$ V, where f = 10kHz, determine an expression for the output signal V_{OUT} as a function of time. Plot both v_{IN} and v_{OUT} on the same graph for at least two complete cycles. Be sure to include the DC bias as well as the "ac" signal.

Simulation

P3. Simulate the circuit of Figure 6-1 and provide plots of v_{OUT} and v_{IN} as a function of time for two complete cycles of each waveform and compare to your hand analysis.

P4. Repeat the simulation for the circuit of Figure 6-2 which uses *voltage-divider-bias* so that the input signal can be referenced to ground. Again, provide plots of v_{OUT} and v_{IN} as a function of time for two complete cycles of each waveform.

P5. Simulate the circuit of Figure 6-3 using *ac analysis* and plot the frequency response of the amplifier (ie. gain vs. frequency). Use a logarithmic scale with the gain expressed in decibels (dB) and the frequency in Hz. NOTE: $Gain_{dB} = 20LOG(|V_{OUT}/V_{IN}|)$. Confine the frequency range from 10Hz to 100MHz.

P6. Simulate the circuit of Figure 6-4 and provide a plot of the output signal showing any distortion or clipping.

NOTE: Originally written by Prof. J. McNeill
Modified by S. J. Bitar

ECE 2201 – LAB 6

BJT COMMON EMITTER (CE) AMPLIFIER

PURPOSE:

The purpose of this laboratory assignment is to investigate the BJT Common Emitter (CE) Amplifier. Upon completion of this lab you should be able to:

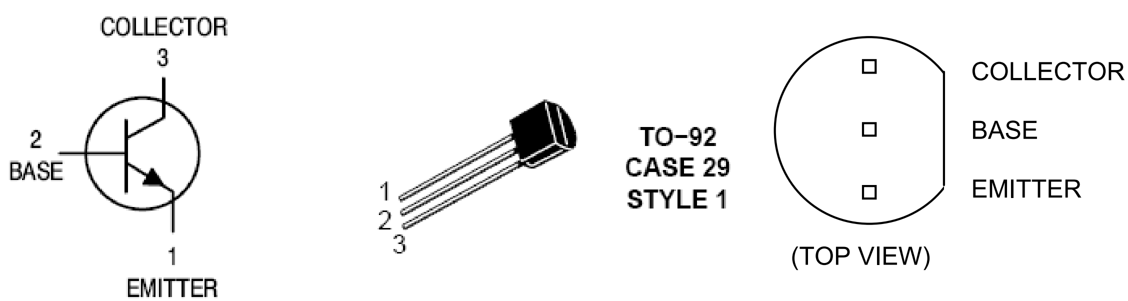
- Determine the biasing of a BJT CE Amplifier.
- Determine the gain of a BJT CE Amplifier with emitter degeneration resistance.
- Use Voltage-Divider-Bias to bias a BJT CE Amplifier.
- Measure the frequency response of a BJT CE Amplifier.
- Dramatically increase the gain of a BJT CE Amplifier using emitter bypass capacitance.

MATERIALS:

- ECE Lab Kit
- DC Power Supply
- DMM
- Function Generator
- Oscilloscope

NOTE: Be sure to record ALL results in your laboratory notebook.

2N3904 BJT terminal designation reminder:



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COMMON EMITTER AMPLIFIER WITH DEGENERATION RESISTANCE R_E

L1. Build the amplifier circuit shown in Fig. 6-1. Note that the supply voltage is +15V (record the actual value to use in calculations).

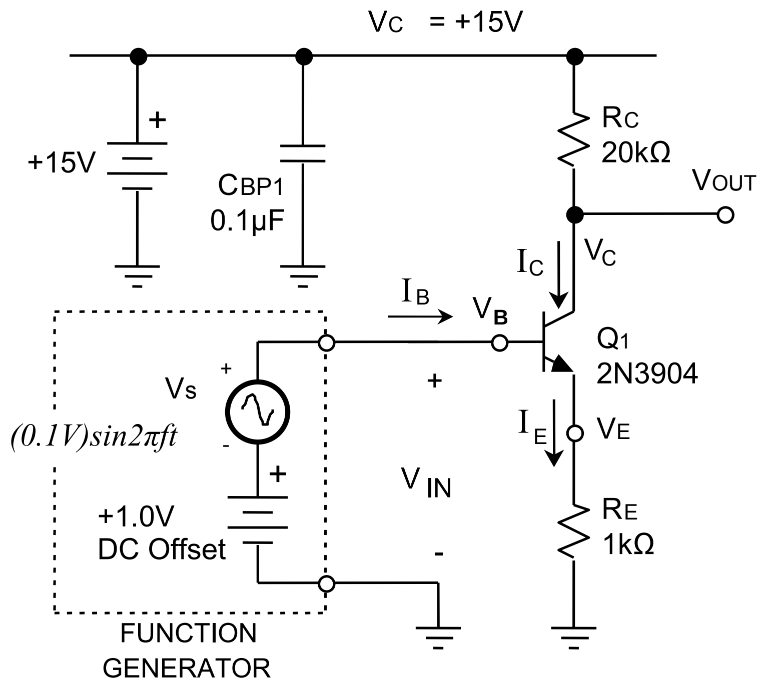

Figure 6-1

FUNCTION GENERATOR SET-UP

L2. Set up the function generator to produce a 0.1V peak, 10kHz sine wave with a 1.0V DC offset (bias). Use the oscilloscope to display v_{IN} on channel 1. Be sure the scope channel is set to DC Coupling so that the DC bias can be displayed.

To set the peak amplitude more accurately, switch to AC Coupling on the scope and "zoom in" to a vertical resolution of 50mV/div. Adjust the function generator for an input signal amplitude of 0.1Vpk (0.2Vpk-pk).

COMMON EMITTER AMPLIFIER OPERATION

L3. Using scope channel 2, measure the output voltage v_{OUT}. Be sure to use DC Coupling so that the DC level can be displayed. Adjust the vertical axis to 2V/DIV and adjust the ground reference level near the bottom of the screen.

If the circuit is working properly, you should see an amplified version of the input signal riding on a DC bias of approximately 8V (7-9V). The output signal should also be INVERTED when compared to the input.

DC BIAS CHECK

L4. Using scope channel 2, measure the average DC level of the output voltage v_{OUT}. Verify this DC measurement using the DMM. Using this DC value, determine the collector bias current I_C. How well does this value compare to your prelab?

SMALL SIGNAL GAIN

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L5. Measure the peak-to-peak amplitudes of both the input and output voltages, $v_{in(p-p)}$ and $v_{out(p-p)}$. For greater accuracy, use AC Coupling and “zoom in” to a finer vertical scale.

NOTE: If there is noise (fuzz) on the input signal, the scope will not be able to display the automatic peak-to-peak measurement accurately. INSTEAD, use voltage cursors to *measure the peak-to-peak amplitude by placing each cursor HALF-WAY BETWEEN the* fuzz at the top and bottom of the signal.

L6. Now, determine the small-signal voltage gain a_v of this amplifier by taking the ratio, $a_v = v_{out(p-p)}/v_{in(p-p)}$. Compare to the theoretically predicted value R_C/R_E.

VOLTAGE DIVIDER BIAS

L7. Modify the previous circuit of Figure 6-1 by eliminating the DC bias provided by the Function Generator (i.e. setting the DC Offset to zero) and adding the *voltage divider* (R_{B1}, R_{B2}) as shown in Figure 6-2. NOTE: Voltage dividers are often used to allow *Single-Supply Operation* when biasing transistor amplifiers.

L8. NEXT, add the 1µF capacitor C_B to *capacitively couple* the input signal to the amplifier. Be sure to observe the POLARITY of the capacitor. NOTE: This capacitor allows the ac input signal to be superimposed on to the base of the transistor without affecting the DC bias.

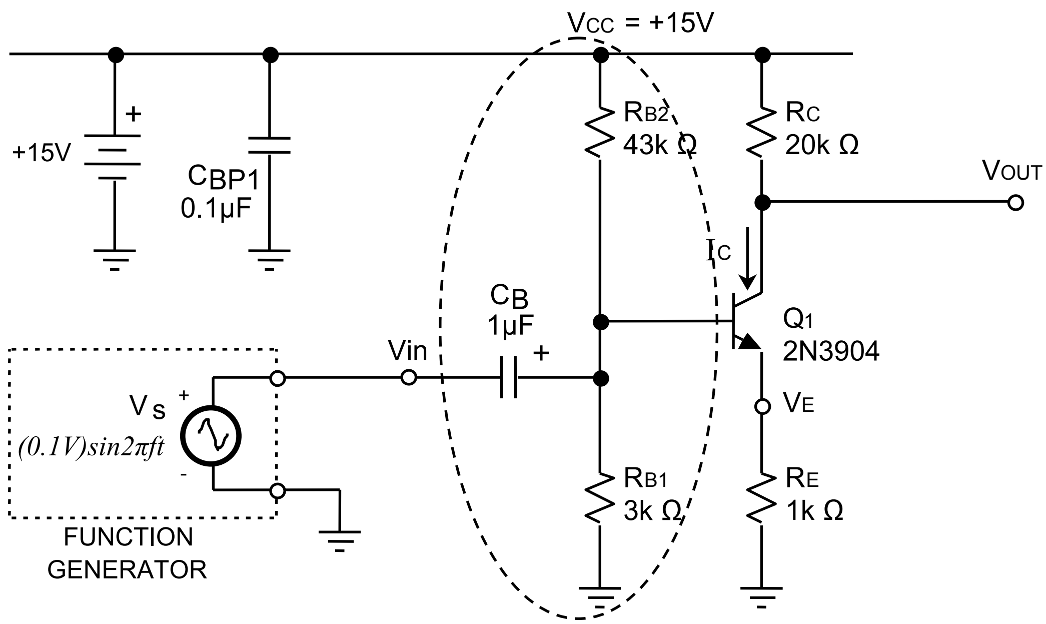

Figure 6-2.

L9. Using the scope or DMM measure the DC voltage at both the base and collector of the transistor and verify that these voltages are similar to the previous circuit of Figure 6-1. How effective is the voltage divider at providing the same bias for the circuit?

L10. Measure the small-signal voltage gain of this amplifier circuit (similar to step L6) and verify that it is the same as the previous circuit of Figure 6-1.

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AMPLIFIER BANDWIDTH LIMITATION

In this part of the lab, you will determine the *bandwidth* of this amplifier (the frequency range before the gain drops to -3dB or $1/\sqrt{2}$ of its maximum value). In addition, you will determine the "roll off" beyond the low and high -3dB cut-off frequencies.

L11. Adjust the function generator to obtain a sine wave amplitude of approximately 100mV peak at v_{in}.

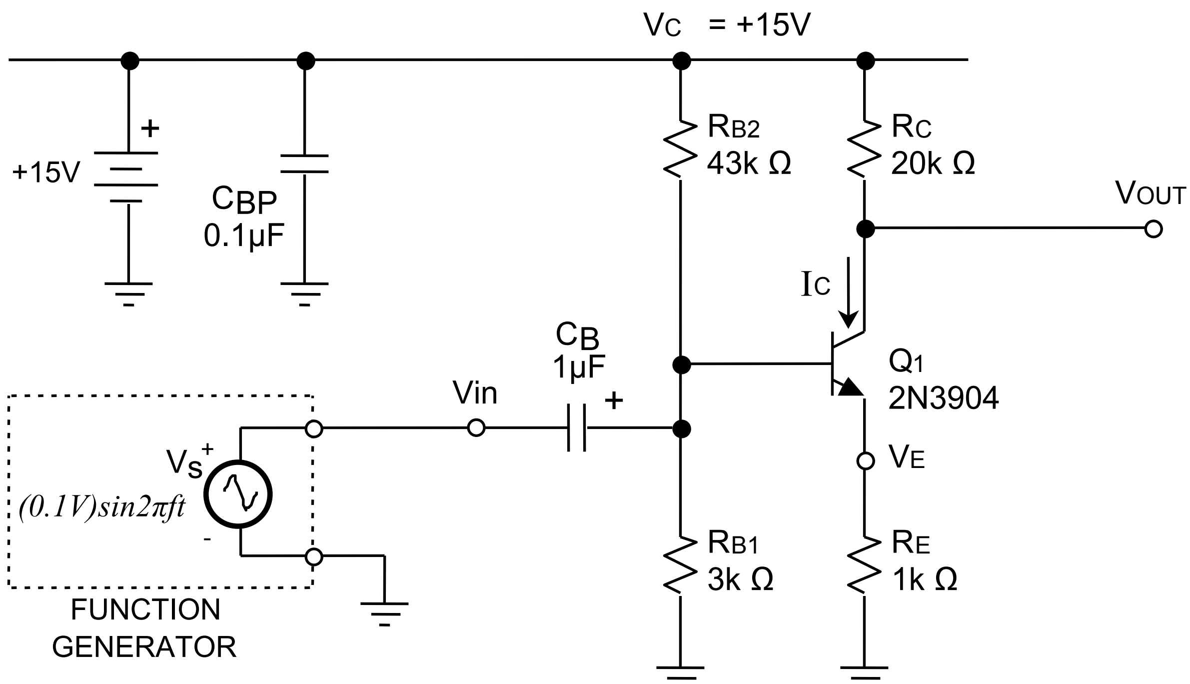

Figure 6-3.

L12. Display v_{IN} on oscilloscope channel 1; set the horizontal time scale to show a few cycles of the sine wave. Use a vertical scale of 50mV per division and adjust the function generator amplitude until the peak level of the signal is ≈ 0.1V (peak-to-peak level of ≈ 200mV). Start with a test frequency of 1kHz.

L13. Display v_{OUT} on oscilloscope channel 2. Use AC coupling and a vertical scale of 0.5V/div and adjust the vertical position so that 0V (ground) is at the center of the screen.

L14. Measure the amplitude of the input and output voltages at the test frequency of 1kHz. Determine the Mid-Band gain $|a_v| = |v_{OUT}|/|v_{IN}|$. Also express the gain in decibels ($Gain_{dB} = 20\ LOG_{10}\ |a_V|$). **NOTE: You should obtain a value of approximately 18 V/V or 25dB.**

L15. Now repeat these measurements for the range of frequencies shown in the following table. At the low end and high end frequencies, you may need to "zoom in" on the output (increase vertical resolution) since the amplitude will decrease dramatically.

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	Nominal Frequency	Actual Frequency (measured)	$\lvert v_{out}\rvert$ (measured)	$\lvert v_{in}\rvert$ (measured) should be ≈ 200mVpk-pk	$\lvert a_v\rvert$ $\lvert v_{out}\rvert / \lvert v_{in}\rvert$ (calculated)	$\lvert a_v\rvert$ [dB]
Low End	10Hz					
	20Hz					
	50Hz					
	100Hz					
	200Hz					
	500Hz					
Mid Band	1kHz					
	10kHz					
	100kHz					
High End	200kHz					
	500kHz					
	1MHz					
	2MHz					
	5MHz					
	10MHz					
	20MHz					

L16. In your lab notebook, plot your measured data on log-log axes, $|a_v|$ in dB vs. LOG_{10} of frequency. Since the frequency and gain vary over a wide range, using a log-log scale will compress the values and present them in a much more informative fashion.

L17. Determine the cut-off frequencies ($f_{-3dB\ LOW}$, and $f_{-3dB\ HIGH}$) where the gain drops by 3dB (ie. to $1/\sqrt{2}$ of its maximum value), as well as the bandwidth ($f_{HIGH} - f_{LOW}$) of the amplifier.

L18. Before proceeding to the next part of the lab, set the input signal back to a 0.1V peak, 10kHz sine wave.

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USING AN EMITTER BYPASS CAPACITOR TO INCREASE GAIN

L19. Add a 100μF capacitor in parallel with R_E as shown in Figure 6-4. Be sure to observe correct polarity! You should see the output waveform amplitude increase significantly, due to the increase in signal gain (WHY?). The output amplitude should exceed the linear range of the amplifier, causing the output "sine wave" to be severely distorted ("clipped"). Measure the maximum and minimum voltage levels at the output, and (in your writeup) identify the transistor operating regions corresponding to each limit.

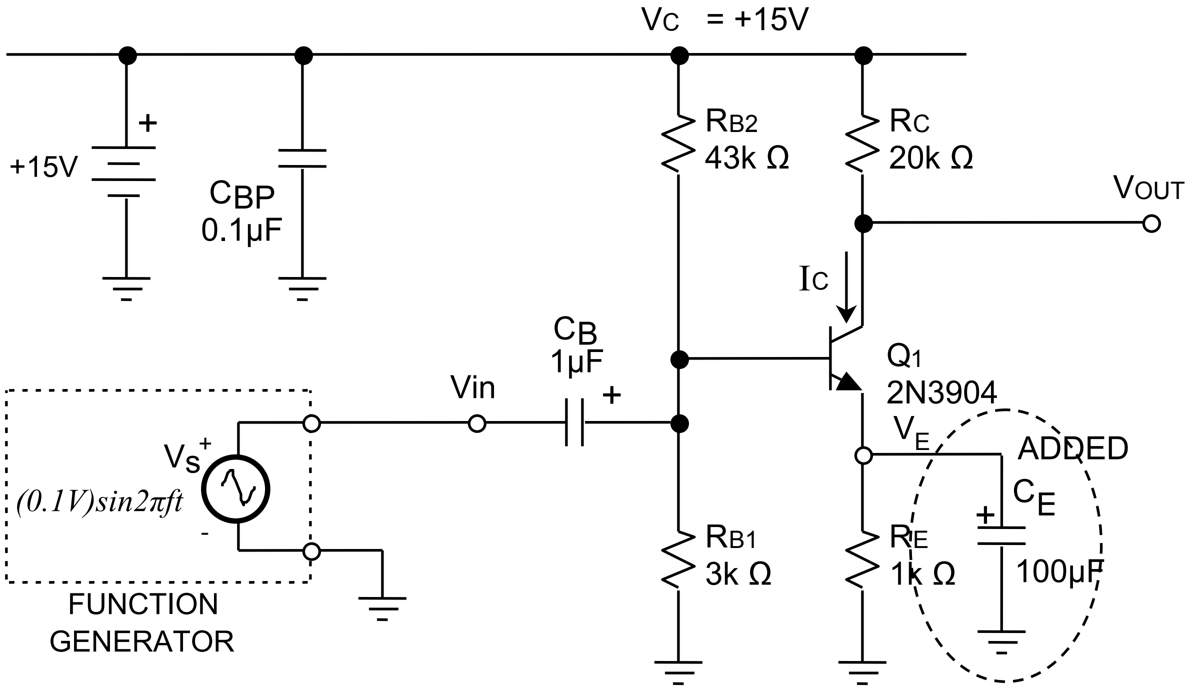

Figure 6-4.

DETERMINE "SMALL SIGNAL" GAIN

L20. Using the function generator, reduce the amplitude of the input signal to $10mV_{PK}$ and determine the new small-signal gain (v_{OUT}/v_{IN}) with the bypass capacitor C_E added. NOTE: Some function generators have a "-20dB feature" which automatically reduces the size of the signal by a factor of 10 which is very convenient for amplifier testing.

NON-LINEAR DISTORTION

L21. Change the input waveform from a sine wave to a triangle wave. This should allow you to see nonlinear distortion more clearly. Increase the input amplitude and note how the nonlinearity (distortion) of the output waveform gets worse as amplitude increases. Even before the severe distortion of clipping, you should see significant nonlinearity for large output waveforms. In your writeup, explain this behavior in light of the small-signal linear approximation.

L22. Increase the input amplitude until the output exceeds the linear range of the amplifier, causing clipping. Measure the maximum and minimum voltage levels at the output, and (in your writeup) identify the transistor operating regions corresponding to each limit.

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LAB WRITEUP

BJT COMMON EMITTER AMPLIFIER

DC BIAS

W1. Compare the simulated, measured and calculated DC Bias values for the BJT Common Emitter Amplifier of Figure 6-1 and explain any similarities or differences. What are your sources of error?

SMALL SIGNAL GAIN

W2. Plot v_{IN} and v_{OUT} (as a function of time) from your oscilloscope observation in lab part L3. Verify the 180° phase shift (inversion of the sine wave) from input to output.

W3. Compare your simulated, measured and calculated small-signal gain values. How do they compare? What are your sources of error?.

W4. Comment on the shape of the output waveform – was it a clean sinusoid, or was there distortion?

VOLTAGE DIVIDER BIAS

W5. Compare the DC Bias and small-signal gain for both amplifier configurations with and without voltage-divider-bias.

FREQUENCY RESPONSE

W6. Plot the frequency response (Bode Plot) of the circuit of Figure 6-3 and compare the actual cut-off frequency to your simulated results.

DRAMATIC GAIN INCREASE WITH USE OF EMITTER BYPASS CAPACITOR

W7. When the 100μF capacitor was added in parallel with R_E (as shown in Figure 6-4, how did circuit operation change? Describe qualitatively and quantitatively.

W8. Plot the output waveform, identifying the measured maximum and minimum voltage clipping levels. Identify the transistor operating regions corresponding to each limit.

NON-LINEAR DISTORTION

W9. Plot a representative waveform showing distortion of the output triangle wave for large waveform amplitudes. Explain this behavior in light of the small-signal linear approximation.

W10. Plot the output waveform, identifying the measured maximum and minimum voltage clipping levels. Identify the transistor operating regions corresponding to each limit.

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