ECE 2201 – PRELAB 4A

MOSFET SWITCHING APPLICATIONS

Digital CMOS Logic Inverter

Hand Analysis

P1. In the circuit of Fig. P4-1, estimate the propagation delays t_{PLH} and t_{PHL} using the resistive switch model for each MOSFET. Assume that $|V_t| = 1.75V$ for both devices, and that the process parameters are as shown.

$$K'_n \frac{W_n}{L_n} = 1.0 \frac{mA}{V^2} \qquad K'_p \frac{W_p}{L_p} = 0.5 \frac{mA}{V^2}$$

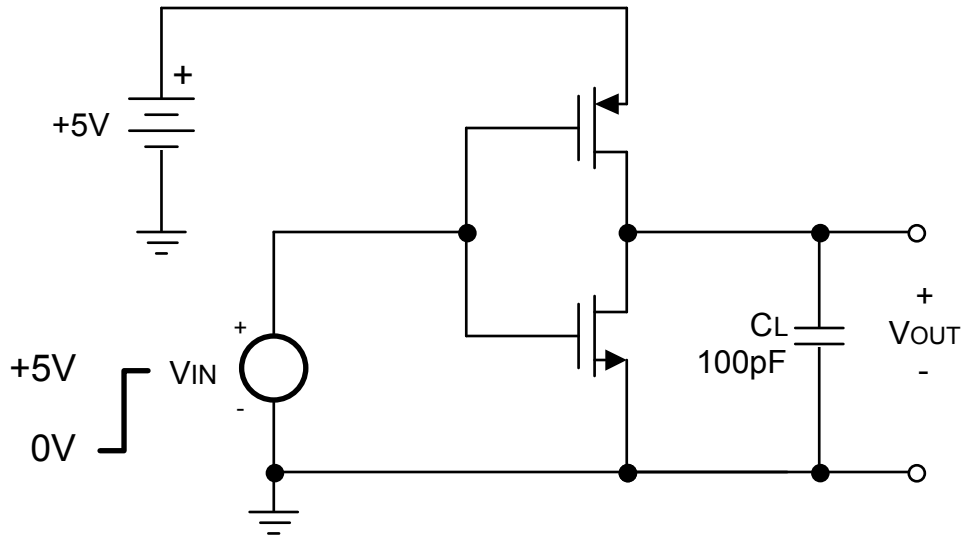


Figure P4-1.

Simulation

P2. Using a simulation tool, determine the propagation delays t_{PLH} and t_{PHL} for this circuit and compare to your hand analysis.

Use the following MOSFET parameters for simulation: $L_n = L_p = 100\mu m$, $W_n = W_p = 100um$, $K'_n = 1mA/V^2$, and $K'_p = 0.5mA/V^2$.

Set V_{IN} to be a 0 to 5V 1MHz clock signal and plot the output as a function of time for at least two clock cycles. Use time cursors on the graph to determine the propagation delays.

ECE 2201 – LAB 4A

MOSFET SWITCHING APPLICATIONS

Digital CMOS Logic Inverter

PURPOSE:

The purpose of this laboratory assignment is to investigate the operation of an integrated CMOS logic inverter utilizing both N-Channel and P-channel enhancement mode MOSFET devices.

Upon completion of this lab you should be able to:

- Recognize the cutoff and triode regions of operation for both N-channel and P-channel MOSFETs.
- Determine the turn-on resistance r_{DS} for several values of gate-to-source voltage V_{GS} for both N and P channel devices.
- Extract MOSFET parameters $k'_n(W_n/L_n)$, $k'_p(W_p/L_p)$ and threshold voltages V_{tn} ,V_{tp} from triode region measurements.
- Apply the P-and N-channel MOSFET in the digital application of a CMOS logic inverter and measure the propagation delays, t_{PHL} and t_{PLH} for high-to-low and low-to-high transitions, respectfully.
- Use the effect of supply voltage on propagation delay to develop a voltage controlled oscillator (VCO).

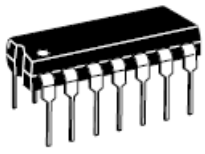
MATERIALS:

- ECE Lab Kit
- DC Power Supply
- DVM
- Function Generator
- Oscilloscope

NOTES:

(1) Be sure to record ALL results in your laboratory notebook.

(2) THIS LAB UTILIZES THE MC14007 (or CD4007) MOSFET ARRAY SHOWN:



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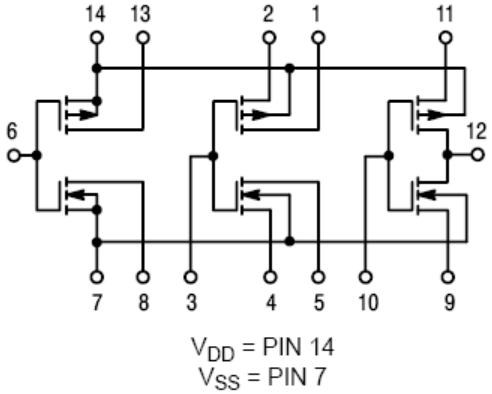

N-CHANNEL ENHANCEMENT MODE MOSFET PARAMETERS

L1. Build the circuit shown in Fig. 4-1, below. This circuit will be used to determine the process parameters $k'_n(W_n/L_n)$ and threshold voltage V_{tn} for one of the N-Channel MOSFETS within the MC14007 MOSFET array.

Note that pins 6, 7 and 8 are used to access one of the NMOS devices within the integrated circuit (IC).

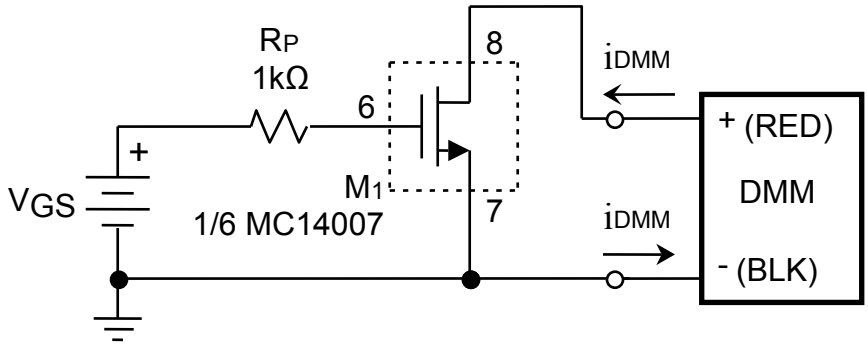

Figure 4-1.

L2. Set V_{GS} to a FIXED 2V and measure the turn-on resistance r_{DSn} using the digital multi-meter (DMM) set to the 20kΩ range.

NOTE: If your meter has an auto-scale feature, disable it and use MANUAL mode. It is important that the meter remains in the 20kΩ range for these measurements, since the internal meter voltage will affect the readings.

L3. Repeat the r_{DSn} measurements for V_{GS} = 3V and 5V.

L4. Using two of your data points and the following expression for r_{DSn} (derived in class), determine values for the process parameter $k'_n(W/L)$ and the threshold voltage V_{tn}.

$$r_{DSn} = \frac{1}{k'_n (W_n / L_n)(v_{GS} - V_{tn})} \qquad (1)$$

NOTE: V_{tn} should be between 1 & 2V and $k'_n(W_n/L_n)$ should be between 0.5 & 1.5 mA/V^2.

P-CHANNEL ENHANCEMENT MODE MOSFET PARAMETERS

L5. Build the circuit shown in Fig. 4-2, below. This circuit will be used to determine the process parameters $k'_p(W_p/L_p)$ and threshold voltage V_{tp} for one of the P-Channel MOSFETS within the MC14007 MOSFET array.

Note that pins 6, 13 and 14 are used to access one of the PMOS devices within the IC.

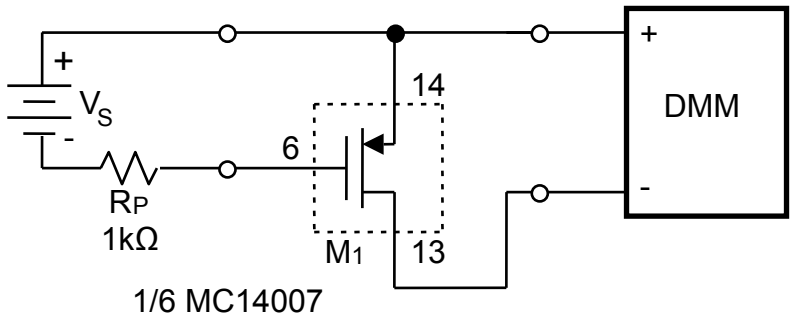

Figure 4-2.

L6. Set V_{SG} to a FIXED 2V and measure the turn-on resistance r_{DS} using the digital multi-meter (DMM) set to the 20kΩ range.

NOTE: Again, if your meter has an auto-scale feature, disable it and use MANUAL mode. It is important that the meter remains in the 20kΩ range for these measurements, since the internal meter voltage will affect the readings.

L7. Repeat the r_{DSp} measurements for V_{SG} = 3V and 5V.

L8. Using two of your data points and the following expression for r_{DSp} (derived in class), determine values for the process parameter $k'_p(W/L)$ and the threshold voltage V_{tp}.

$$r_{DSp} = \frac{1}{k'_p (W_p / L_p)(v_{SG} - |V_{tp}|)} \qquad (2)$$

NOTE: $|V_{tp}|$ should be between 1 & 2V and $k'_p(W_p/L_p)$ should be between 0.5 & 1.5 mA/V^2.

DIGITAL SWITCH APPLICATIONS: CMOS LOGIC INVERTER

L9. The goal of this circuit is the same as the passive load inverter from Lab 3: to take an input voltage of either 0V (logic low) or +5V (logic high) and provide at the output a voltage corresponding to the opposite logic level.

DC Characteristics

L10. Build the CMOS logic inverter shown in Fig. 4-3. Adjust the function generator (using the offset knob) so that v_{IN} is a 100kHz, 0 to +5V square wave.

NOTE: BE SURE TO CHECK V_{IN} ON THE SCOPE BEFORE CONNECTING IT TO THE MOSFET ARRAY.

L11. Set up the oscilloscope to view the gate input v_{IN} on channel 1 at 2V/div, and v_{OUT} on channel 2 at 2V/div. Set both inputs to zero (GND) and adjust the vertical position of each trace so that the input is on the upper half of the display, and the output on the lower half. Once the vertical position is adjusted correctly, when viewing the voltage waveforms, be sure both channels are on DC coupling. Set up the time base of the scope to show at least one full cycle of the square wave.

L12. Sketch the input and output waveforms as shown on the oscilloscope. Measure the high and low voltage levels at the logic output. In particular, note how well the output high and low logic levels reproduce the input levels. How well does this circuit meet the functional goal expressed in part L9?

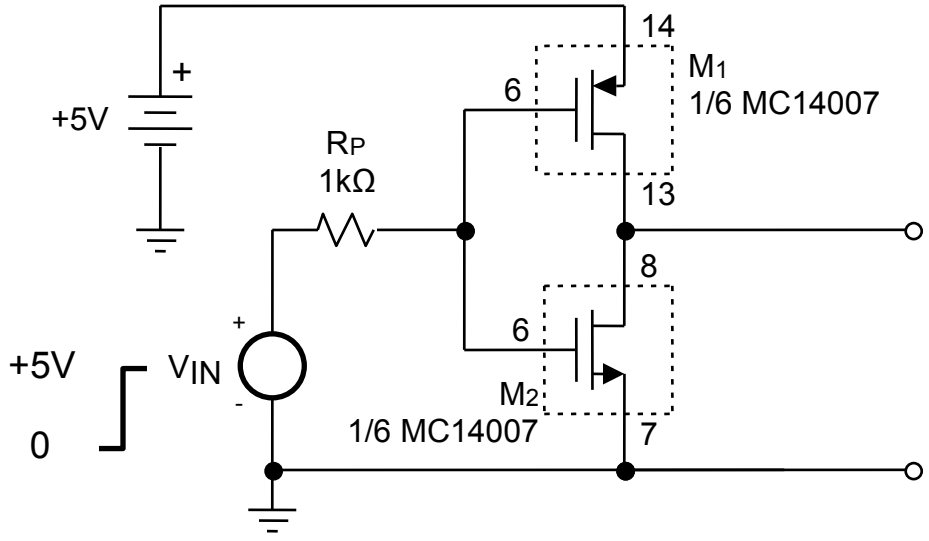

Fig. 4-3

AC Characteristics

L13. As stated in the previous section, the goal of this circuit is provide at the output a logic level corresponding to the opposite of the input. Ideally, if the input changes state, the output would change instantaneously; in practice, there will be a delay which is referred to as the propagation delay.

L14. Add a 100pF load capacitance the logic inverter, as shown in Fig. 4-4. This capacitance corresponds to the capacitive load that the output might "see" due to the capacitance of a PC board trace, bus wiring, or other logic gate inputs.

L15. Sketch the input and output waveforms. Compare to the waveforms from part L10, with no capacitive load.

L16. Measure the high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays. Measurement hint: for the high-to-low measurement, trigger the scope off the rising edge of the input, expand the horizontal scale to get a good look at the delay, and use the time cursors to measure the delay time. For the low-to-high measurement, trigger off the falling edge of the input.

L17. How well does this circuit meet the "instantaneous" functional goal expressed in section L13?

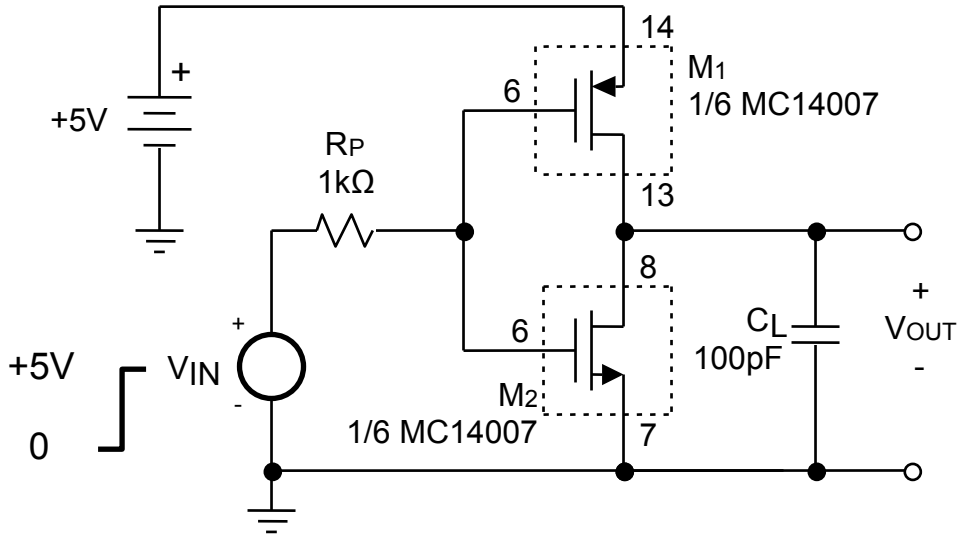

Figure 4-4.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

L18. An important functional block in communication circuits is the voltage controlled oscillator, or VCO. This block is an oscillator for which the output frequency is controlled by a voltage.

One simple type of VCO is the ring oscillator, shown in Fig. 4.5. The ring oscillator is simply a string of inverters connected in a ring. With an odd number of inversions, there is no stable state for v_{OUT}, and the result (after any power-up transients die out) is a single transition "chasing itself" around the ring. Assuming the rising and falling propagation delay times are equal to t_{PD}, the resulting frequency (for an N stage ring) is simply $1/Nt_{PD}$. As we have seen, the propagation delay of the CMOS inverter depends on the supply voltage VDD: a higher VDD increases the gate drive to the MOSFET, reducing r_{DS}, thus reducing the propagation delay. Since the frequency of the ring oscillator is determined by the propagation delay, changing VDD should allow us to change the frequency of the waveform at v_{OUT}.

L19. Build the circuit shown in Fig 4.5.

L20. Measure the frequency of the output waveform at v_{OUT} for VDD=+10V. Measure the frequency at different values of VDD, decreasing in increments of ≈ 1V down to ≈ 3V.

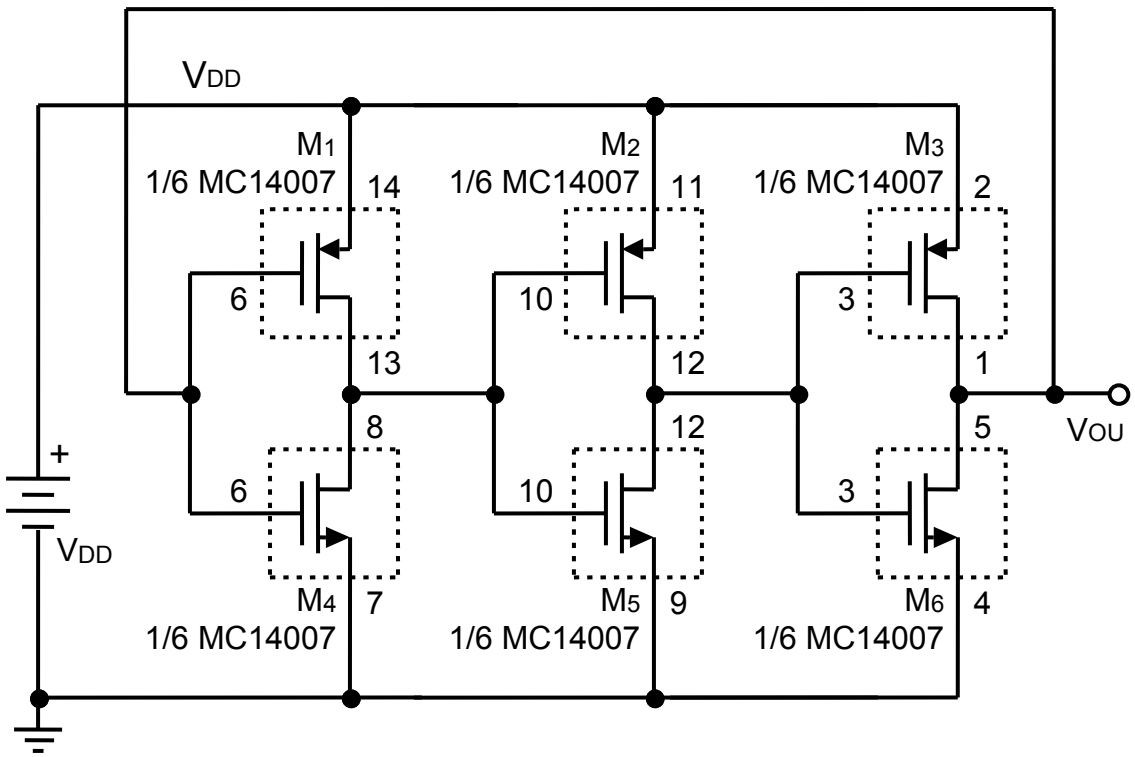

Figure 4-5.

LAB WRITEUP

N-CHANNEL AND P-CHANNEL ENHANCEMENT MODE MOSFET PARAMETERS

W1. Compare the turn-on resistances r_{DSn} & r_{DSp}, as well as the threshold voltages V_{tn} & V_{tp} for the N-channel and P-channel MOSFETS within the MC14007 IC. How do they compare? Which is greater? How balanced are these two devices?

DIGITAL SWITCH APPLICATIONS: CMOS LOGIC INVERTER

W2. Plot the input and output waveforms (without C_L) as shown on the oscilloscope. Indicate the measured high and low voltage levels of the logic output waveform. In particular, note how well the output high and low logic levels reproduce the input levels. How well does this circuit meet the inverter functional goal?

W3. Plot the input and output waveforms with C_L. Compare to the waveforms from part W8, with no capacitive load.

W4. Analysis: Derive equations (in terms of C_L and r_{DS}) predicting the high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays for this logic gate.

W5. Compare the measured high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays to the numerical predictions of your analysis in part W4.

W6. Discussion: How well does this circuit meet the "instantaneous switching" functional goal? Can you suggest any changes in the circuit that would improve delay performance?

W7. Using the process parameters and threshold voltages that you determined in steps L4 and L8 of this lab for the N and P Channel MOSFETS, repeat your prelab simulation using these values and compare your measured propagation delays to that of your simulation. Comment on how well the simulation matches your actual results.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

W8. Plot your frequency measurements of the output waveform at v_{OUT} as a function of the supply voltage VDD. How well does this circuit perform as a VCO in terms of the functional goal expressed in part L18?