ECE 2201
LAB 3 - MOSFET Fundamentals PRELAB

Hand Analysis:

P1. In the circuit of Fig. P3-1, a DMM is used to measured the drain-source resistance r_{DS} as a function of applied gate-source voltage v_{GS}. The following data is obtained:

v_{GS}	r_{DS}
1.0 V	∞
1.5	3180 Ω
2.0	710 Ω
2.7	330 Ω
4.0	180 Ω

Estimate the threshold voltage V_t and $k'_n \frac{W}{L}$ for this MOSFET.

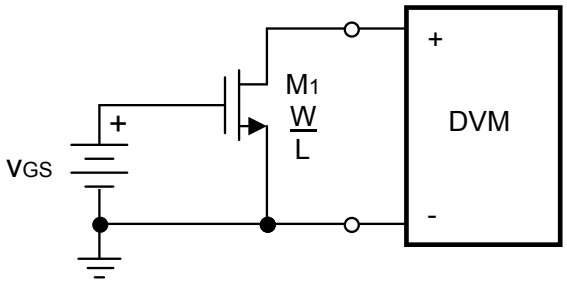


Figure P3-1.

P2. The MOSFET from part P1 is used in the resistive load logic inverter shown in Figure P3-2. Find v_{OUT} for v_{IN}=0V and v_{IN}=+5V.

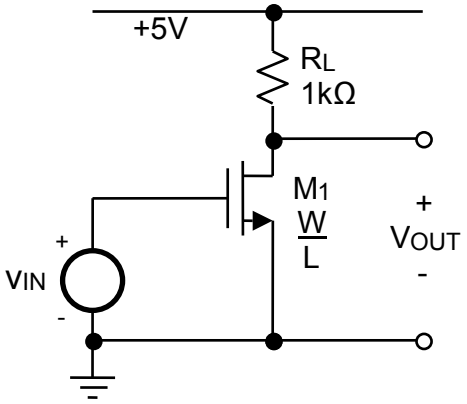


Fig. P3-2

Simulation:

See helpful MOSFET videos at: http://users.wpi.edu/~sjbitar/

P3. Plot the i_{DS} vs. v_{DS} characteristic for both the BS170 and IRF530 MOSFETS. Use the manufacturer models provided.

P4. Now plot the *transconductance* curves, i_{DS} vs. v_{GS} for both MOSFETS, as well.

P5. Duplicate sections L7 to L15, *Digital Switch Applications: Logic Inverter (Passive Load)*, using simulation.

EE2201 - LAB 3

MOSFET Fundamentals and Applications: i_D-v_{DS} Characteristic Digital Switch Applications: Logic Inverter, LED Driver Analog Switch Applications: Automatic Shut-Off Switch

PURPOSE:

The purpose of this laboratory assignment is to investigate the N-channel enhancement mode MOSFET. Upon completion of this lab you should be able to:

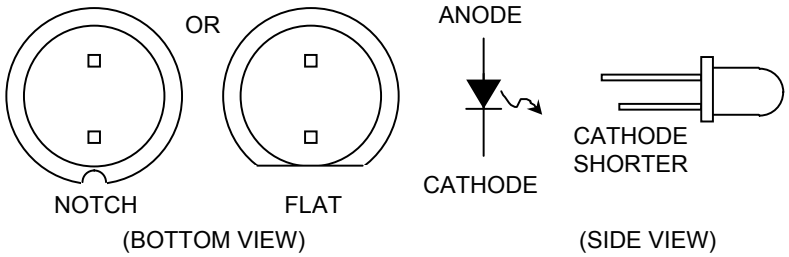
- Recognize the cutoff and triode regions of operation for the MOSFET.
- Characterize the relationship between on resistance r_{DS} and gate drive voltage v_{GS} in the resistive portion of the triode region.
- Extract MOSFET parameters $k'_n \frac{W}{L}$ and threshold voltage V_t from triode region measurements.
- Apply the MOSFET in the digital application of a logic inverter with passive (resistive) load, and measure the propagation delay for high-to-low and low-to-high transition.
- Use the MOSFET to drive a light-emitting diode (LED).
- Recognize the high input impedance of the MOSFET in an automatic shut-off switch application.

MATERIALS:

- ECE Lab Kit / BS170 N-Channel Enhancement Mode MOSFET
- DC Power Supply
- DMM
- Function Generator
- Oscilloscope

NOTE: Be sure to record ALL results in your laboratory notebook.

Light Emitting Diode (LED) terminal designation reminder: Cathode pin on flat (or notched) side:



N-CHANNEL ENHANCEMENT MODE MOSFET: i_D-v_{DS} CHARACTERISTIC

L1. Using the BS170 MOSFET, build the circuit shown in Fig. 3-1. Notice that TWO power supplies are used in this circuit: V_{GS}, set to a FIXED 3V and V_1 which will be varied. The voltage across resistor R_1 will then be used to determine the current i_D in the circuit.

Note: Resistor R_P and capacitor C_P are solely for protection of the high-impedance gate terminal; since $i_G = 0$ under static conditions, there will be no voltage drop across R_{P1} and v_{GS} will be +3V.

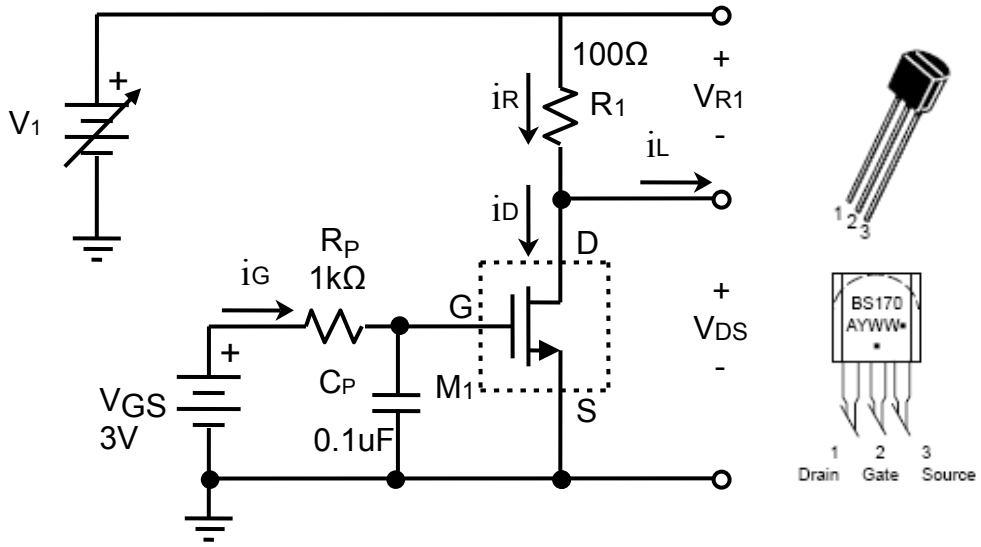


Figure 3-1.

L2. Vary V_1 from 0 to 12 volts in 1V increments and record the drain-to-source voltage V_{DS} at each point. Also measure V_{R1} and calculate the MOSFET drain current i_D at each point using Ohm's Law,

$$i_D = \frac{v_{R1}}{R_1} \qquad (1)$$

Note that Eq. (1) assumes i_L is negligible, so that $i_D \approx i_R$.

L3. Plot the v_{DS}-i_D characteristic (current i_D on the vertical axis, as a function of v_{DS}). Note the saturation and triode operating regions.

IMPROVING ON RESISTANCE r_{DS} BY INCREASING GATE DRIVE v_{GS}

L5. Modify the circuit of Fig. 3-1 as shown in Fig. 3-2, to use the DMM in ohmmeter mode to measure the on resistance r_{DS} directly. As you vary v_{GS}, you will see variation in the on resistance.

NOTES:

(1) Unfortunately, this part requires lots of DMM lead swapping and button clicking – you need to measure the on resistance r_{DS} between the drain and source terminals (DMM as ohmmeter), but also the applied gate-source voltage v_{GS} (DMM as voltmeter). Keep the DMM negative (- or black) lead attached to ground; just swap the positive (+ or red) lead. Since the currents flowing in this circuit are relatively small, you don't need to turn power off when changing the lead configuration - save time in the lab!

(2) It's important to observe the DMM lead polarity shown in Fig. 3-2. If the DMM connection is reversed, the DMM current i_{DMM} will forward bias the substrate-to-drain diode when $V_{GS} < V_t$.

(3) The turn-on resistance of the BS170 can be as low as 5Ω. Therefore, choose a low resistance range for the DMM that measures the resistance to at least 3 significant figures. If using a meter with an "autoscale" feature, switch the meter to MANUAL mode, so it does not automatically change ranges. If possible, stay in one range for consistency.

L6. Starting with $v_{GS} \approx +5V$, measure r_{DS} and v_{GS}. The resistance r_{DS} should be less than 10Ω. Reduce v_{GS} in steps of about 0.5V, measuring r_{DS} and v_{GS} at each step. As v_{GS} decreases, you should see r_{DS} increase. As v_{GS} gets closer to the threshold voltage V_t, r_{DS} will start increasing rapidly. Take a few data points with r_{DS} about 20Ω, 50Ω, 100Ω, 200Ω, 500Ω. You should end up with about 10 data points. Plot r_{DS} as a function of v_{GS} .

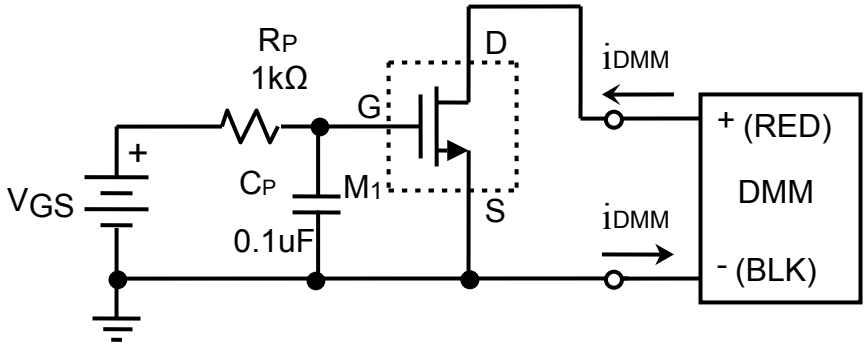


Figure 3-2.

DIGITAL SWITCH APPLICATIONS: LOGIC INVERTER (PASSIVE LOAD)

L7. The goal of this circuit is to take an input voltage of either 0V (logic low) or +5V (logic high) and provide at the output a voltage corresponding to the opposite logic level.

DC Characteristics

L8. Build the logic inverter shown in Fig. 3-3. Adjust the function generator (using the offset knob) so that v_{IN} is a 100kHz, 0 to +5V square wave. Note that C_P has been removed.

L9. Set up the oscilloscope to view the gate input v_{IN} on channel 1 at 2V/div, and v_{OUT} on channel 2 at 2V/div. Set both inputs to zero (GND) and adjust the vertical position of each trace so that the input is on the upper half of the display, and the output on the lower half. Once the vertical position is adjusted correctly, when viewing the voltage waveforms, be sure both channels are on DC coupling. Set up the time base of the scope to show at least one full cycle of the square wave.

L10. Sketch the input and output waveforms as shown on the oscilloscope. Measure the high and low voltage levels at the logic output. In particular, note how well the output high and low logic levels reproduce the input levels. How well does this circuit meet the functional goal expressed in part L7?

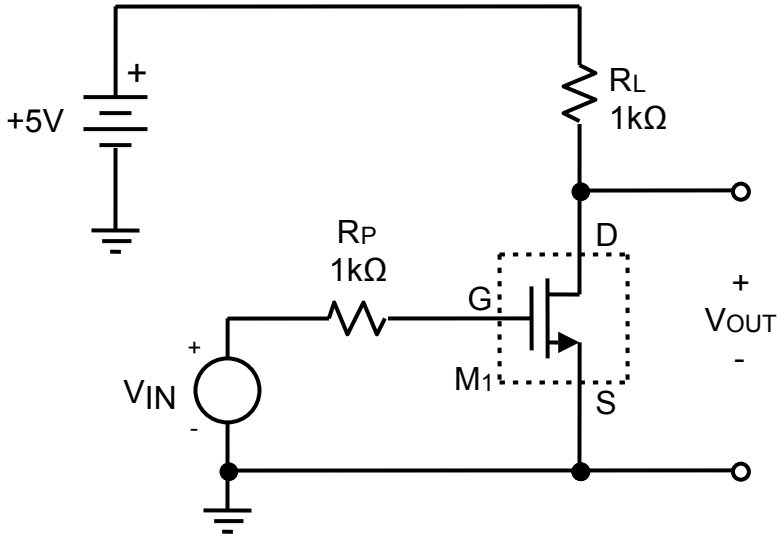


Fig. 3-3

AC Characteristics

L11. As stated in the previous section, the goal of this circuit is provide at the output a logic level corresponding to the opposite of the input. Ideally, if the input changes state, the output would change instantaneously; in practice, there will be a delay which is referred to as the propagation delay.

L12. Add a 100pF load capacitance at the output of the logic inverter, as shown in Fig. 3-4. This capacitance corresponds to the load that the output might "see" due to the capacitance of a PC board trace, cable, bus wiring, or other logic gate inputs.

L13. Sketch the input and output waveforms. Compare to the waveforms from part L10, with no capacitive load.

L14. Measure the high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays as defined in Figure 3-5. Note that the waveforms in Fig. 3-5 are only for definition of the t_{PHL} and t_{PLH} quantities; your waveform shapes will probably be different!

Measurement hint: for the high-to-low measurement, trigger the scope off the rising edge of the input, expand the horizontal scale to get a good look at the delay (shifting horizontal position if necessary), and use the time cursors to measure the delay time. For the low-to-high measurement, trigger off the falling edge of the input. Set both channels to a scale of 1V/div, and adjust the channel position so that ground is 2.5 divisions below the center of the display. Then the center of the display will correspond to the 2.5V logic threshold used in the definition of t_{PHL} and t_{PLH}.

L15. How well does this circuit meet the "instantaneous" functional goal expressed in section L11?

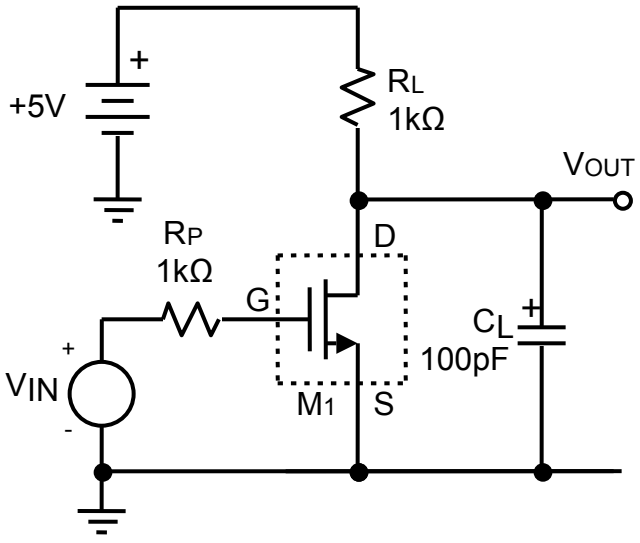


Figure 3-4.

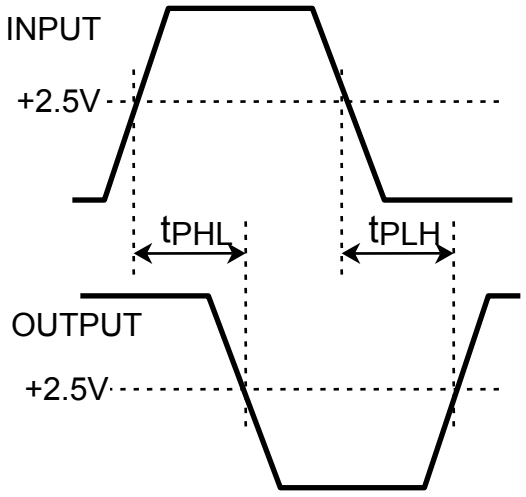


Figure 3-5

LIGHT EMITTING DIODE (LED) DRIVER

Application

L16. The LED emits light when forward biased. Depending on the specific LED (color, efficiency, etc.) the required current is approximately 5 to 10 mA for reasonable light output; the accompanying forward bias voltage is about 2V for the red LED in your lab kit.

L17. The circuit of Figure 3-6 shows an attempt to drive an LED from a voltage source with a high output resistance R_S=100kΩ. It is desired that the LED current be at least 5mA for adequate illumination.

L18. Analysis: assuming a constant-voltage-drop model of +2V for the LED in the forward bias region, find the resulting LED current i_{LED} when v_{IN} = +5V. How does this value compare with the desired current from part L17?

L19. One solution is to use the MOSFET as a switch to drive the LED, as shown in Figure 3-7. Since the MOSFET gate current is zero, there is no voltage drop across the high source resistance R_S.

L20. Design: Using your data from part L6 for r_{DS} with a +5V gate drive at v_{GS}, determine the resistance R_2 required so that the total resistance (R_2 + r_{DS}) gives a 5mA LED current.

L21. Build the circuit of Figure 3-7, with a red LED and your design value for R_2 from part L20 (use the closest standard value available in your ECE lab kit). Set v_{IN} to be a 0 to +5V square wave at a frequency of 1Hz (one cycle per second). You should see the LED blinking, with good illumination during the "on" half of the cycle.

L22. Increase the frequency of the square wave until the frequency is high enough that you can no longer notice the on/off blinking. Note the frequency above which your eye isn't fast enough to follow changes in illumination. Years of research have allowed manufacturers of computer monitors to determine this critical frequency precisely, allowing them to set industry standard screen refresh rates slightly lower, resulting in barely noticeable (but subtly annoying) flicker.

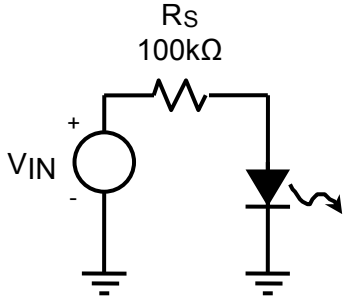


Figure 3-6

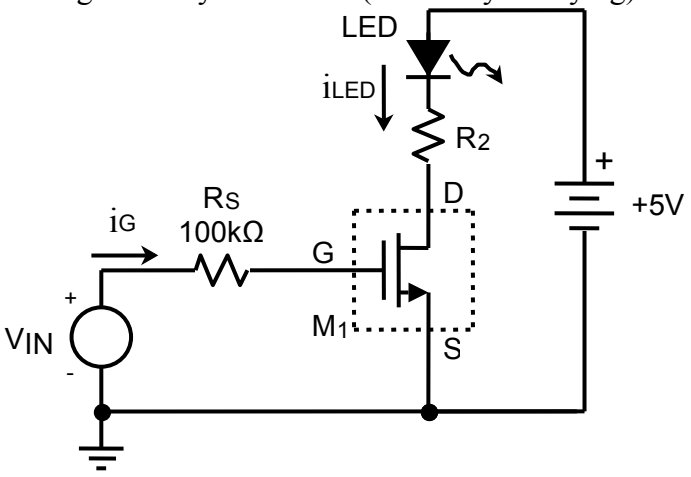


Figure 3-7

AUTOMATIC SHUTOFF SWITCH

L23. One of our professors once bought a toy flashlight that became one of his son's favorite toys. When the boy got it for his birthday, his father realized, "Oh no! We'll be buying batteries for this thing every week. He'll never remember to turn it off, and the batteries will be dying all the time!!!" (This increasingly negative attitude seems to be a part of normal parental aging).

However, his father was surprised and pleased to discover that this flashlight had an automatic shutoff feature: to turn it on, you pushed a button; after a few seconds, the light started to fade and then turned off. If you wanted the light to stay on, you just pressed the button again. Figure 3-8, below, is one circuit that can perform this operation.

L24. Modify your previous LED drive circuit and build the automatic shutoff circuit shown in Figure 3-8 below. The normally open (N.O.) momentary contact (pushbutton) switch can be simulated using a length of wire that you momentarily connect to the +5V rail.

L25. When the "pushbutton" switch is closed, the LED should go on. When the "pushbutton" switch is opened, the LED should go out after a delay of a few seconds. If you have a stopwatch or timer function available, record the delay time until the light goes out.

If capacitor C_T is increased (add another 0.01µF in parallel, or try 0.1µF), does the delay until LED shutoff increase or decrease?

L26. Explain (qualitatively) how this circuit works. Hint: this is one case in which we can't assume the reverse bias current of the 1N4148 to be negligible! (Major hint: In the reverse bias region, we can model the 1N4148 as a current source with a value of order 10nA; check your Lab 1 results for the reverse bias current value you measured).

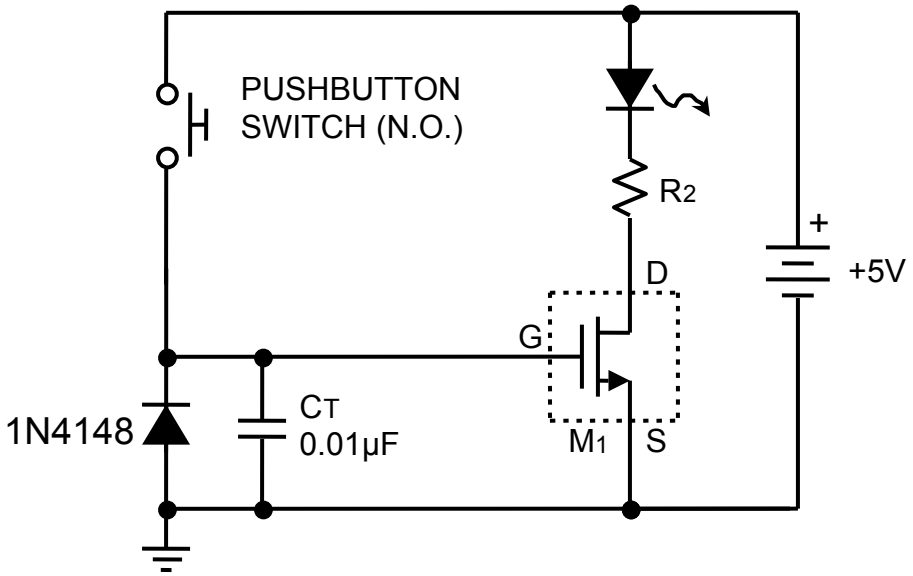


Figure 3-8.

LAB WRITEUP

N-CHANNEL ENHANCEMENT MODE MOSFET: i_D-v_{DS} CHARACTERISTIC

W1. Plot the v_{DS}-i_D characteristic (current i_D on the vertical axis, as a function of v_{DS}). Note the saturation and triode operating regions.

W2. Determine the slope of the v_{DS}-i_D characteristic near the origin (the resistive part of the triode operating region). From the slope, determine the value of r_{DS} as $\Delta v_{DS}/\Delta i_D$.

IMPROVING ON RESISTANCE r_{DS} BY INCREASING GATE DRIVE v_{GS}

W3. Plot r_{DS} as a function of v_{GS}. Compare your measured r_{DS} resistance at v_{GS} = +3V to the value obtained from the slope of the v_{DS}-i_D plot in part W2.

W4. Plot $1/r_{DS}$ as a function of v_{GS}. Using this plot, extract the MOSFET model parameters $k'_n \frac{W}{L}$ and threshold voltage V_t for the triode region "on" resistance expression:

$$r_{DS} = \frac{1}{k'_n \frac{W}{L}(v_{GS} - V_t)} \qquad (2)$$

W5. Using your parameters from W4, plot the prediction of the MOSFET r_{DS} model on the same axes with your measured data from parts W3 and W4. How well does the model predict the measured data?

DIGITAL SWITCH APPLICATIONS: LOGIC INVERTER (PASSIVE LOAD)

W6. Plot the input and output waveforms (without C_L) as shown on the oscilloscope. Indicate the measured high and low voltage levels of the logic output waveform. In particular, note how well the output high and low logic levels reproduce the input levels. How well does this circuit meet the functional goal expressed in part L7?

W7. Plot the input and output waveforms with C_L. Compare to the waveforms from part W6, with no capacitive load.

W8. Explain qualitatively any difference in circuit behavior with C_L when processing rising vs. falling edges (e.g. unequal propagation delays).

W9. Analysis: Derive equations (in terms of R_L, C_L, and r_{DS}) predicting the high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays (as defined in Figure 3-5) for this logic gate.

W10. Compare the measured high-to-low (t_{PHL}) and low-to-high (t_{PLH}) propagation delays to the numerical predictions of your analysis in part W9.

W11. Discussion: How well does this circuit meet the "instantaneous" functional goal expressed in section L11? Can you suggest any changes in the circuit that would improve delay performance?

Would these changes have any other effects on circuit performance (e.g. output high and low logic levels as discussed in part W6).

LIGHT EMITTING DIODE (LED) DRIVER

W12. Design: Using your data from part L6 for r_{DS} with a +5V gate drive at v_{GS}, determine the resistance R_2 required so that the total resistance ($R_2 + r_{DS}$) gives a 5mA LED current. Also, indicate the value actually used (e.g. closest standard value available in your ECE lab kit).

W13. Did the value chosen for R_2 from your design provide enough LED current for adequate LED illumination? At what switching frequency was the LED flashing no longer perceptible?

AUTOMATIC SHUTOFF SWITCH

W14. Discussion: Describe (qualitatively) the operation of the circuit. If you were able to make quantitative measurements of the delay time, report those as well. How was the delay time affected by changes in capacitor C_T?

W15. Explain (qualitatively AND quantitatively) how this circuit works. Hint: this is one case in which we can't assume the reverse bias current (also called leakage current) of the 1N4148 to be negligible!

W16. Analysis: Derive an equation for the (approximate) delay time to LED shutoff in terms of capacitor C_T, the reverse leakage current I_L of the 1N4148, and the threshold voltage V_t of the MOSFET.
(Major hint: In the reverse bias region, we can model the 1N4148 as a current source with a value of order $I_L \approx 10nA$; check your Lab 1 results for the reverse bias current value you measured).

W17. In your equation from part W16, plug in the value(s) you used for C_T, your extracted V_t from part W4, and your measured I_L for the 1N4148 from your Lab 1 results. Compare this predicted delay to the delay observed in the lab in part W14. Note: if you're within a factor of 2X, that's pretty good! The leakage current of the diode is very sensitive to temperature (doubles approximately every 10°C) so the actual I_L for the 1N4148 is probably different from your Lab 1 results.