ECE 2201
Term A-2023

Problem Set 4

Due: Monday, September 25, 2023

NOTES:
(1) You must show all work to receive credit. Answers alone are not sufficient.

(2) The book problems may have been used before and I am sure solutions are floating about. Be sure you know how to do these problems ON YOUR OWN, since you will be tested in each area.

Section 5.3: MOSFET Circuits at DC (pg. 298)

1. D5.43
2. D5.45 *(Note: This problem refers to Fig. E5.10 which is on page 277.)*
3. 5.47
4. D5.48 (PMOS)
5. D5.49
6. 5.53
7. 5.54 (a) (V1 through V7)

* Problems 8-10 have been graciously provided by Prof. McNeill (see attached)

8. CMOS Inverter and Propagation Delays
9. MOSFET Logic Gate
10. How small is "small v_{DS}", anyway?

8. CMOS Inverter and Propagation Delays

Figure 4-1 shows a CMOS logic inverter driving a capacitive load of 100pF, and being controlled by a digital input signal *Vin* switching between 0 and 5V. Several parameters are also given for each MOSFET, and the supply voltage is 5V. ***NOTE: The process parameters for the devices are NOT equal!***

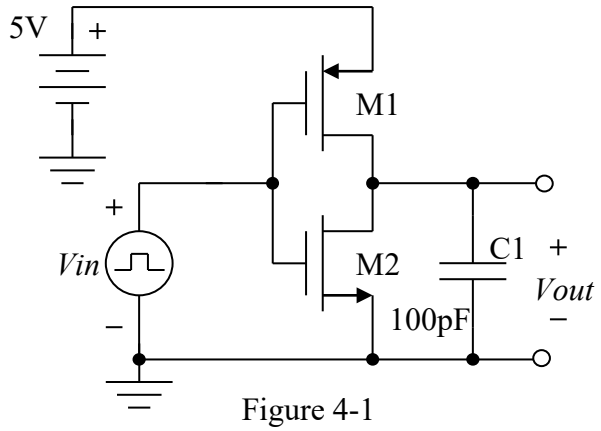

Figure 4-1

M1 : P-Channel
$W_p = 50\mu m$
$L_p = 10\mu m$
$k'_p = 70\mu A / V^2$
$|V_{tp}| = 1.1V$

M2: N-Channel
$W_n = 50\mu m$
$L_n = 10\mu m$
$k'_n = 150\mu A / V^2$
$V_{tn} = 1.1V$

a) Determine the *propagation delays* $\mathbf{t_{PLH}}$ (low-to-high output transition) and $\mathbf{t_{PHL}}$ (high-to-low output transition) for this CMOS inverter.

NOTE: Use the simple resistor/switch MOSFET models presented in class.

b) If Vin is a 2MHz, 0 to 5V square wave with a 50% duty cycle, sketch two cycles of the input and output voltage waveforms to scale, relative to one another.

c) One desirable feature of a CMOS inverter is to have equal propagation delays. Assuming that the channel length, L of each device is fixed, what new width should the PMOS device have, in order to achieve this result?

(d) Repeat part (a), but use the constant saturation current model for each MOSFET when it turns on, instead of the resistor model.

(e) How do the propagation delays compare to the resistive model?

9. MOSFET Logic Gate Analysis

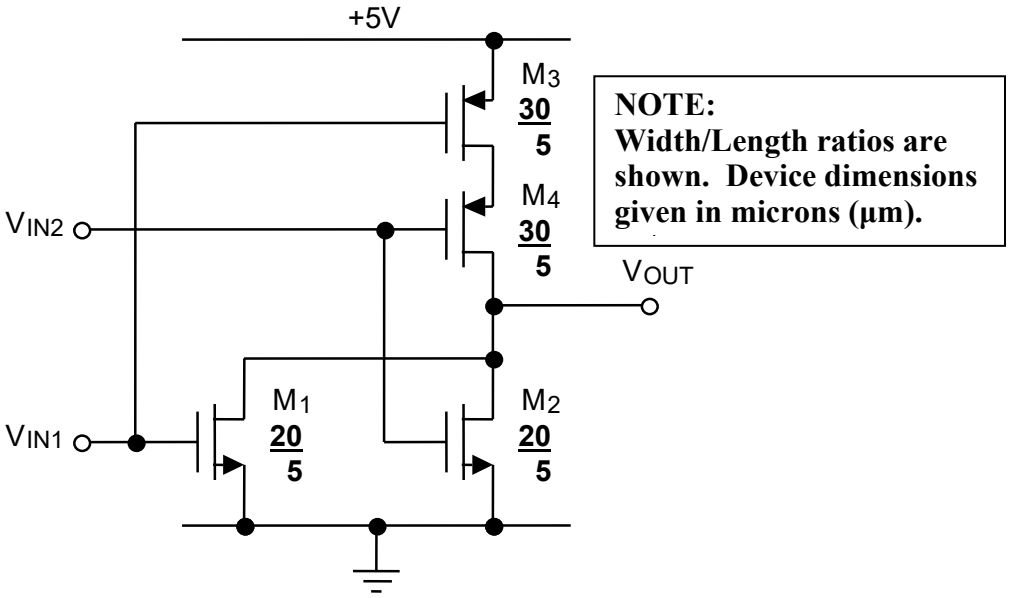

Figure 1.0

a) Fill in the table below showing the state of each MOSFET (ON or OFF) and the output voltage for each combination of input logic states.

b) If 0V represents a logic low, and +5V represents a logic high, what is the logic gate function of this circuit?

V_{IN1}	V_{IN2}	M_1	M_2	M_3	M_4	V_{OUT}
0V	0V					
0V	+5V					
+5V	0V					
+5V	+5V					

c) If $k_n' = 50uA/V^2$, $k_p' = 25uA/V^2$ AND $V_{tn}=|V_{tp}|= 1.2V$, determine the output resistance *Rout*, of this logic gate for each input combination. **NOTE: Don't forget to include the device dimensions!**

IN1	IN2	Rout
0	0	
0	1	
1	0	
1	1	

10. How small is "small v_{DS}", anyway?

The full triode region equation:

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS}-V_t)v_{DS}-\frac{1}{2}v_{DS}^{\,2}\right] \qquad \text{(Eq.1)}$$

gives a nonlinear relationship between v_{DS} and i_D, due to the v_{DS}^2 term. Assuming the v_{DS}^2 term to be negligible allowed us to approximate the relationship between v_{DS} and i_D as linear, which gives a resistive behavior:

$$\frac{v_{DS}}{i_D} = r_{DS} = \frac{1}{k_n'\left(\frac{W}{L}\right)(v_{GS}-V_t)} \qquad \text{(Eq.2)}$$

Several people have asked, what is a "small enough" v_{DS}? The answer depends on how accurate you need to be. As v_{DS} gets larger, the difference between Eq.1 and Eq.2 gets larger (see Figure 2.0 below).

a) Find a **value for the fraction v_{DS} / (v_{GS}-V_t)**, for which the current **i_D** predicted by the resistive approximation of Eq.2 is within **10%** of the actual current value given by the full triode model of Eq.1?

b) For what fraction is the error less than **1%**?

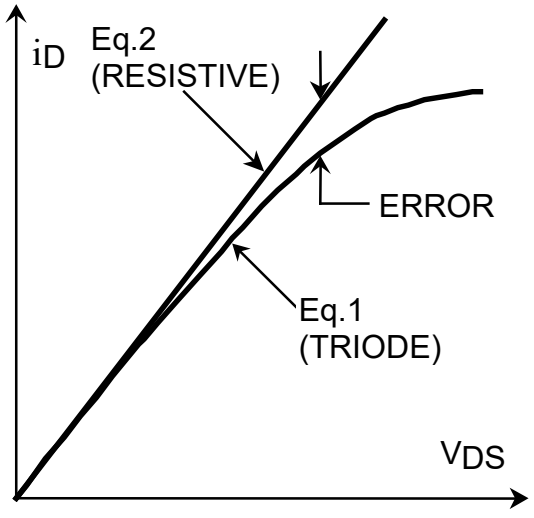

Figure 2.0