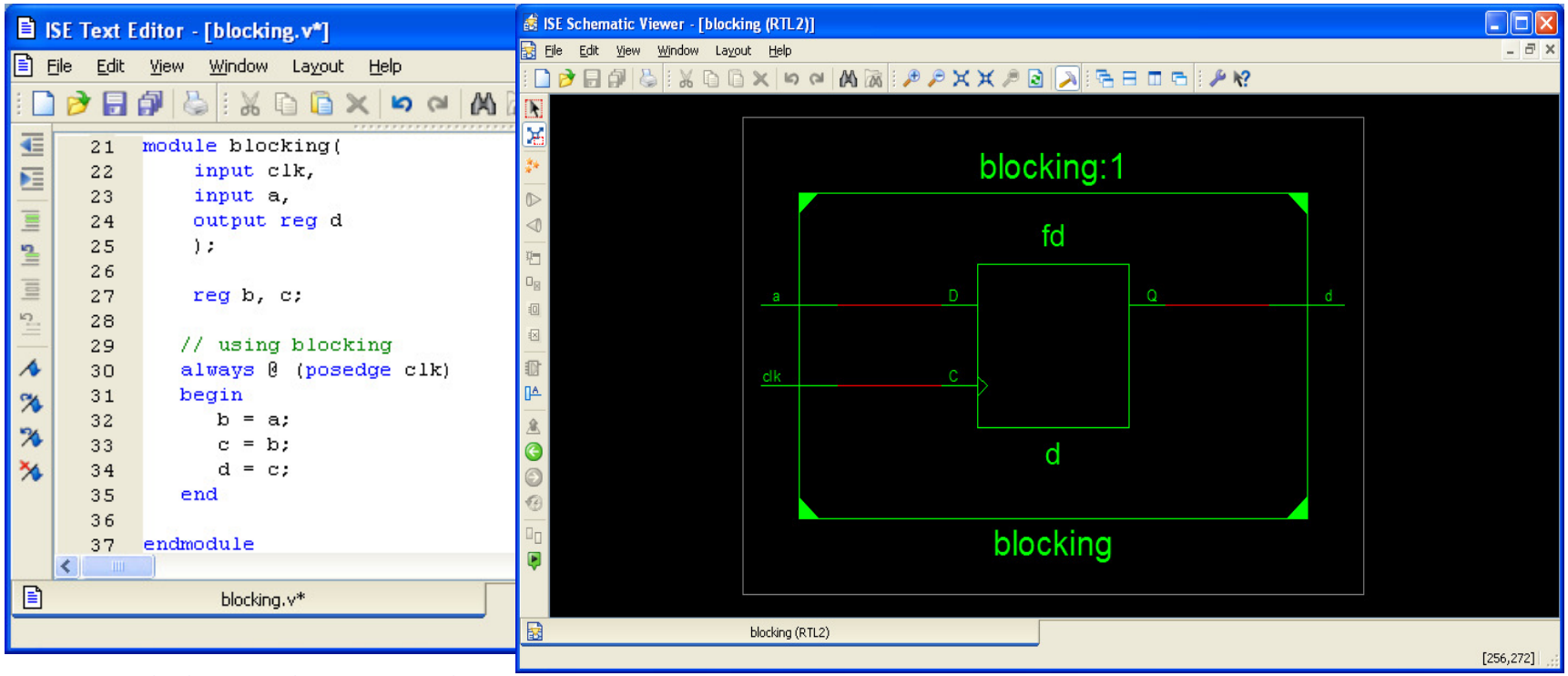
Verilog

Misc

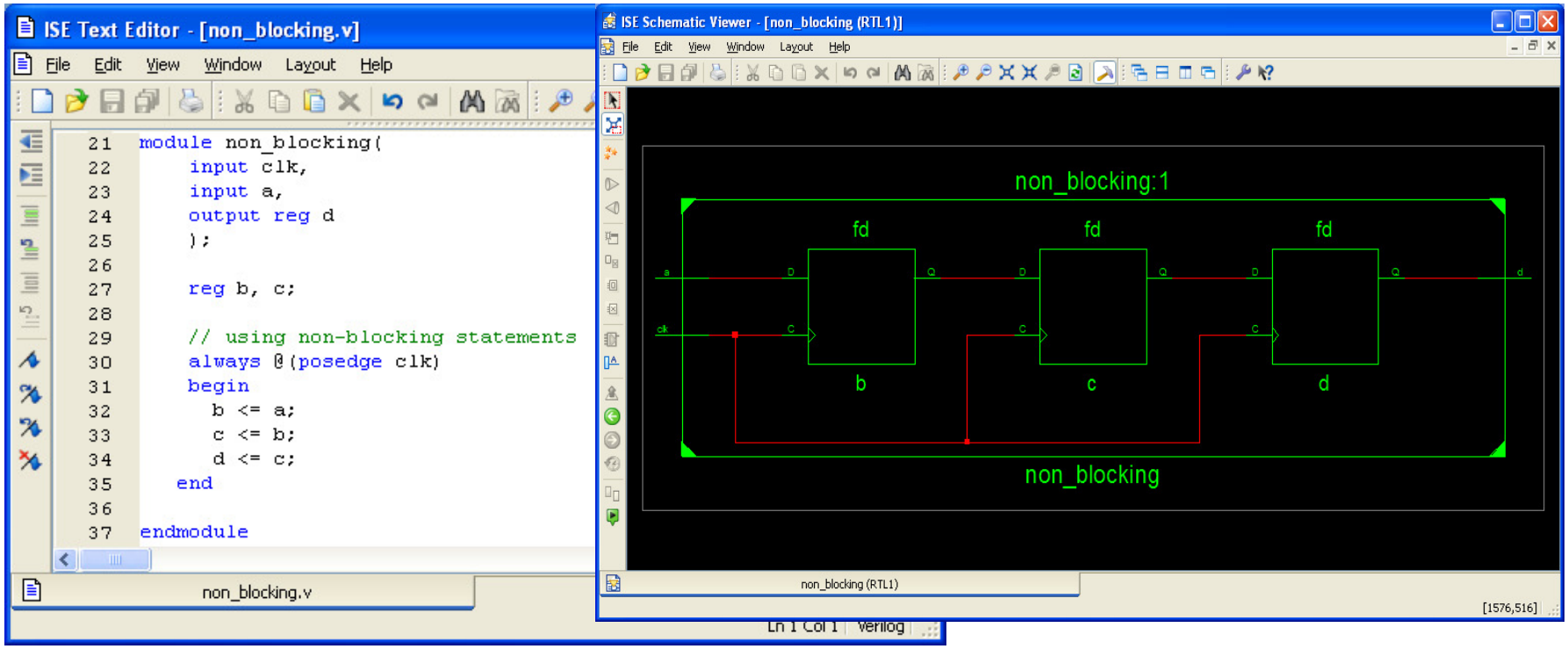
(blocking, time constraints, clocks, customizing modules)

Blocking Example (incorrect result)




```
Synthesizing Unit <blocking>.
WARNING:Xst:646 - Signal <c> is assigned but never used. This unconnected signal
will be trimmed during the optimization process.
WARNING:Xst:646 - Signal <b> is assigned but never used. This unconnected signal
will be trimmed during the optimization process.
    Found 1-bit register for signal <d>.
    Summary:
          inferred   1 D-type flip-flop(s).
Unit <blocking> synthesized.
```

Non-Blocking (expected result)




```
Synthesizing Unit <non_blocking>.
    Related source file is "non_blocking.v".
    Found 1-bit register for signal <d>.
    Found 1-bit register for signal <b>.
    Found 1-bit register for signal <c>.
    Summary:
          inferred   3 D-type flip-flop(s).
Unit <non_blocking> synthesized.
```

Timing Constraints

- Used to guide the synthesis tools
- Example 32-bit counter - no constraints (speed grades -4 and -5)

```
=========================================================
Advanced HDL Synthesis Report
Macro Statistics
# Counters                      : 1
 32-bit up counter              : 1
=========================================================
Timing Summary:
---------------
Speed Grade: -4
   Minimum period: 6.680ns (Maximum Frequency: 149.703MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 8.094ns
   Maximum combinational path delay: No path found
=========================================================
Speed Grade: -5
   Minimum period: 5.767ns (Maximum Frequency: 173.400MHz)
```

Adding timing constraint

- Add to UCF file:
  - `NET "clk" PERIOD = 6ns HIGH 50%;`

```
WARNING:Par:62 - Your design did not meet timing.
-------------------------------------------------------------------------------
  Constraint  | Check | Worst Case | Best Case | Timing |Timing | Slack | Achievable |
   Errors | Score
-------------------------------------------------------------------------------
* NET "clk_BUFGP/IBUFG" PERIOD = 6 ns HIGH  | SETUP| -0.456ns | 6.456ns |  9| 1430
  50%                                       | HOLD | 2.432ns  |         |  0|    0
-------------------------------------------------------------------------------
1 constraint not met.
```

Try relaxing constraint

- `NET "clk" PERIOD = 6.5ns HIGH 50%;`

```
--------------------------------------------------------------------------------
Constraint | Check| Worst Case | Best Case | Timing | Timing | Slack| Achievable |
   Errors |    Score
--------------------------------------------------------------------------------
  NET "clk_BUFGP/IBUFG" PERIOD = 6.5 ns HIG | SETUP| 0.203ns| 6.297ns| 0|  0
  H 50%                                     | HOLD | 2.280ns|        | 0|  0
--------------------------------------------------------------------------------
```

All constraints were met.

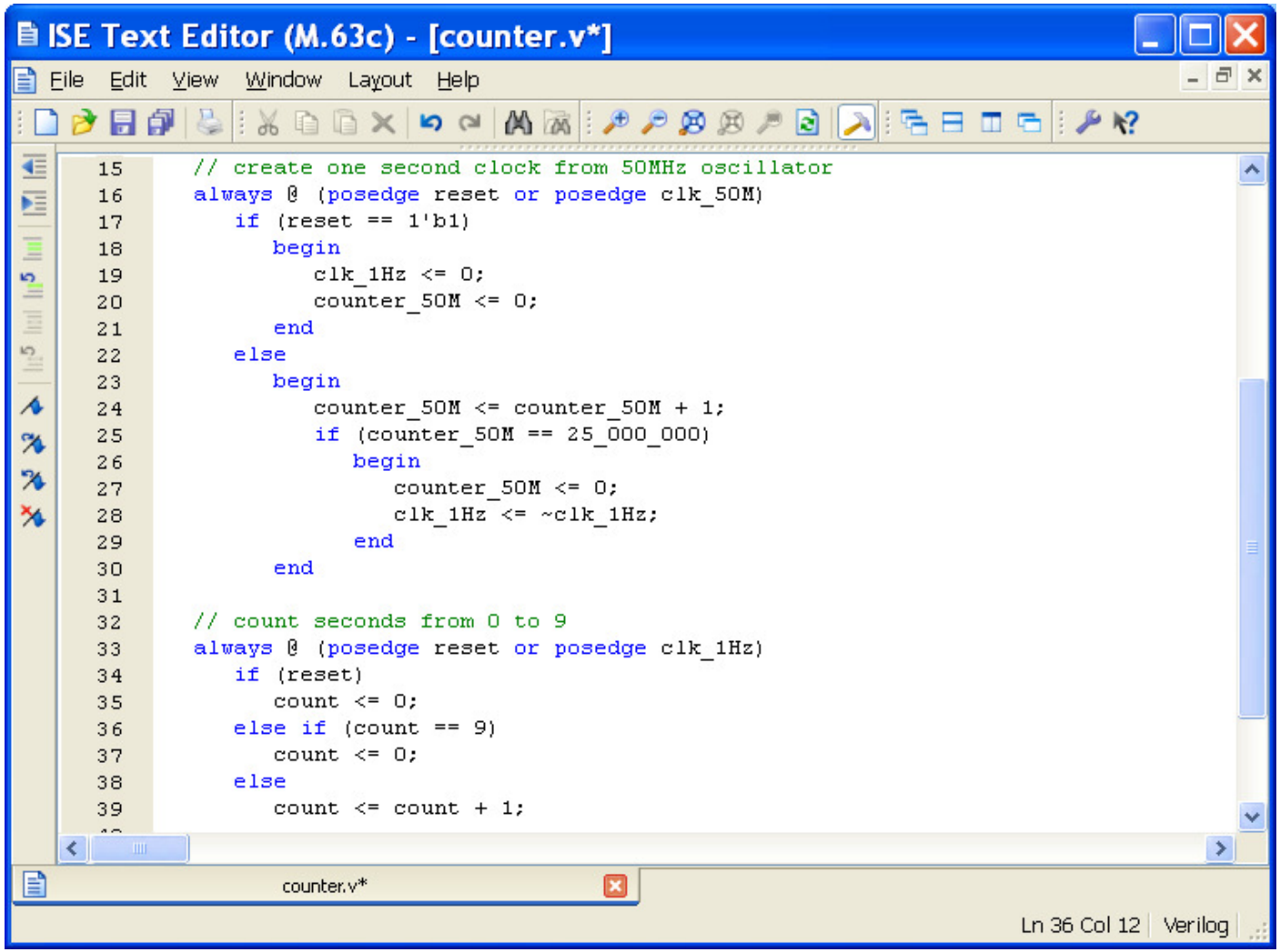
- Also see Timing Constraint User Guide
- Examples:

```
NET ‘abc’ OFFSET = OUT xx ns AFTER ‘clk’;
NET ‘def’ OFFSET = IN xx ns BEFORE ‘clk’;
```

Clock Skew

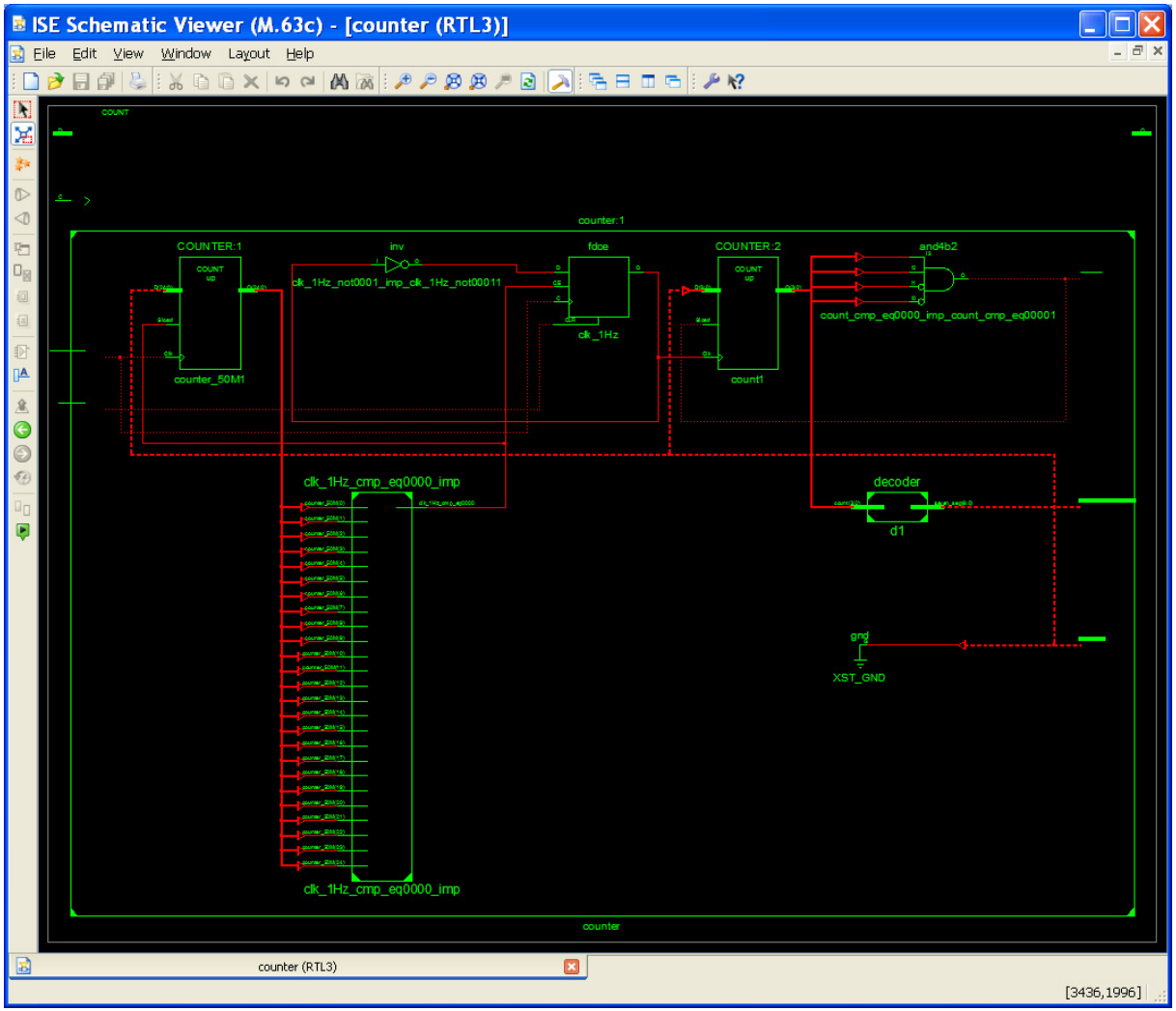
- The difference between the time a **clock** signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop.
  - Misalignment of clock edges
  - Degrades (reduces) time for flip-flop to flip-flop timing
- Can be caused by different things but wire interconnect delays are the main cause inside FPGAs
  - There are fast dedicated clock circuits and slower data paths

Old method of deriving slower clocks

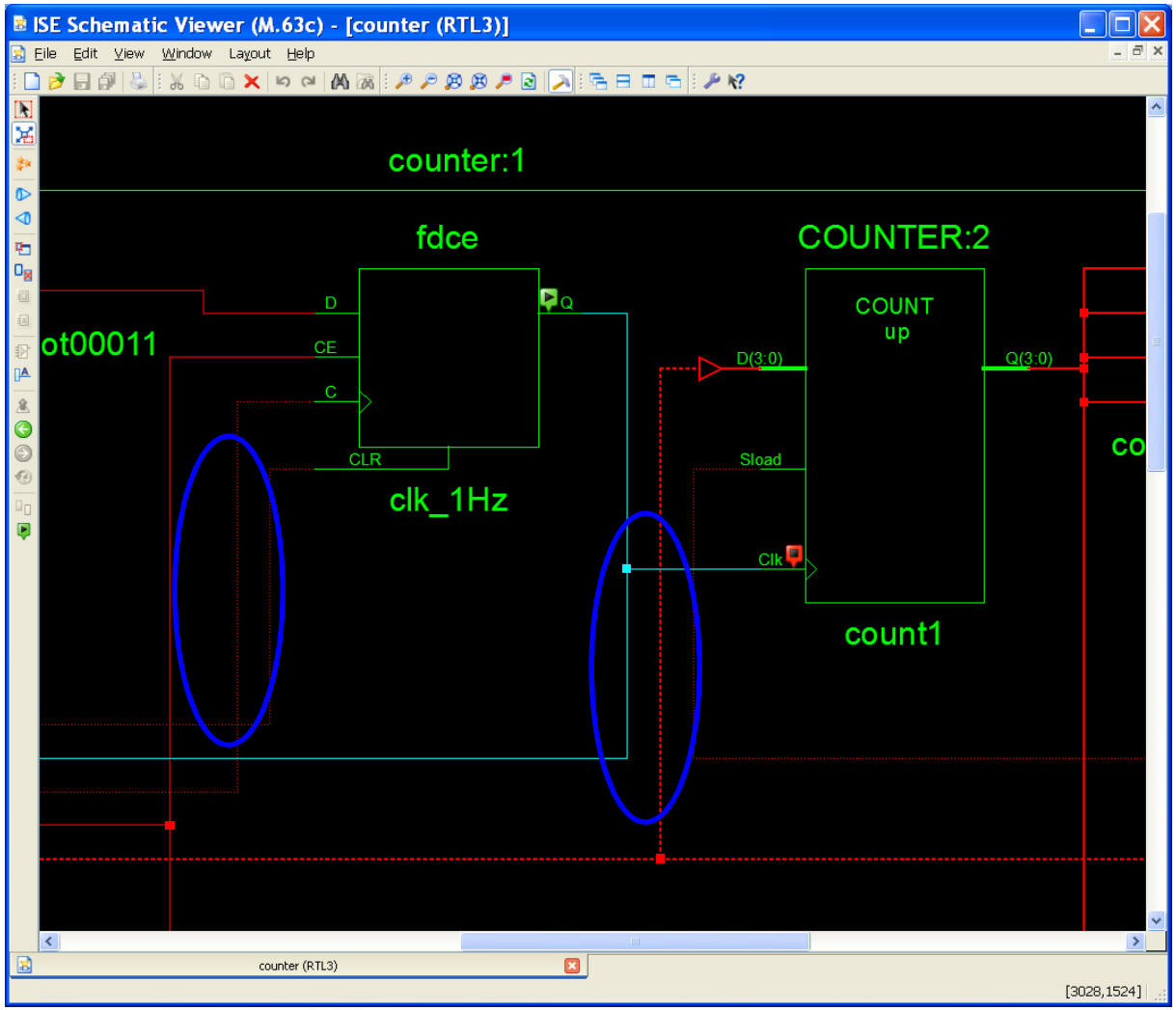


```
WARNING:Route:455 - CLK Net:clk_1Hz may have excessive
   skew because 0 CLK pins and 1 NON_CLK pins failed to
   route using a CLK template.
```

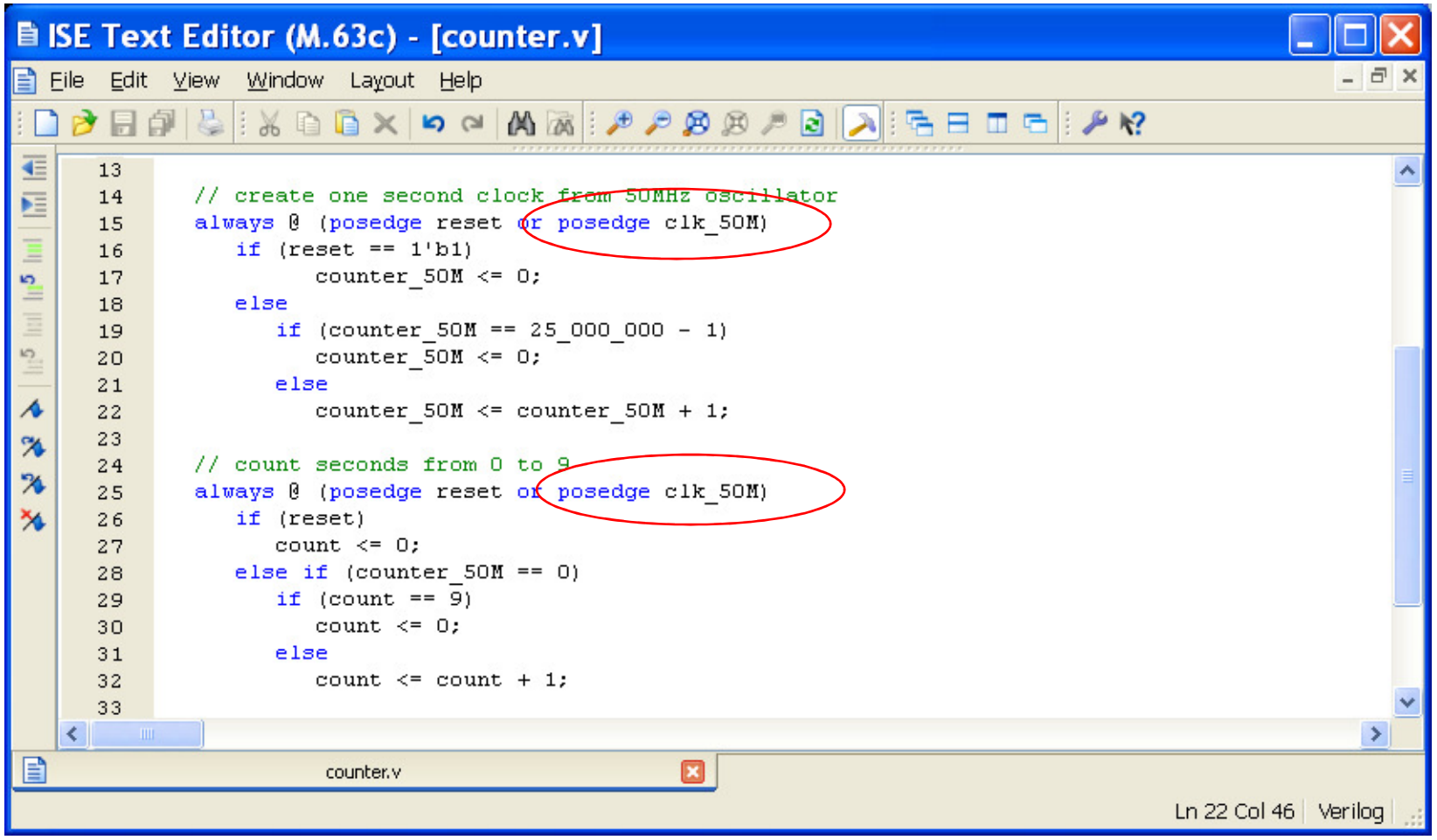
Synthesis uses two clock signals



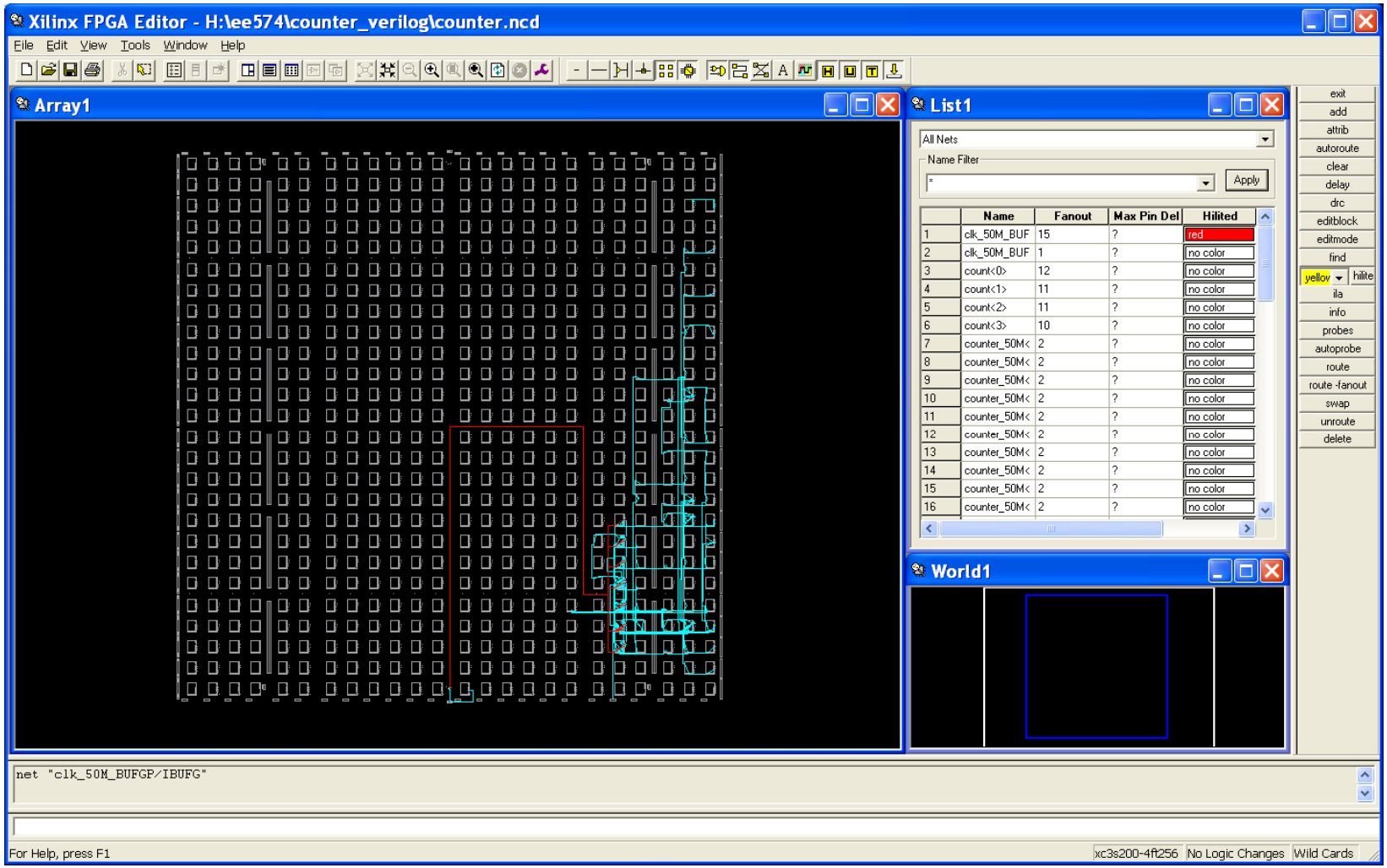
Two clock signals – not good!



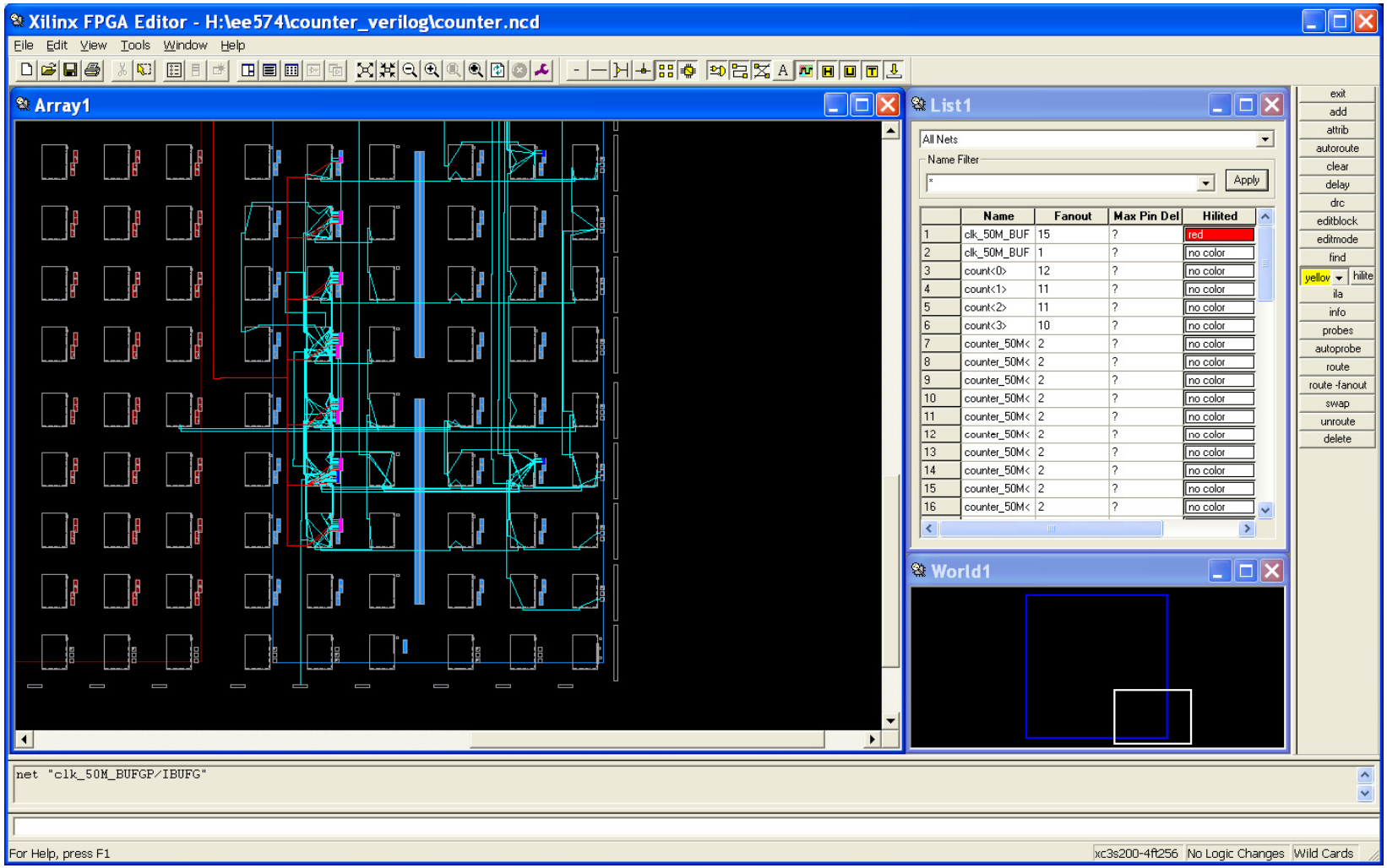
Modify to only use one clock signal



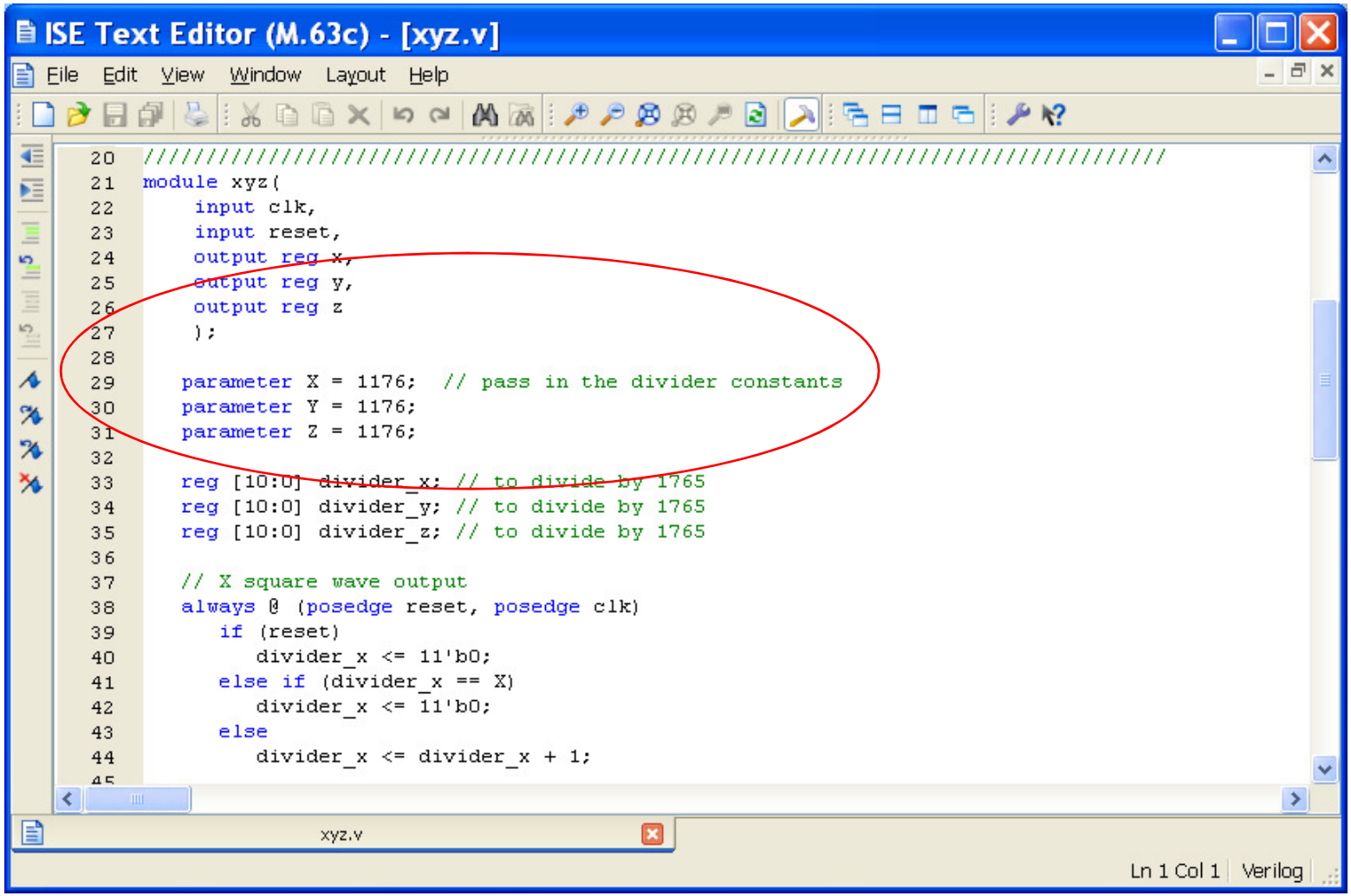
Clock signals use dedicated lines

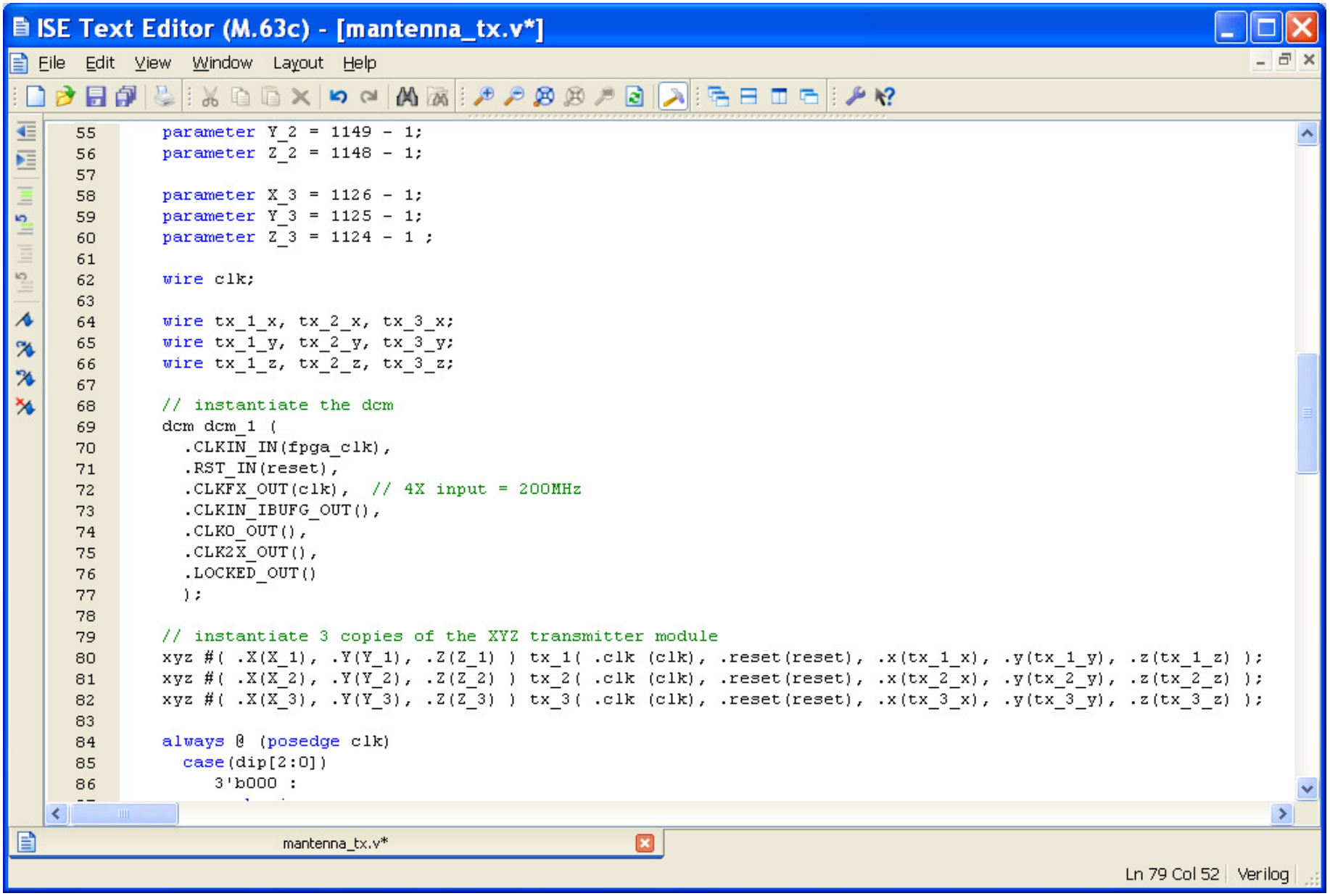


Clock drives all flip-flops

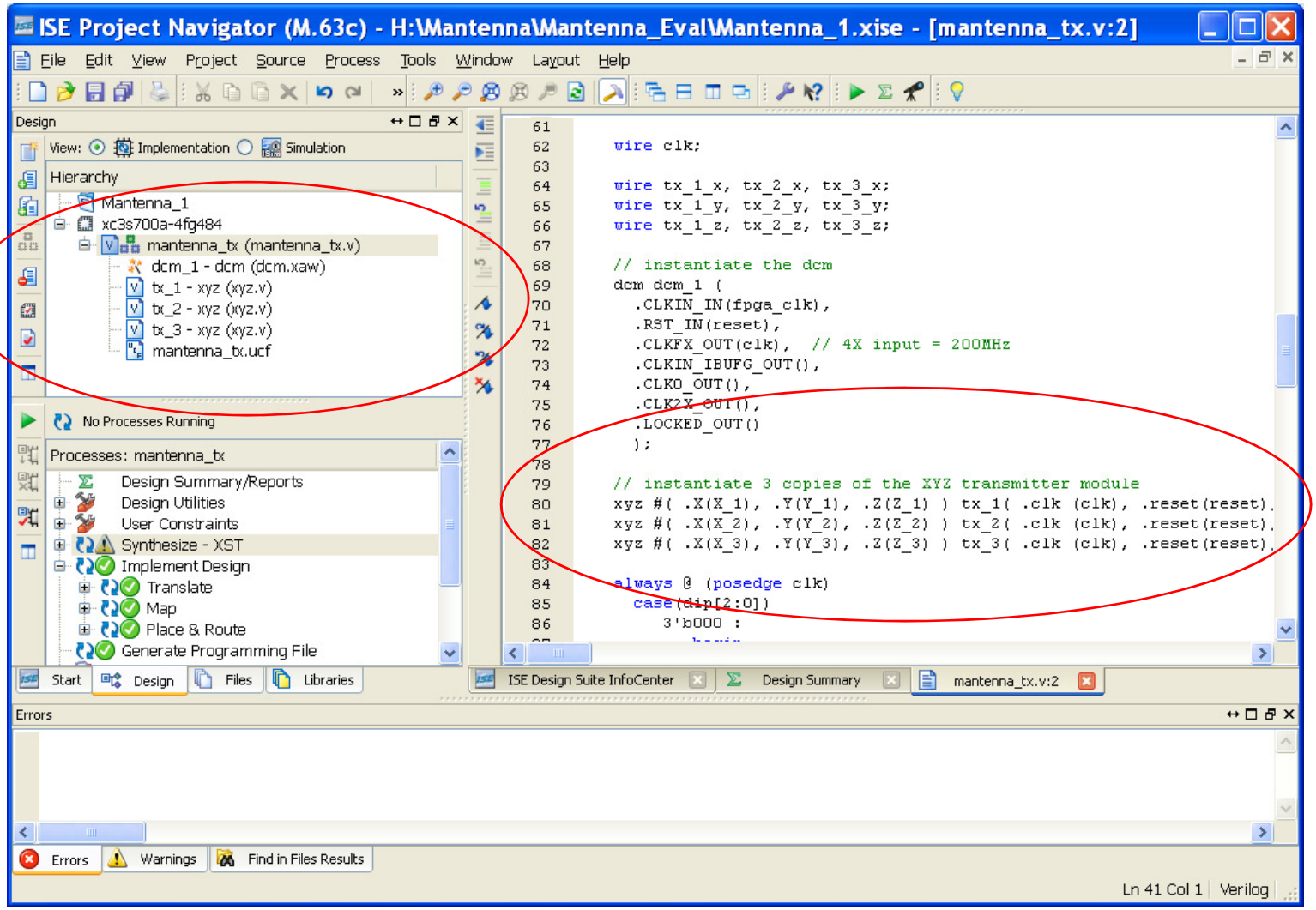


Verilog Lower Level Module with Parameters

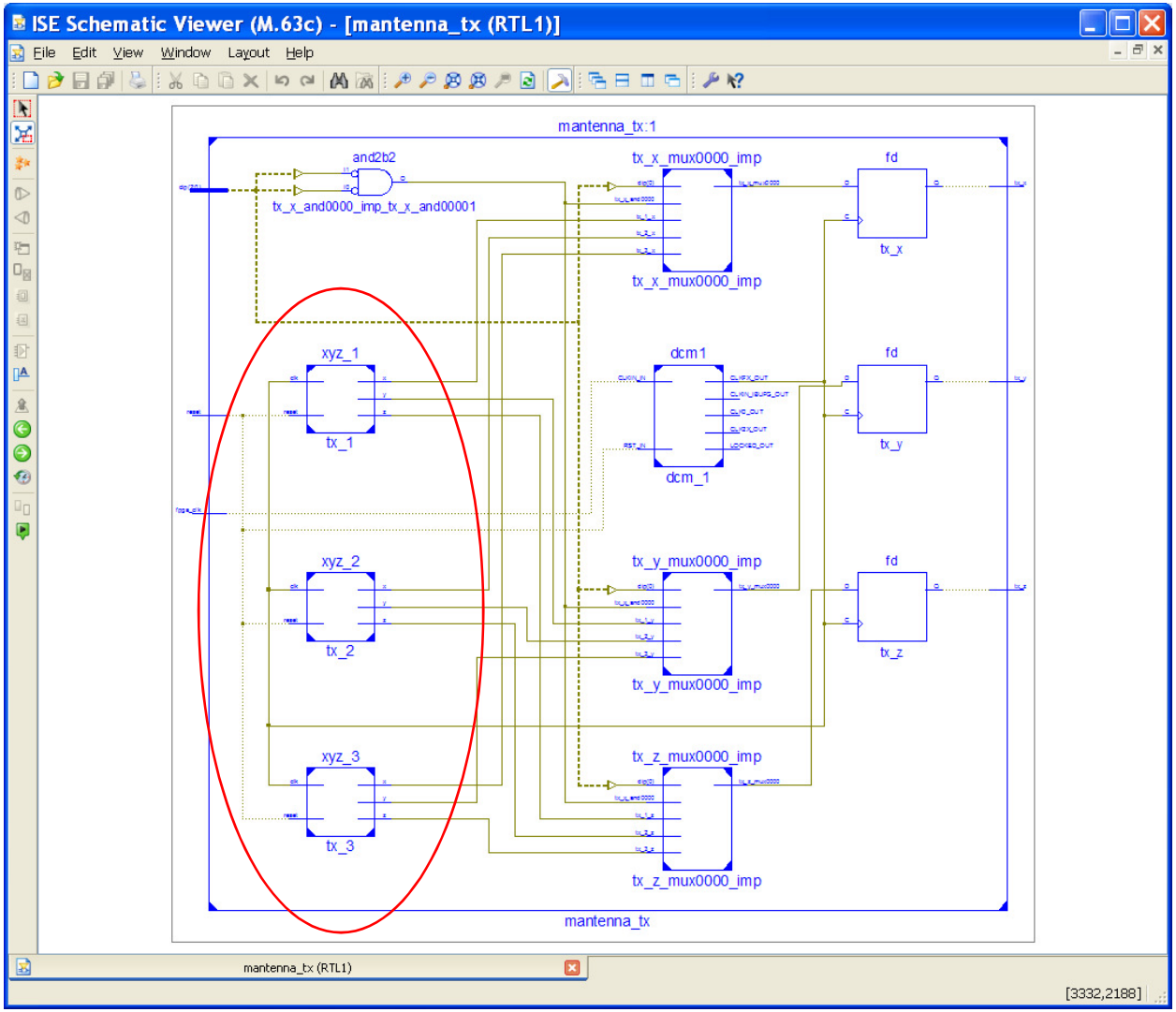



ISE Text Editor (M.63c) - [mantenna_tx.v*]
File Edit View Window Layout Help
55 parameter Y_2 = 1149 - 1;
56 parameter Z_2 = 1148 - 1;
57
58 parameter X_3 = 1126 - 1;
59 parameter Y_3 = 1125 - 1;
60 parameter Z_3 = 1124 - 1 ;
61
62 wire clk;
63
64 wire tx_1_x, tx_2_x, tx_3_x;
65 wire tx_1_y, tx_2_y, tx_3_y;
66 wire tx_1_z, tx_2_z, tx_3_z;
67
68 // instantiate the dcm
69 dcm dcm_1 (
70 .CLKIN_IN(fpga_clk),
71 .RST_IN(reset),
72 .CLKFX_OUT(clk), // 4X input = 200MHz
73 .CLKIN_IBUFG_OUT(),
74 .CLK0_OUT(),
75 .CLK2X_OUT(),
76 .LOCKED_OUT()
77);
78
79 // instantiate 3 copies of the XYZ transmitter module
80 xyz #(.X(X_1), .Y(Y_1), .Z(Z_1)) tx_1(.clk (clk), .reset(reset), .x(tx_1_x), .y(tx_1_y), .z(tx_1_z));
81 xyz #(.X(X_2), .Y(Y_2), .Z(Z_2)) tx_2(.clk (clk), .reset(reset), .x(tx_2_x), .y(tx_2_y), .z(tx_2_z));
82 xyz #(.X(X_3), .Y(Y_3), .Z(Z_3)) tx_3(.clk (clk), .reset(reset), .x(tx_3_x), .y(tx_3_y), .z(tx_3_z));
83
84 always @ (posedge clk)
85 case(dip[2:0])
86 3'b000 :
mantenna_tx.v*
Ln 79 Col 52 Verilog

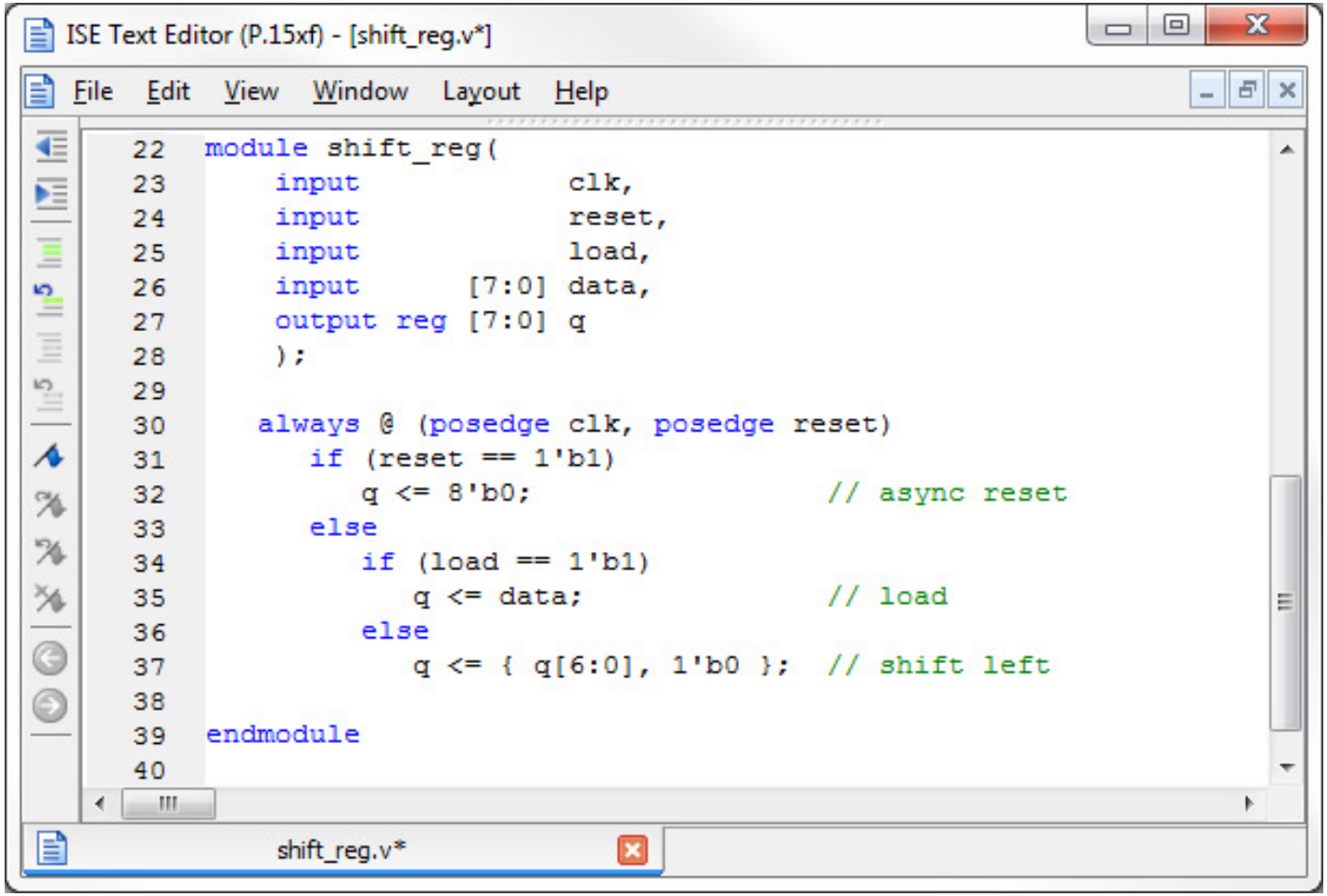
Three copies of XYZ module



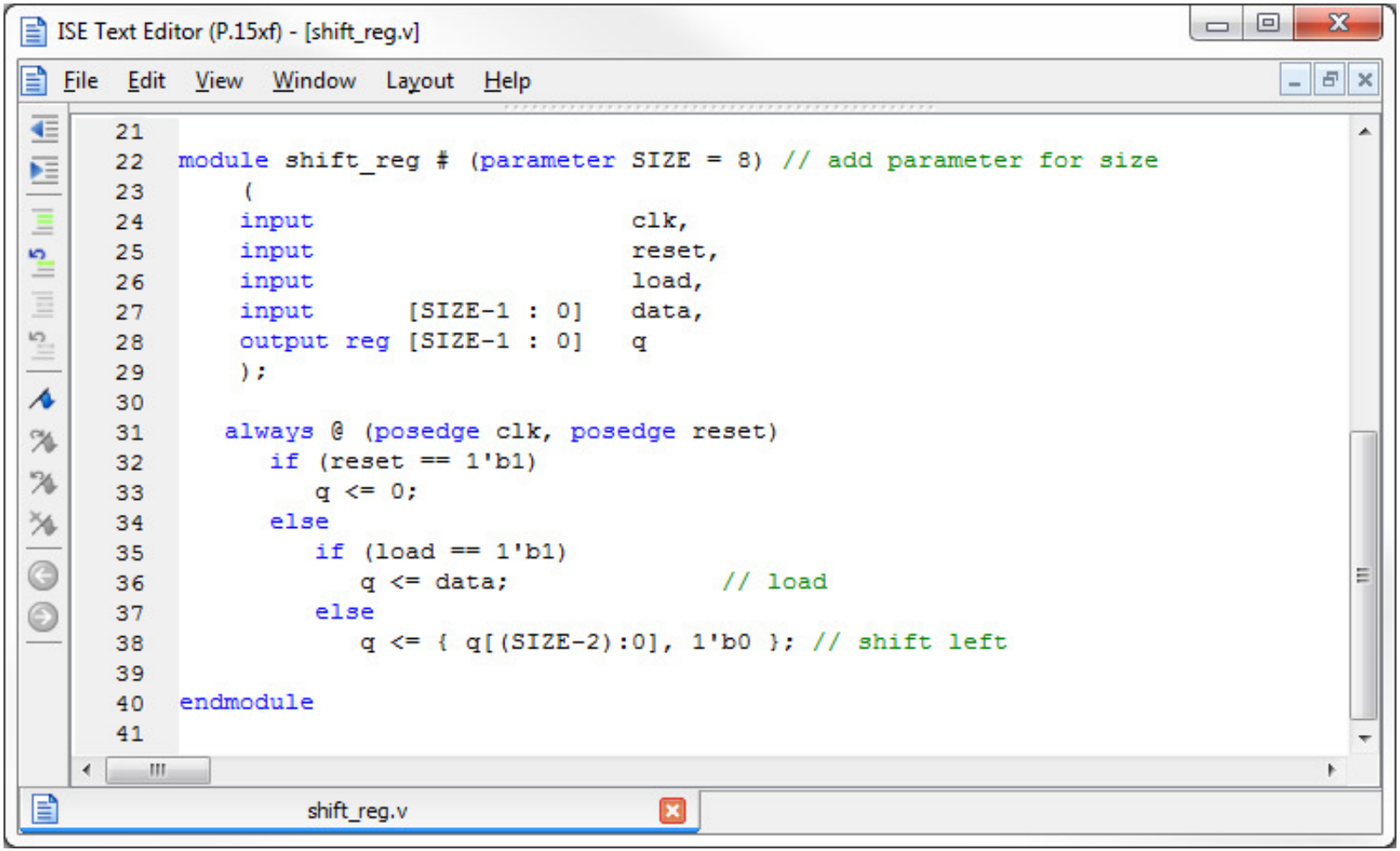
RTL Schematic showing 3 modules



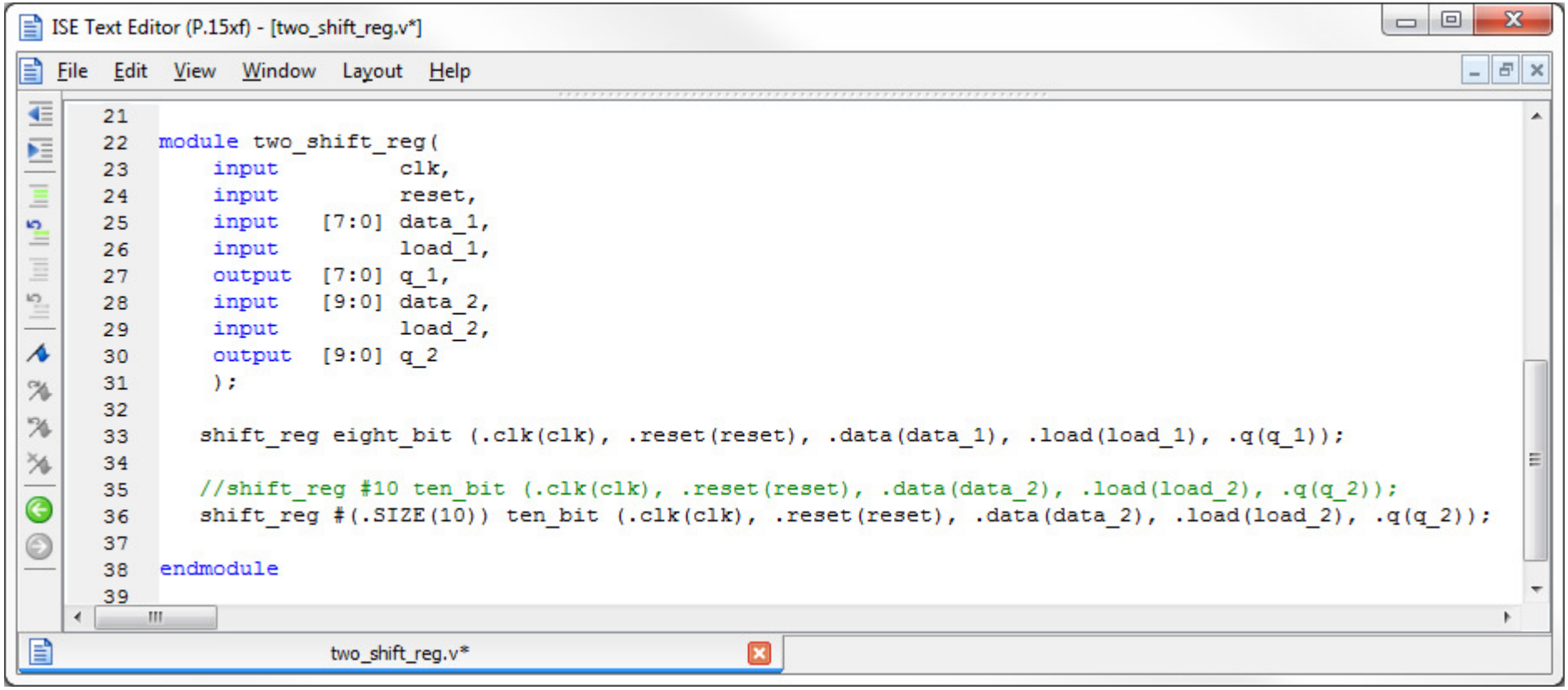
Shift Register – Fixed Size



Modifying Component Size

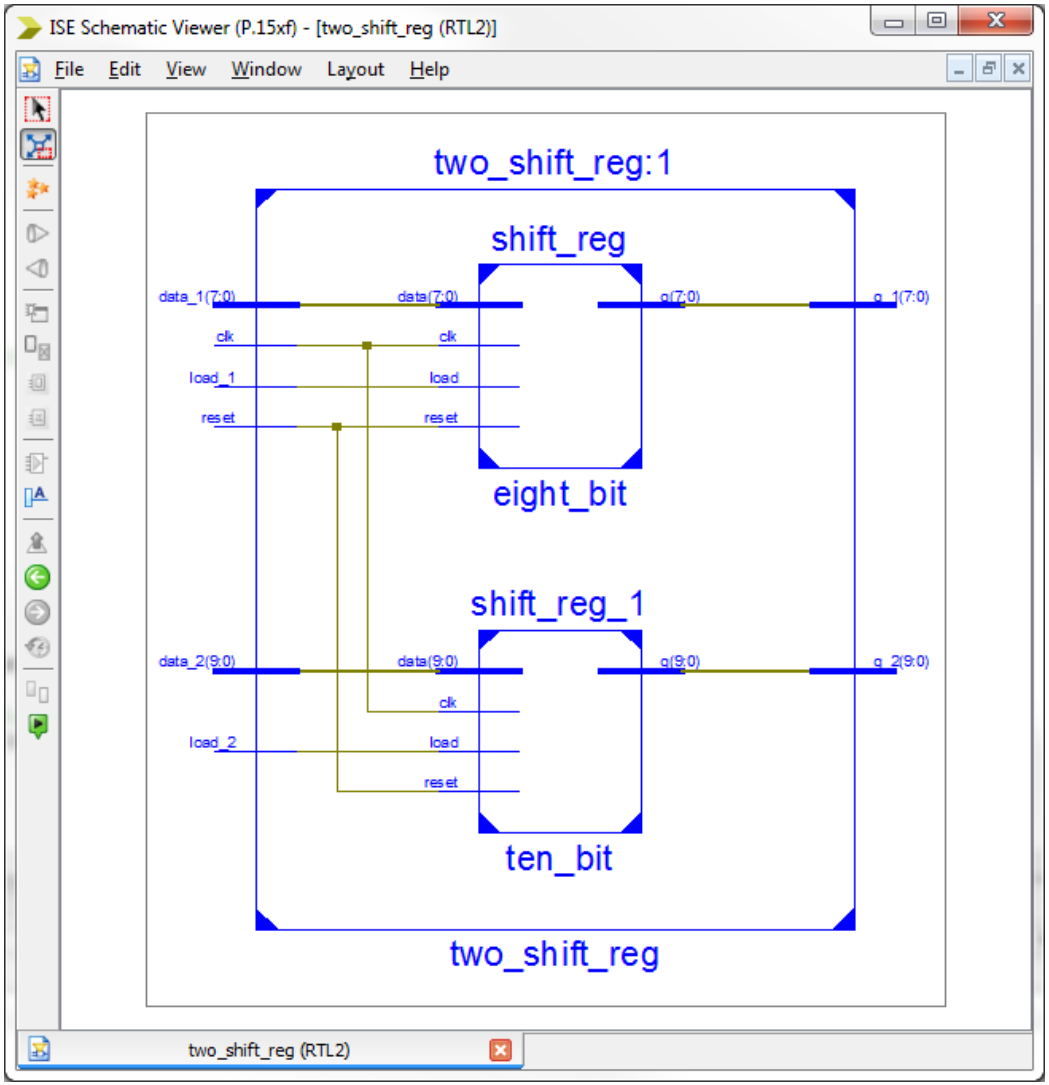


Making two copies – different size

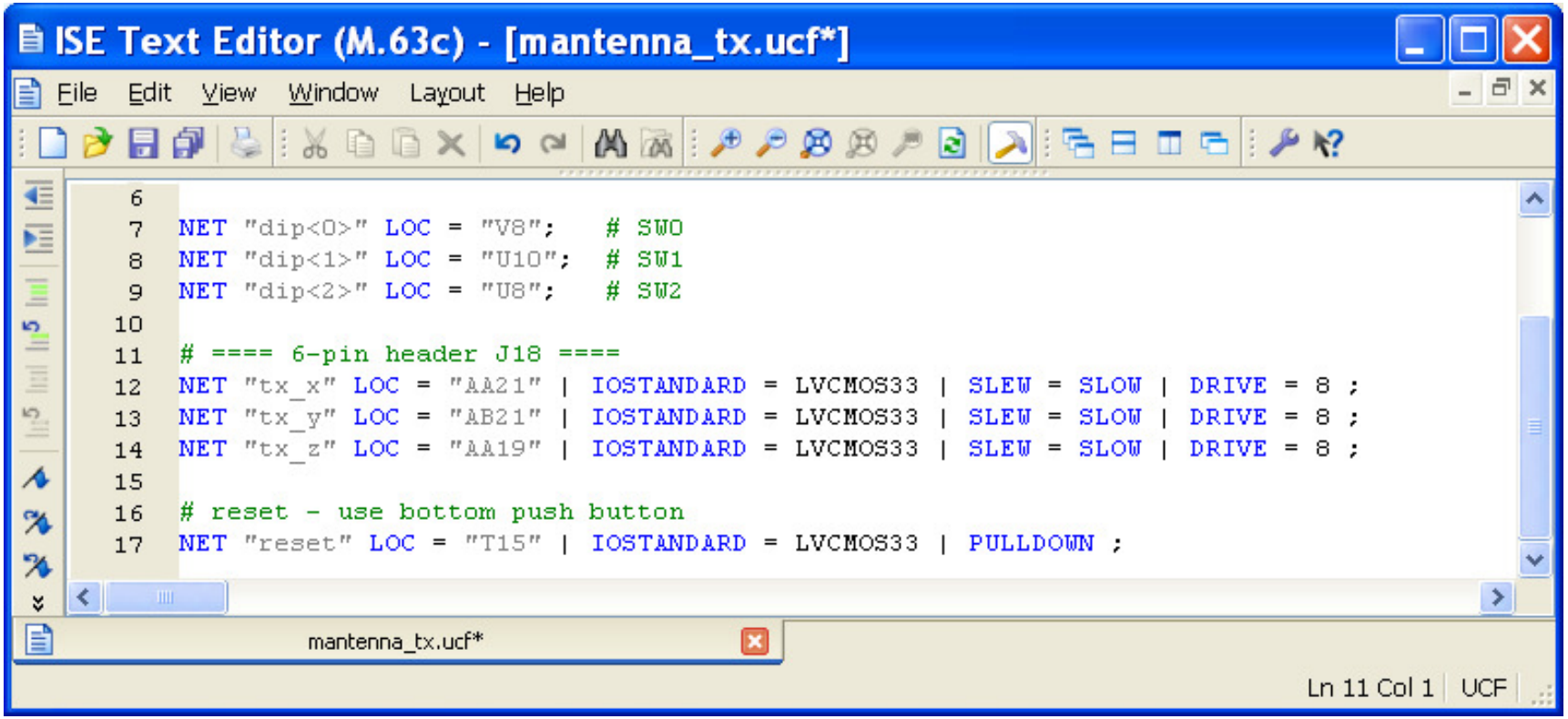


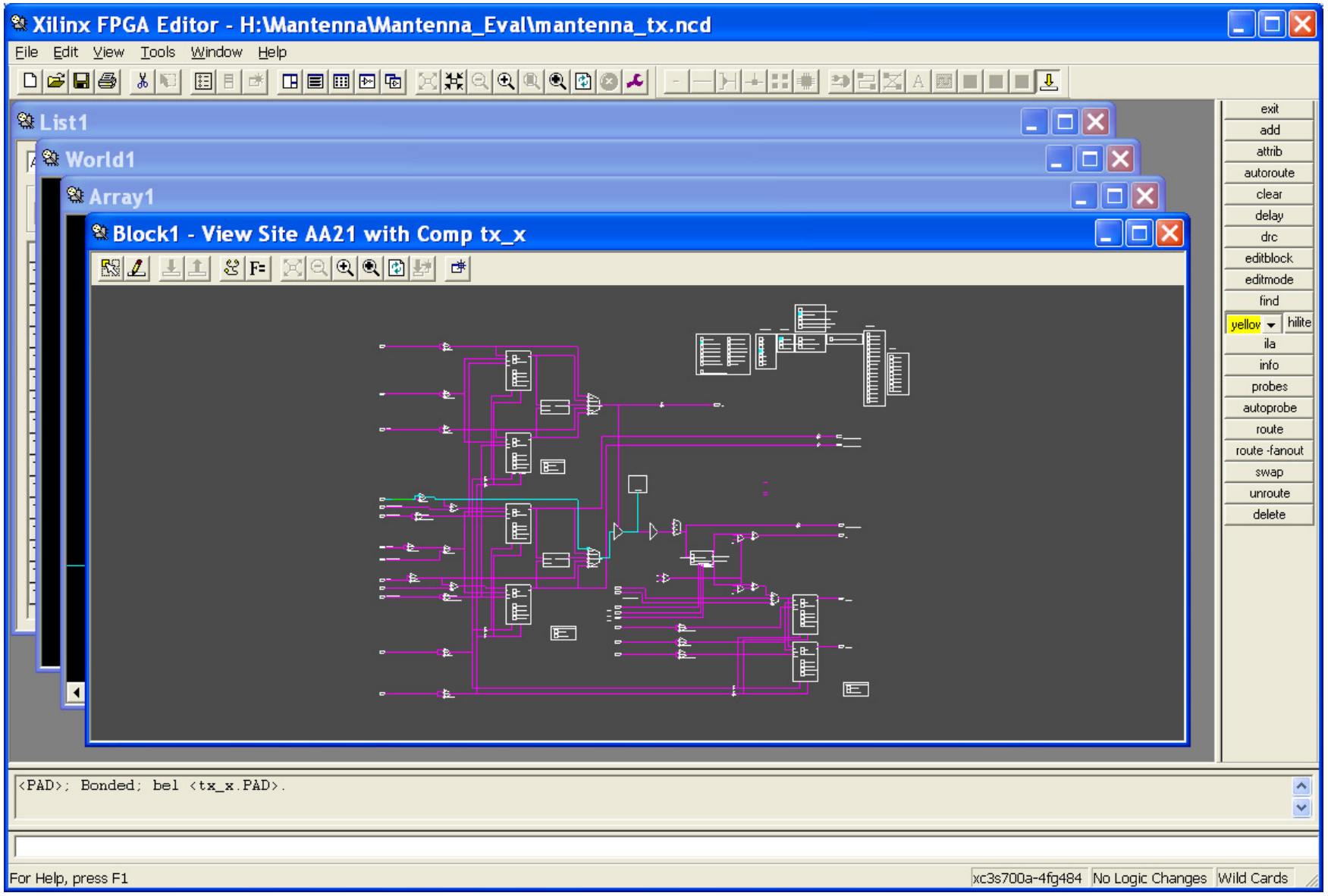

```
21
22  module two_shift_reg(
23      input          clk,
24      input          reset,
25      input    [7:0] data_1,
26      input          load_1,
27      output   [7:0] q_1,
28      input    [9:0] data_2,
29      input          load_2,
30      output   [9:0] q_2
31      );
32
33     shift_reg eight_bit (.clk(clk), .reset(reset), .data(data_1), .load(load_1), .q(q_1));
34
35     //shift_reg #10 ten_bit (.clk(clk), .reset(reset), .data(data_2), .load(load_2), .q(q_2));
36     shift_reg #(.SIZE(10)) ten_bit (.clk(clk), .reset(reset), .data(data_2), .load(load_2), .q(q_2));
37
38  endmodule
39
```

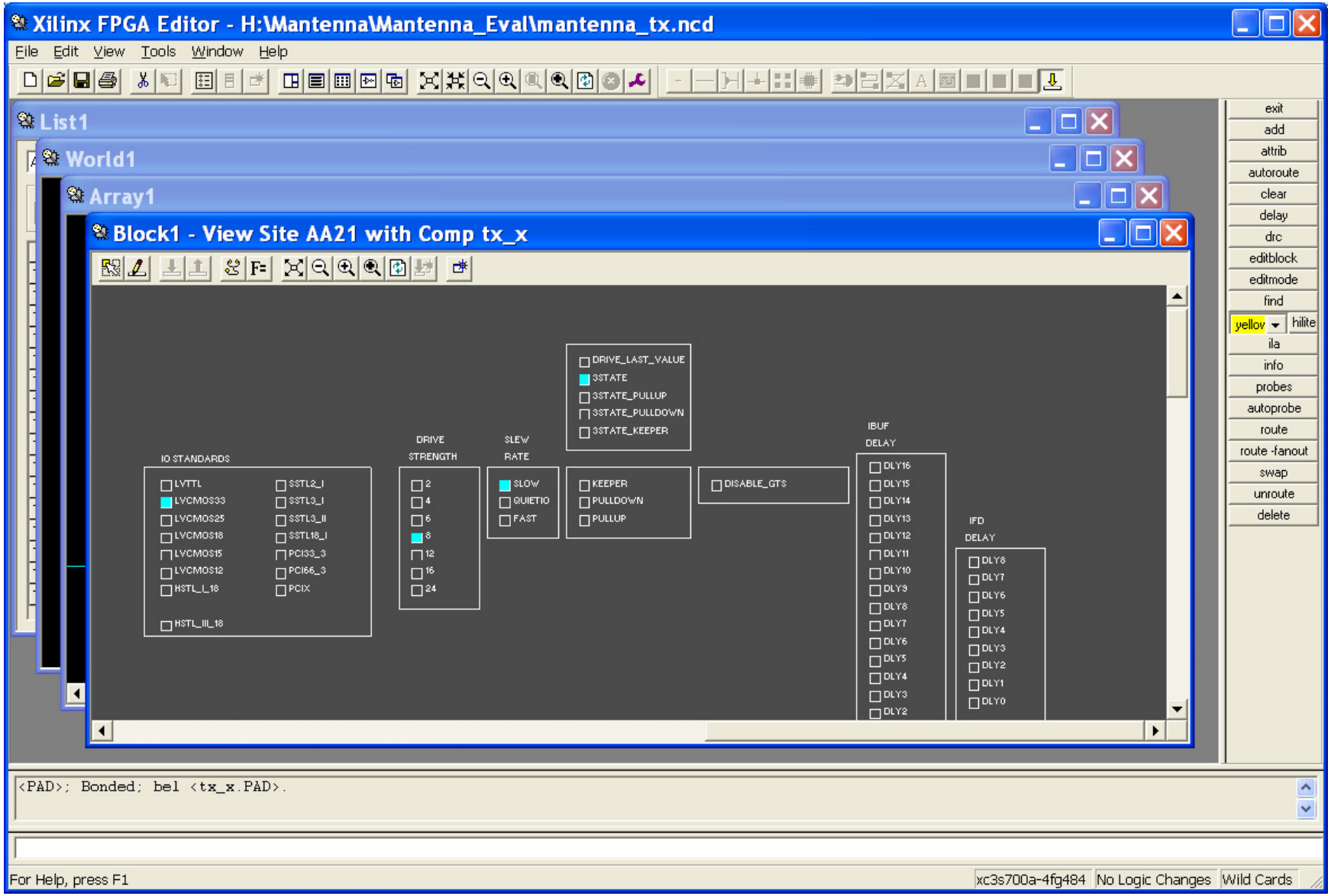
Schematic of two shift registers



(Misc) Using UCF to specify pin options




Xilinx FPGA Editor - H:\Mantenna\Mantenna_Eval\mantenna_tx.ncd
File Edit View Tools Window Help
List1
World1
Array1
Block1 - View Site AA21 with Comp tx_x
exit
add
attrib
autoroute
clear
delay
drc
editblock
editmode
find
yellow
hilite
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
delete
<PAD>; Bonded; bel <tx_x.PAD>.
For Help, press F1
xc3s700a-4fg484
No Logic Changes
Wild Cards


Xilinx FPGA Editor - H:\Mantenna\Mantenna_Eval\mantenna_tx.ncd
File Edit View Tools Window Help
List1
World1
Array1
Block1 - View Site AA21 with Comp tx_x
IO STANDARDS
LVTTL
LVCMOS33
LVCMOS25
LVCMOS18
LVCMOS15
LVCMOS12
HSTL_I_18
HSTL_III_18
SSTL2_I
SSTL3_I
SSTL3_II
SSTL18_I
PCI33_3
PCI66_3
PCIX
DRIVE STRENGTH
2
4
6
8
12
16
24
SLEW RATE
SLOW
QUIETIO
FAST
DRIVE_LAST_VALUE
3STATE
3STATE_PULLUP
3STATE_PULLDOWN
3STATE_KEEPER
KEEPER
PULLDOWN
PULLUP
DISABLE_GTS
IBUF DELAY
DLY16
DLY15
DLY14
DLY13
DLY12
DLY11
DLY10
DLY9
DLY8
DLY7
DLY6
DLY5
DLY4
DLY3
DLY2
IFD DELAY
DLY8
DLY7
DLY6
DLY5
DLY4
DLY3
DLY2
DLY1
DLY0
exit
add
attrib
autoroute
clear
delay
drc
editblock
editmode
find
yellow
hilite
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
delete
<PAD>; Bonded; bel <tx_x.PAD>.
For Help, press F1
xc3s700a-4fg484
No Logic Changes
Wild Cards