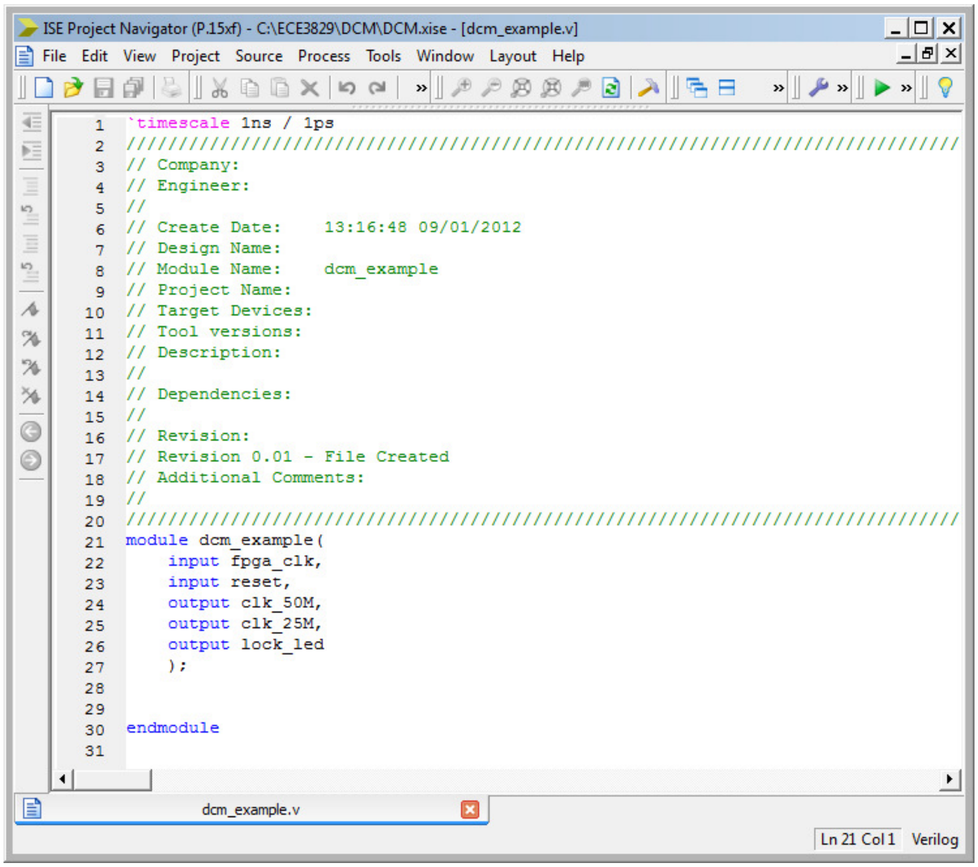
This tutorial shows how to create a simple project using a DCM (Digital Clock Manager).
(Jim Duckworth/Myo Thaw – August 2012)

The DCM generates 50MHz and 25MHz signals from the 50MHz xtal clock connected to the FPGA.

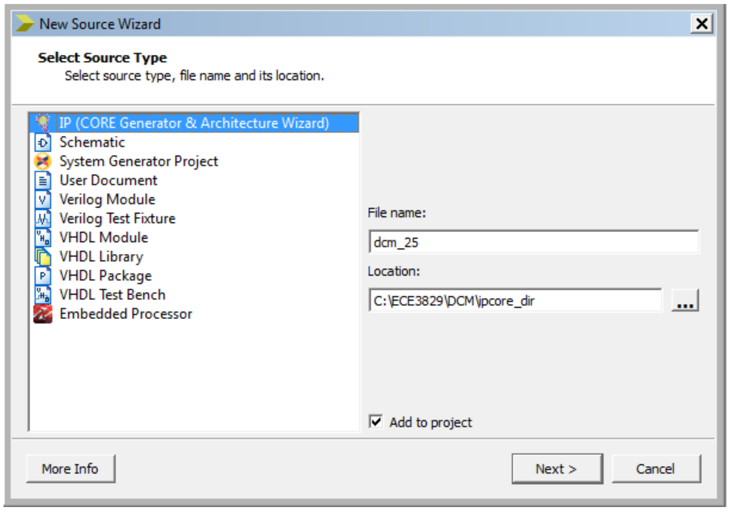
Create a simple module with the following ports:



```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:16:48 09/01/2012
// Design Name:
// Module Name:    dcm_example
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module dcm_example(
    input fpga_clk,
    input reset,
    output clk_50M,
    output clk_25M,
    output lock_led
    );


endmodule
```

Add a new IP source: Call it dcm_25 (for 25MHz DCM)



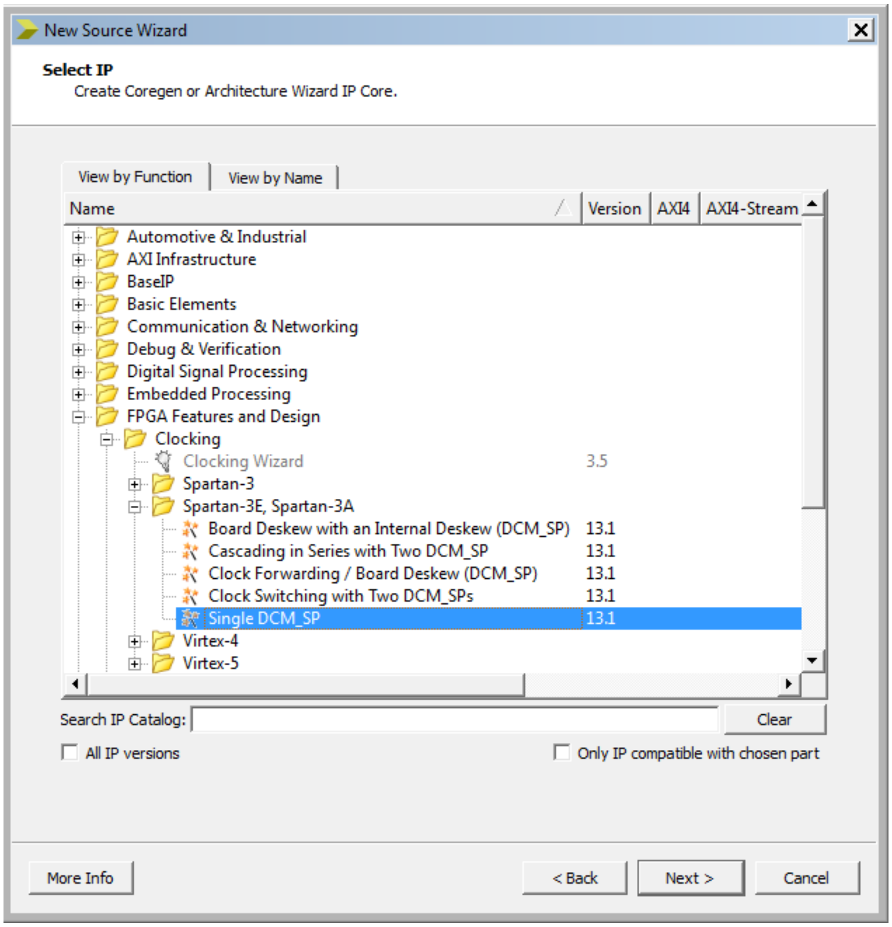
Select Source Type
Select source type, file name and its location.

File name: dcm_25

Location: C:\ECE3829\DCM\ipcore_dir

☑ Add to project

Select the Single DCM_SP core:



New Source Wizard

Select IP
Create Coregen or Architecture Wizard IP Core.

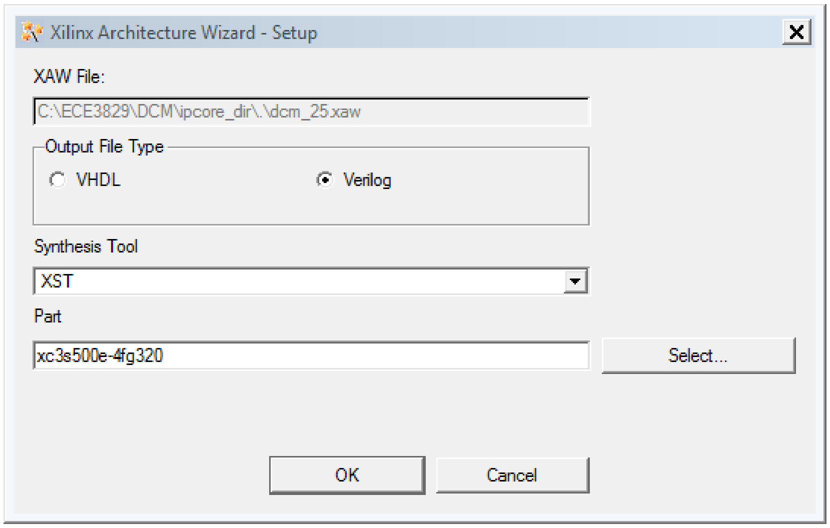
View by Function | View by Name

Name	Version	AXI4	AXI4-Stream
Automotive & Industrial			
AXI Infrastructure			
BaseIP			
Basic Elements			
Communication & Networking			
Debug & Verification			
Digital Signal Processing			
Embedded Processing			
FPGA Features and Design			
Clocking			
Clocking Wizard	3.5		
Spartan-3			
Spartan-3E, Spartan-3A			
Board Deskew with an Internal Deskew (DCM_SP)	13.1		
Cascading in Series with Two DCM_SP	13.1		
Clock Forwarding / Board Deskew (DCM_SP)	13.1		
Clock Switching with Two DCM_SPs	13.1		
Single DCM_SP	13.1		
Virtex-4			
Virtex-5			

Search IP Catalog:

☐ All IP versions ☐ Only IP compatible with chosen part

Click Next and then Finish.



Xilinx Architecture Wizard - Setup

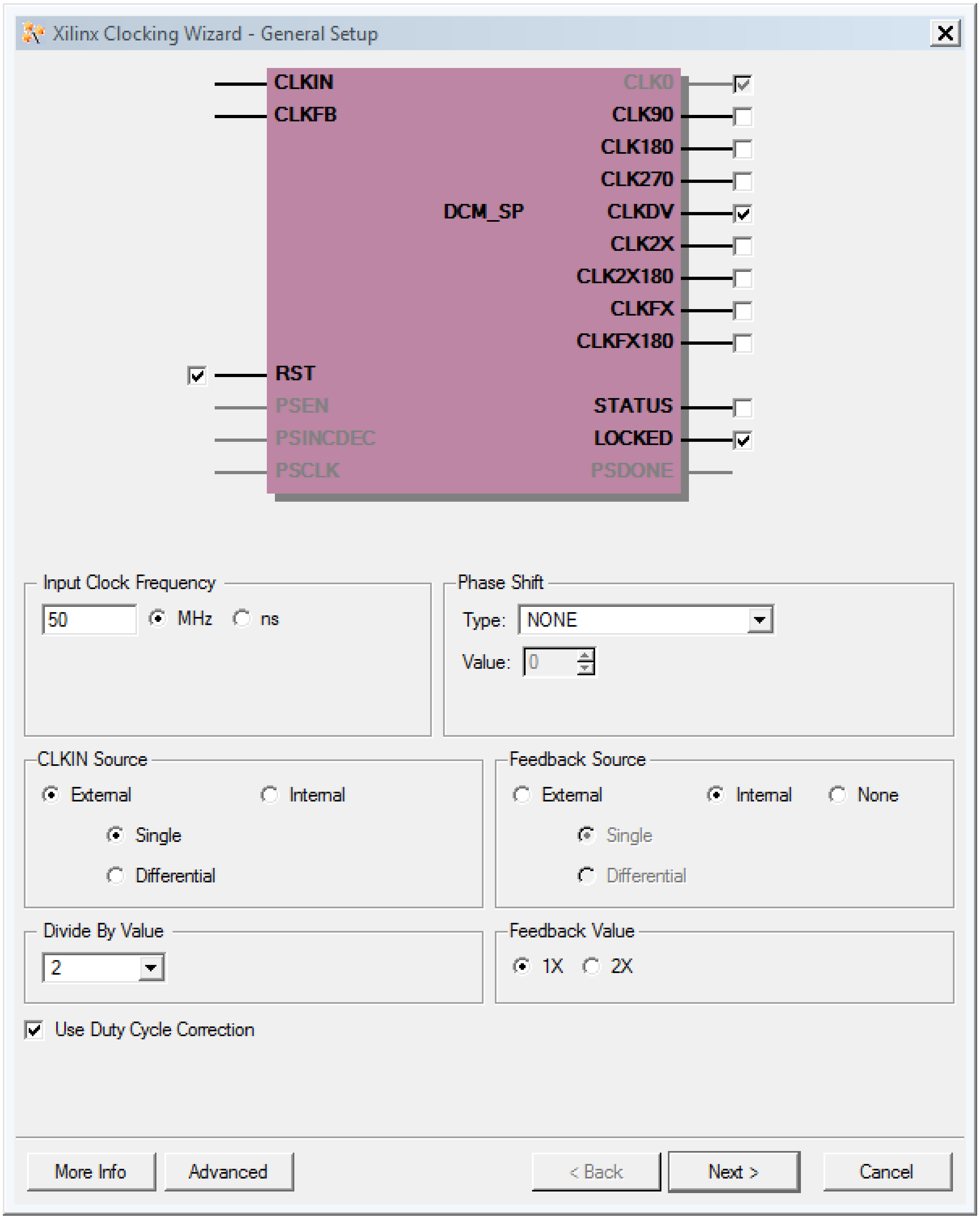
XAW File: C:\ECE3829\DCM\ipcore_dir\.\dcm_25.xaw

Output File Type
○ VHDL ● Verilog

Synthesis Tool: XST

Part: xc3s500e-4fg320

Click OK



Xilinx Clocking Wizard - General Setup

☑ CLK0
□ CLK90
□ CLK180
□ CLK270
☑ CLKDV
□ CLK2X
□ CLK2X180
□ CLKFX
□ CLKFX180
☑ RST
□ STATUS
☑ LOCKED

Input Clock Frequency: 50 ● MHz ○ ns

Phase Shift
Type: NONE
Value: 0

CLKIN Source
● External ○ Internal
● Single
○ Differential

Feedback Source
○ External ● Internal ○ None
● Single
○ Differential

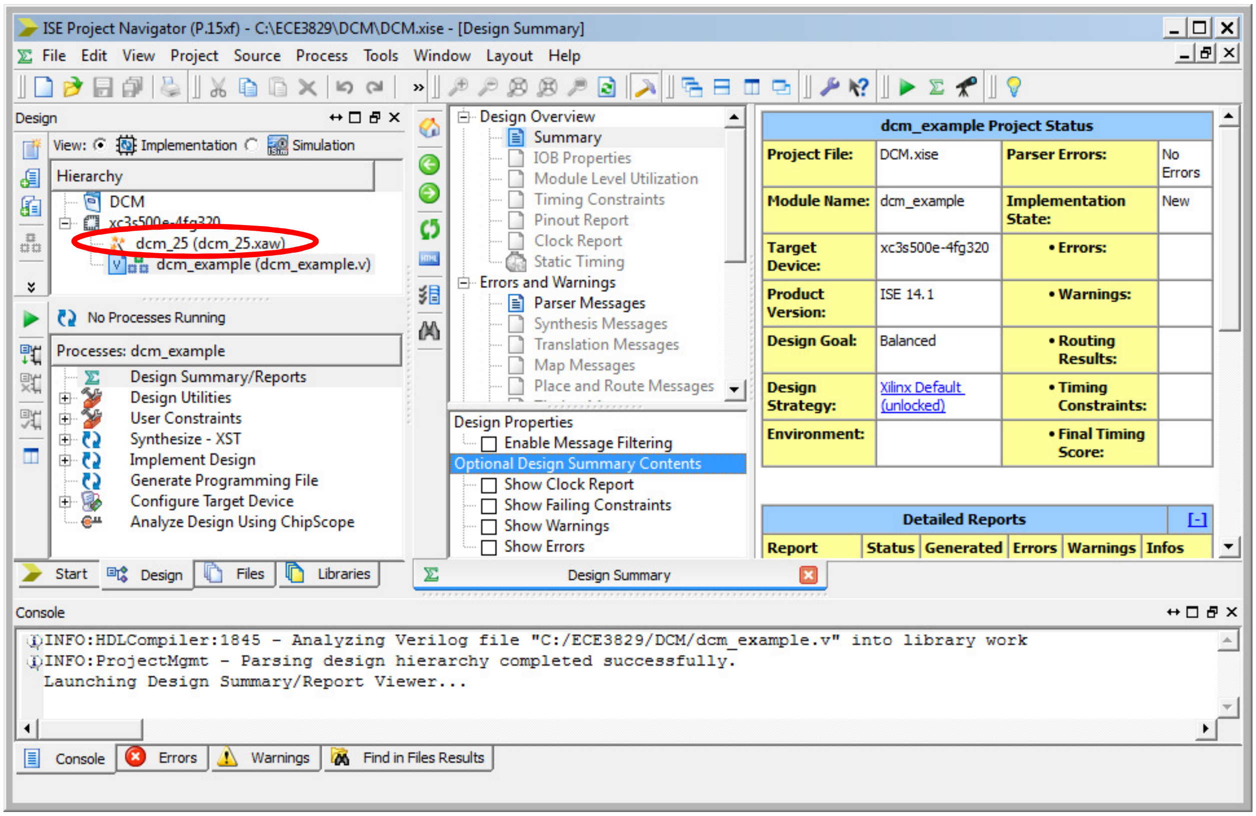
Divide By Value: 2

Feedback Value: ● 1X ○ 2X

☑ Use Duty Cycle Correction

Click the LOCKED, and CLKDV pin options and enter 50 for the Input Frequency and Select 2 for the Divide by Value

Click Next, Next, and Finish



ISE Project Navigator (P.15xf) - C:\ECE3829\DCM\DCM.xise - [Design Summary]

dcm_example Project Status			
Project File:	DCM.xise	**Parser Errors:**	No Errors
Module Name:	dcm_example	**Implementation State:**	New
Target Device:	xc3s500e-4fg320	• **Errors:**	
Product Version:	ISE 14.1	• **Warnings:**	
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:		• **Final Timing Score:**	

Detailed Reports [-]

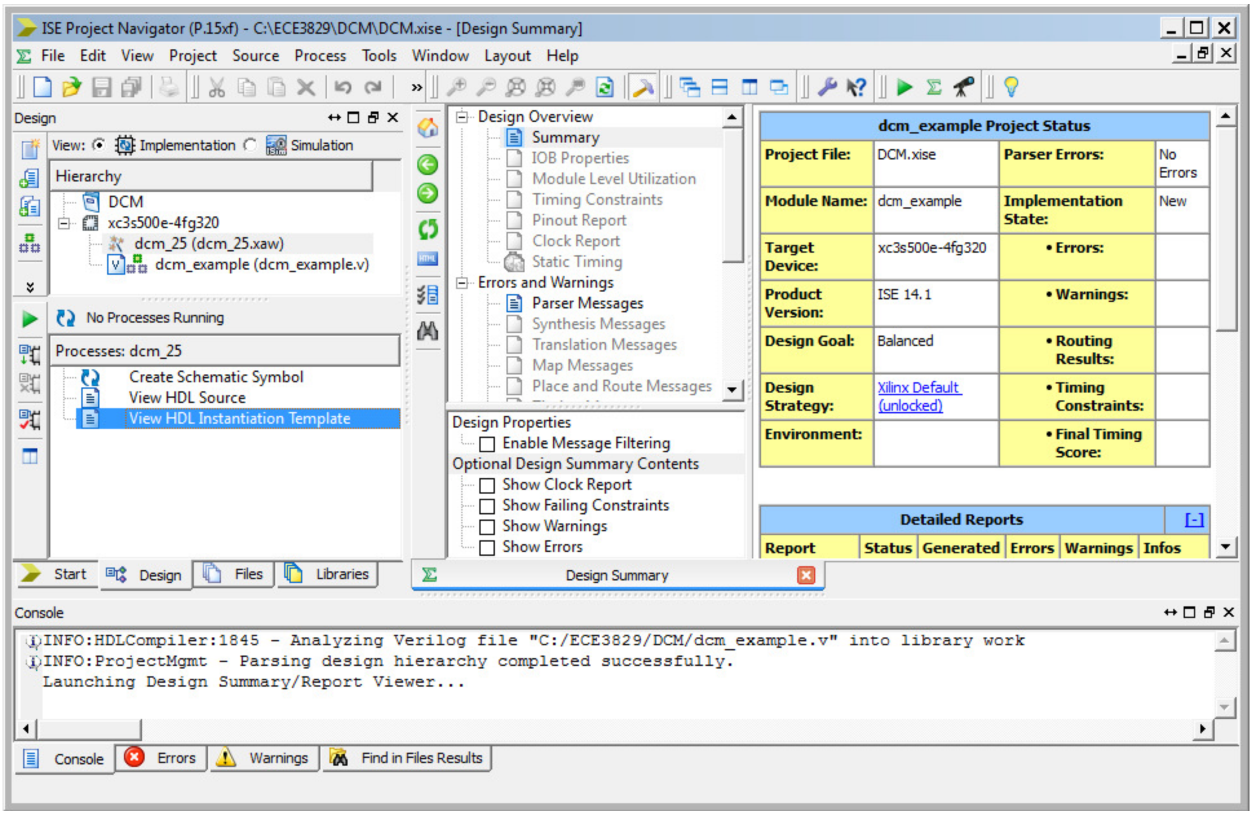
Report	Status	Generated	Errors	Warnings	Infos

```
INFO:HDLCompiler:1845 - Analyzing Verilog file "C:/ECE3829/DCM/dcm_example.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
```

You can now see the dcm_25 in the Design pane,

Select it and you will see some options in the Processes pane.

Select the View HDL Instantiation Template

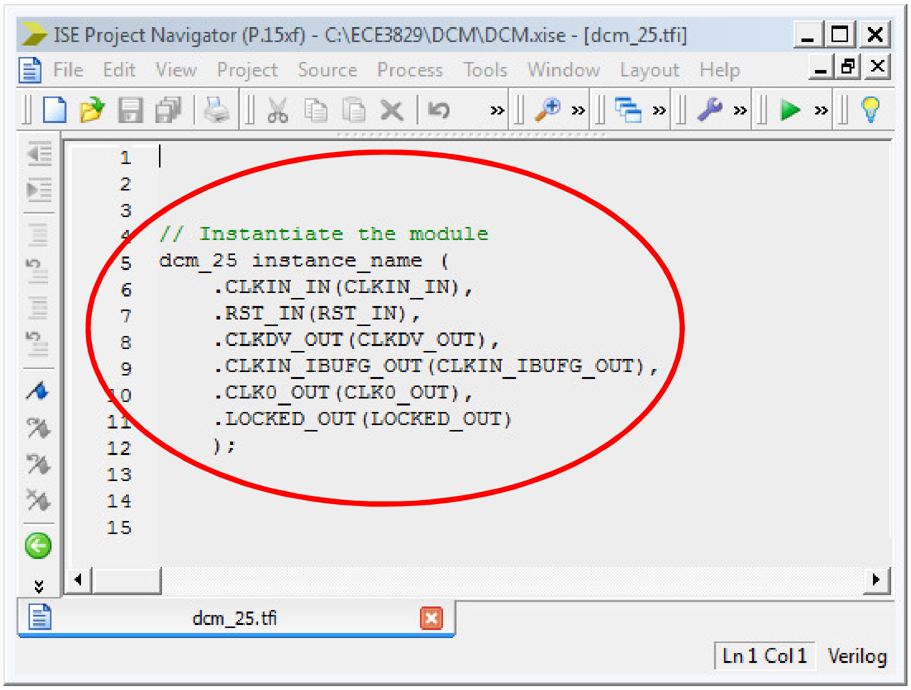


dcm_example Project Status			
Project File:	DCM.xise	**Parser Errors:**	No Errors
Module Name:	dcm_example	**Implementation State:**	New
Target Device:	xc3s500e-4fg320	**• Errors:**	
Product Version:	ISE 14.1	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:		**• Final Timing Score:**	

Detailed Reports					
Report	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**

```
INFO:HDLCompiler:1845 - Analyzing Verilog file "C:/ECE3829/DCM/dcm_example.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Launching Design Summary/Report Viewer...
```

Double –click the *View HDL Instantiation Template* process:

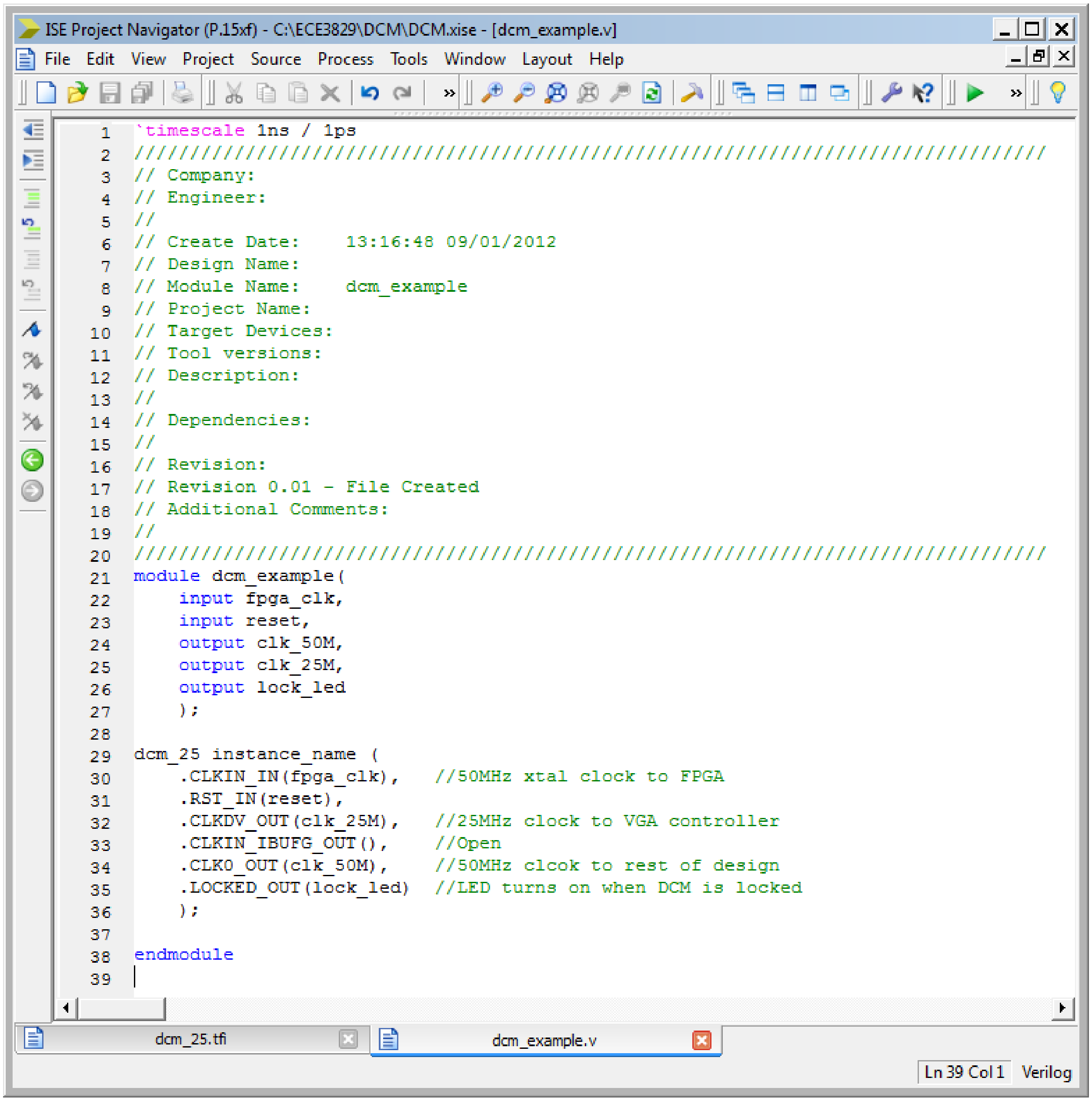

ISE Project Navigator (P.15xf) - C:\ECE3829\DCM\DCM.xise - [dcm_25.tfi]
File Edit View Project Source Process Tools Window Layout Help
dcm_25.tfi
Ln 1 Col 1
Verilog

```



// Instantiate the module
dcm_25 instance_name (
    .CLKIN_IN(CLKIN_IN),
    .RST_IN(RST_IN),
    .CLKDV_OUT(CLKDV_OUT),
    .CLKIN_IBUFG_OUT(CLKIN_IBUFG_OUT),
    .CLK0_OUT(CLK0_OUT),
    .LOCKED_OUT(LOCKED_OUT)
    );
```

Copy and Paste the DCM instantiation templates to your original Verilog:


ISE Project Navigator (P.15xf) - C:\ECE3829\DCM\DCM.xise - [dcm_example.v]
File Edit View Project Source Process Tools Window Layout Help
dcm_25.tfi
dcm_example.v
Ln 39 Col 1
Verilog

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:16:48 09/01/2012
// Design Name:
// Module Name:    dcm_example
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//////////////////////////////////////////////////////////////////////////////////
module dcm_example(
    input fpga_clk,
    input reset,
    output clk_50M,
    output clk_25M,
    output lock_led
    );

dcm_25 instance_name (
    .CLKIN_IN(fpga_clk),   //50MHz xtal clock to FPGA
    .RST_IN(reset),
    .CLKDV_OUT(clk_25M),   //25MHz clock to VGA controller
    .CLKIN_IBUFG_OUT(),    //Open
    .CLK0_OUT(clk_50M),    //50MHz clcok to rest of design
    .LOCKED_OUT(lock_led)  //LED turns on when DCM is locked
    );

endmodule
```
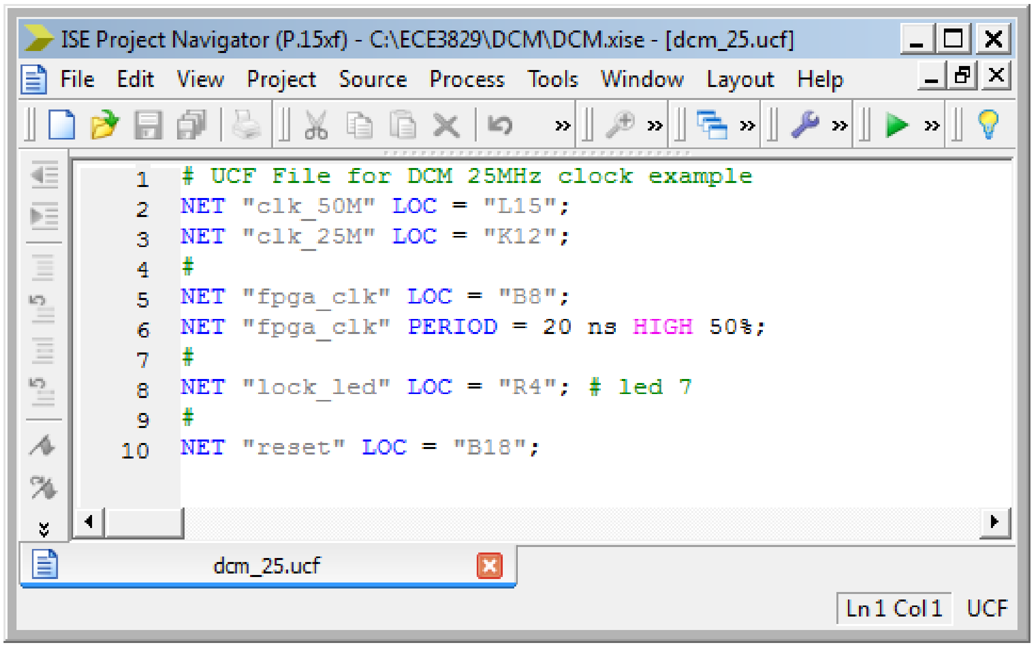
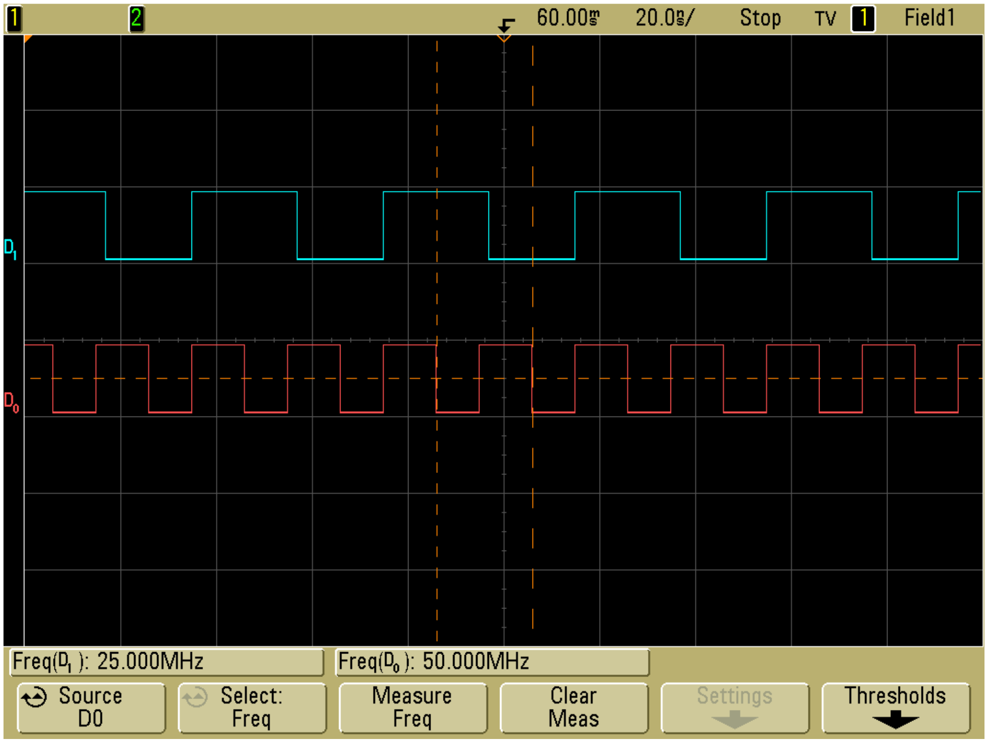

Create a UCF File (clk_50MHz is connected to debug port JA1, and Clk_25M to JA2):


ISE Project Navigator (P.15xf) - C:\ECE3829\DCM\DCM.xise - [dcm_25.ucf]
File Edit View Project Source Process Tools Window Layout Help
dcm_25.ucf
Ln 1 Col 1 UCF

```
# UCF File for DCM 25MHz clock example
NET "clk_50M" LOC = "L15";
NET "clk_25M" LOC = "K12";
#
NET "fpga_clk" LOC = "B8";
NET "fpga_clk" PERIOD = 20 ns HIGH 50%;
#
NET "lock_led" LOC = "R4"; # led 7
#
NET "reset" LOC = "B18";
```

Synthesize, Implement, and Generate a Programming File,

Using an oscilloscope confirm that JA1 has a 50MHz clock and JA2 has a 25MHz clock and the LED 7 is on indicating the DCM is locked.

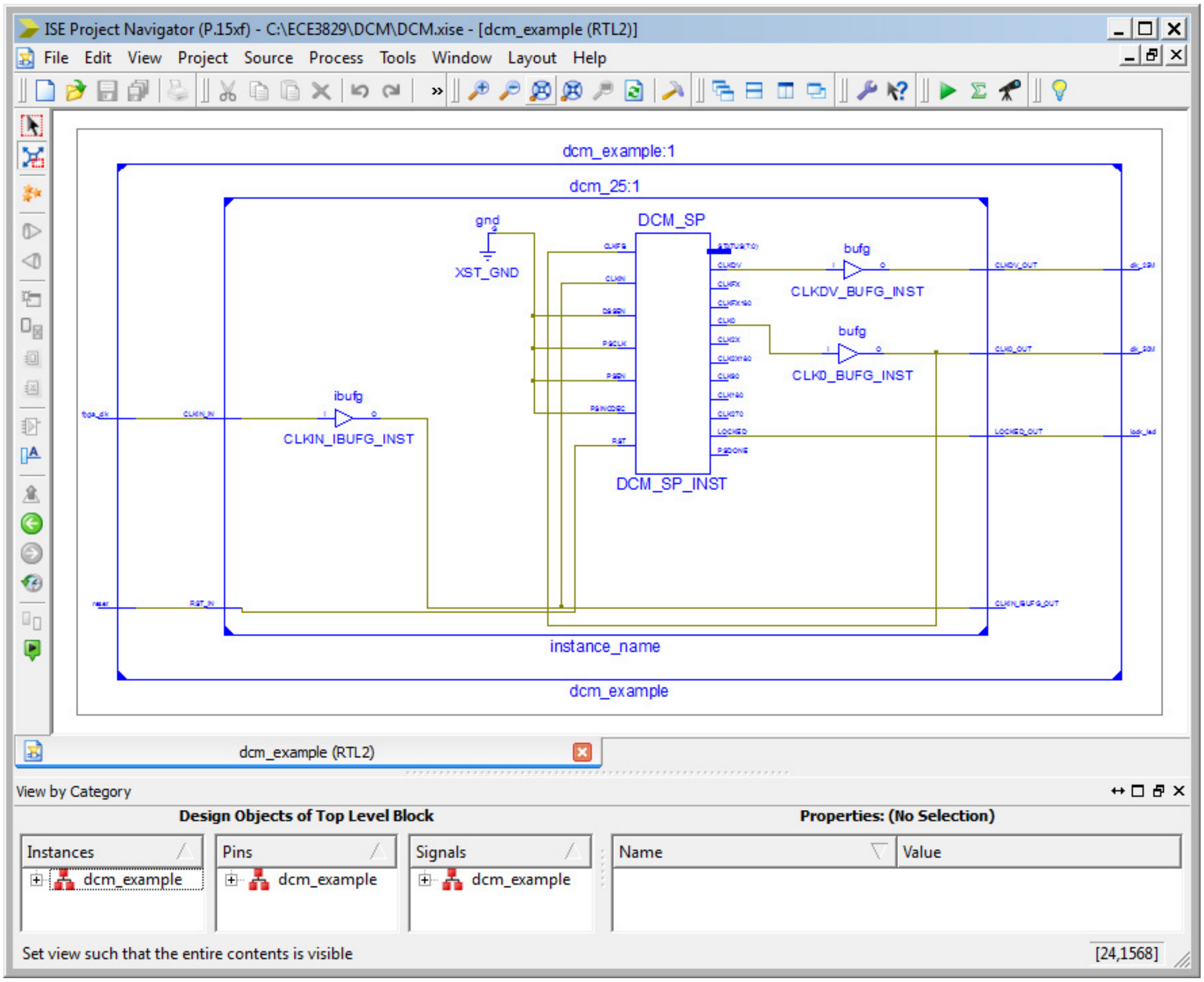


Freq(D_1): 25.000MHz

Freq(D_0): 50.000MHz

Press BTN0 to try reset the DCM and confirming the DCM locks again and the clock signals are correct.

Here is a schematic of what we have created:



Set view such that the entire contents is visible [24,1568]