Simple Circuits for Generating High-Voltage Staircase Waveforms

John A. McNeill

Abstract—**Two novel circuits are described which provide simple generation of high-voltage staircase waveforms for driving electro-optical (EO) loads. The circuits use power MOSFET's in what is essentially a switching mode. For applications which require high-voltage step-type waveforms, this technique offers substantial power savings and improved time-domain response over drive circuits that use a linear amplifier approach. Waveform characteristics can be controlled at a low voltage point, allowing flexible and accurate operation.**

I. Introduction

THE need for wideband, high-voltage drive signals is encountered in various instrumentation applications, for example in electro-optical (EO) systems [1], [2]. Theophanous *et al.* [3] describe the general problem: a typical EO load can be modeled as a lumped capacitance of order 100 pF, and requires a drive voltage in the kilovolt range.

A subclass of the general problem is found in step-type or staircase waveforms, which are required in applied physics [4] on optical interferometry [5] applications. Fig. 1 shows a typical "staircase" waveform, with uniform voltage steps of ΔV, up to a maximum of V_{MAX}, then returning to zero. The period of the waveform T is of order 100 μs to 1 ms.

Previous approaches to the general design problem have been primarily linear amplifier techniques [3], [4], which require a large bandwidth and high slew rate to accurately process the fast edges of step waveforms. With the high supply voltage required for the large output voltage swing, biasing active devices in the linear region for large bandwidth also raises the quiescent power consumption to undesirable levels, in the tens of watts [3].

The circuits described in this paper are optimized for generating step waveforms. The design goals are to minimize power required from the high-voltage supply and to provide control of output characteristics from a low-voltage point. The resulting circuits feature low power consumption and decoupling of time-domain performance from quiescent power consumption. Control of the output from a low-voltage point allows improved accuracy as well as simple generation of steps which are nonuniform in voltage or time.

Manuscript received October 13, 1992; revised May 4, 1993.
J. McNeill is with Boston University, Boston, MA 02215.
IEEE Log Number 9211712.

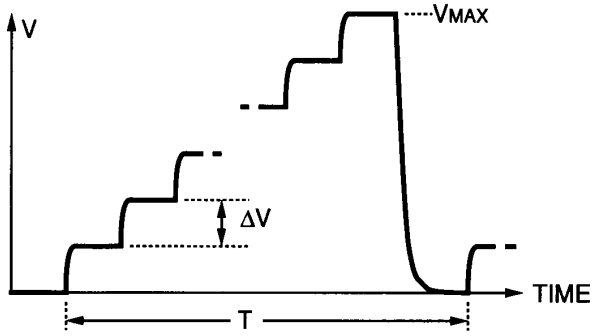


Fig. 1. Typical "staircase" waveform.

II. Basic Circuit

The "voltage doubler" is a familiar circuit [6] which used diodes and capacitors to approximately double the maximum voltage swing available in a circuit. The "doubling" concept has been extended to achieve higher order voltage multiplication for high-voltage systems [7], and the related charge pump is used to realize moderate voltage multiplication in low-voltage systems [8].

The first of the two novel circuits to apply these general concepts for generating a staircase waveform will be referred to as the "basic circuit," shown in Fig. 2. The input V_{in} is a pulse waveform, with amplitude approximately equal to the size of the desired output step. On the rising edge of V_{in}, D_1 is forward biased, and the rising edge is passed to V_{out} translated by V_{C1}, the voltage on the level-shifting capactior C_1. On the falling edge of V_{in}, enhancement mode MOSFET M_1 conducts and charges C_1, thereby achieving progressively higher voltages in time at V_1 and V_{out}.

A. Output Step Size

For a first-order analysis, we will assume an input square wave amplitude of ΔV_{in}, diode forward voltage of V_{D1}, MOSFET threshold voltage of V_{TH1}, and M_1 and D_1 stray capacitances negligible. Referring to the timing diagram of Fig. 3, circuit operation is as follows:

The RESET switch M_3 is held closed until time t_0. C_{LOAD} discharges and V_{OUT} falls to 0 V; C_1 discharges through D_1, and V_1 falls to $+V_{D1}$, one diode drop above ground. At t_1, V_{in} goes negative, and C_1 pulls V_1 more than a threshold voltage below V_{out}. M_1 conducts and C_1 charges until $V_1 = -V_{TH1}$.

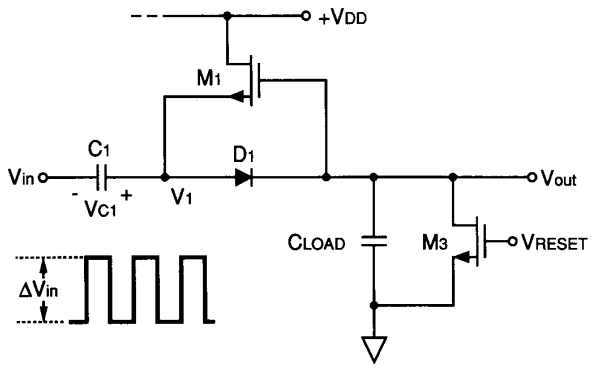


Fig. 2. Basic circuit, simplified schematic.

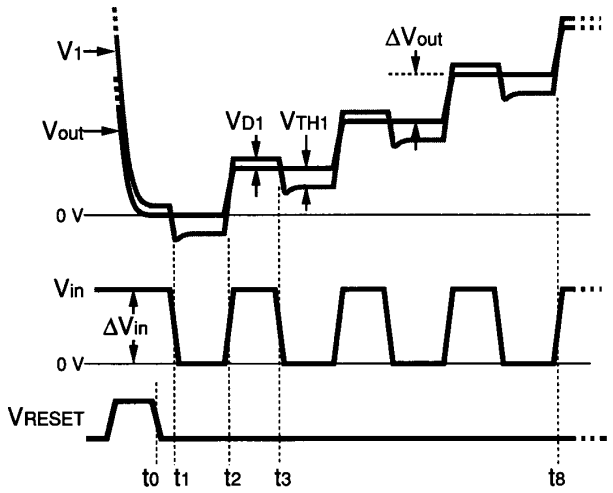


Fig. 3. Basic circuit timing waveforms.

At t_2, V_{in} goes positive. By voltage division (and since division of ΔV_{in} across C_1 and C_{LOAD} does not begin until D_1 is forward biased), V_1 increases by

$$\Delta V_1 = \frac{C_1}{C_1 + C_{LOAD}} \Delta V_{in} + \frac{C_{LOAD}}{C_1 + C_{LOAD}} (V_{D1} + V_{TH1}). \quad (1)$$

V_{out} will be one diode drop below V_1; therefore the first output voltage step will be

$$V_{out} = -V_{TH1} + \Delta V_1 - V_{D1}. \quad (2)$$

At time t_3, the falling edge of V_{in} pulls V_1 low; C_1 charges up until $V_1 = V_{out} - V_{TH1}$. Combining (1) and (2), we find that the output voltage increases in uniform steps of amplitude

$$\Delta V_{out} = \frac{C_1}{C_1 + C_{LOAD}} [\Delta V_{in} - (V_{TH1} + V_{D1})]. \quad (3)$$

The output will increase on each rising edge of V_{in}, with a limit of $+V_{DD}$ when the MOSFET runs out of headroom. Note that the charge for the level-shifting capacitor C_1 comes from V_{DD} through M_1. No charge is required from C_{LOAD}, so that V_{out} remains constant until the next step. When the staircase sequence is complete, the V_{RESET} signal goes high, discharging C_{LOAD} and C_1.

B. Dynamic Performance

To first order, the rise time of V_{out} is determined by either the rise time of the V_{in} voltage source driving C_{LOAD}, or the time constant of the incremental forward resistance r_{D1} of D_1 and the load capacitance. Since $r_{D1} \cdot C_{LOAD}$ may be ≈ 10 ns, V_{in} will usually determine rising-edge performance. For the fall time, V_{out} will combine slewing due to current limiting in M_3, followed by exponential settling governed by the "on" resistance r_{on3} of M_3 and C_{LOAD}.

The rise and fall times can be increased by inserting resistors in series with D_1 and M_3, respectively. The amplitude of V_{RESET} will affect the maximum current in M_3, thereby affecting the fall time. Note that the time-domain performance depends only on switching parameters, and does not require a large quiescent current.

C. Power Consumption from High-Voltage Supply

In the basic circuit, C_{LOAD} is charged by the square wave signal source. The high-voltage supply V_{DD} charges C_1 through M_1, which requires an average current from V_{DD} of

$$I_{supply} = \frac{\Delta Q}{\Delta T} = \frac{1}{T} C_1 V_{MAX}. \quad (4)$$

The average power consumption from the high-voltage supply is

$$P_{supply} = \frac{1}{T} C_1 V_{MAX} V_{DD}. \quad (5)$$

For typical values of $C_1 = 1000$ pF, $V_{MAX} = V_{DD} = 1$ kV, and $T = 1$ ms, (5) gives a power consumption of 1 W, much lower than for a linear circuit with similar time-domain performance [3].

D. Second-Order Effects: Droop

There will be some decay of V_{out} when V_{in} is low, due to the leakage current of M_3 and D_1 and any resistance associated with C_{LOAD}. Increasing the duty cycle of V_{in} and adding capacitance in parallel with C_{LOAD} are two possible methods of reducing droop.

III. Modification of Basic Circuit: Symmetric Circuit

There are two characteristics of the basic circuit that may be disadvantageous in some applications:

1) ΔV_{out} is directly dependent on C_1 and C_{LOAD}, requiring that C_1 be much greater than C_{LOAD}, and
2) the square wave source V_{in} is also used to charge C_{LOAD}.

To eliminate these characteristics we generalize the concept of the basic circuit by using a MOSFET to unload the square wave source. This circuit will be referred to as the "symmetric circuit," and is shown in Fig. 4. MOSFET M_2 has been added to charge C_{LOAD} on the rising edge of V_{in}, so that C_1 need not be much greater than C_{LOAD}. M_4 must also be added so there is a discharge path for C_1 when M_3 is conducting.

A. Step Size

Fig. 5 shows the timing waveforms for the symmetric circuit. The analysis will include the MOSFET stray capacitances, which now may be significant compared to C_1 and C_{LOAD}. The simplest MOSFET capacitance model [9] was used, where C_{gs}, C_{gd}, and C_{ds} represent the gate-source, gate-drain, and drain-source capacitances respectively. Although MOSFET capacitances are strongly dependent on operating point [10], [11], the model allows simple calculations and gives good agreement with experimental data. Applying the model to the circuit of Fig. 4 gives an equivalent circuit with

$$C_1' = C_1 + C_{gd2} + C_{ds1} + C_{ds4} + C_{gd4} \quad (6)$$

$$C_G' = C_{gs1} + C_{gs2} \quad (7)$$

$$C_{LOAD}' = C_{LOAD} + C_{gd1} + C_{ds2} + C_{ds3} + C_{gd3} \quad (8)$$

where C_G' models the gate capacitances, and appears between the gates of M_1 and M_2. C_1' and C_{LOAD}' are capacitances C_1 and C_{LOAD} in parallel with the MOS strays.

There are three major ways in which the stray capacitances will reduce the output voltage step amplitude:

1) attenuation of ΔV_{in} by the capacitive voltage divider formed by C_1 and the capacitance on the gate of M_2,
2) voltage drop across C_1 to supply charge to gate capacitances C_{gs1} and C_{gs2}, and
3) coupling of the falling edge of V_{in} to V_{out} through C_{gs1} and C_{gs2}.

Including all of these effects in the analysis of the circuit model gives for ΔV_{out}:

$$\Delta V_{out} = \Delta V_{in}\left(\frac{C_1}{C_1'}\right) - (V_{TH1} + V_{TH2}) \cdot \left(1 + \frac{C_G'}{C_1'} + \frac{C_G'}{C_{LOAD}'}\right) \quad (9)$$

where the ΔV_{in} term accounts for effect (1), and the $(V_{TH1} + V_{TH2})$ term accounts for effects (2) and (3). From (9) we see that ΔV_{out} is somewhat dependent on C_{LOAD}. However, the dependence is not as strong as that of (3) for the simple circuit, since in (9) the term in C_{LOAD} multiplies only $(V_{TH1} + V_{TH2})$, and not ΔV_{in}.

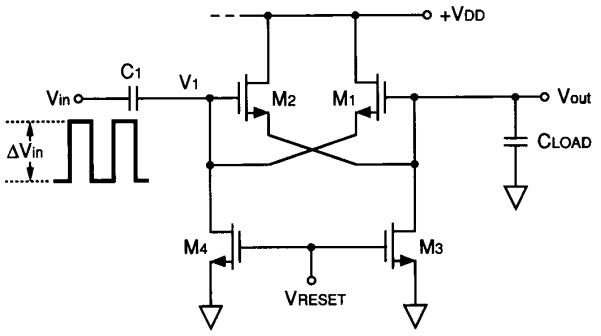


Fig. 4. Symmetric circuit, simplified schematic.

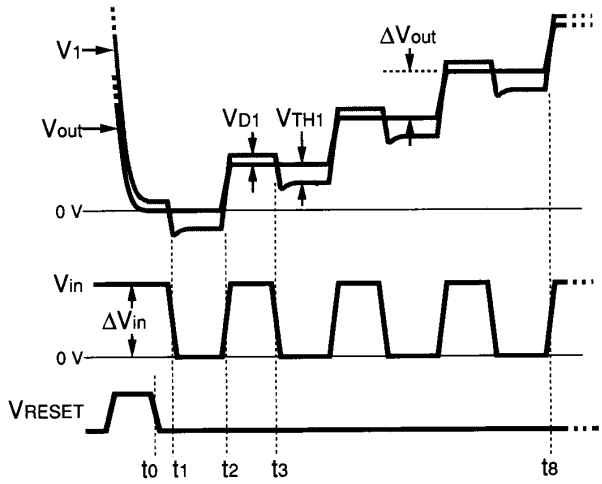


Fig. 5. Symmetric circuit timing waveforms.

B. Dynamic Performance

The rise time of V_{out} is determined by the rise time of V_{in} and the ability of M_2 to charge C_{LOAD}. On the rising edge of V_{in}, M_2 acts as a source follower driving C_{LOAD}. In practice, current limiting in M_2 leads to a slewing characteristic.

For the fall time of V_{out}, the analysis of Section II for the simple circuit applies. As in Section II, rise and fall times can be tailored by inserting resistors in series with M_2 and M_3, respectively.

C. Power Consumption

In this case the high-voltage supply V_{DD} charges both C_1 and C_{LOAD}. Analysis including the stray capacitances gives

$$I_{supply} = \frac{1}{T}(C_1' + C_{LOAD}' + C_G')\, V_{MAX} \quad (10)$$

$$P_{supply} = \frac{1}{T}(C_1' + C_{LOAD}' + C_G')\, V_{MAX} V_{DD}. \quad (11)$$

For a given C_{LOAD}, the power consumption for the symmetric circuit will be lower than that given by (5) for the basic circuit, because C_1 is no longer required to be much greater than C_{LOAD}.

IV. Experimental Results and Discussion

The circuit built as proof of concept used a 150 V power supply for V_{DD} and 200 V breakdown MOSFET's. The same approach can be used for higher breakdown voltage transistors; devices rated up to 1 kV are available [11]. All voltage readings were taken from a Tektronix model 11301 oscilloscope. The current measurements were made with a 3 1/2 digit DVM in series with the high-voltage supply. The MOSFET V_{TH}s were measured at $I_D = 1\ \mu A$.

A. Step Size: Basic Circuit

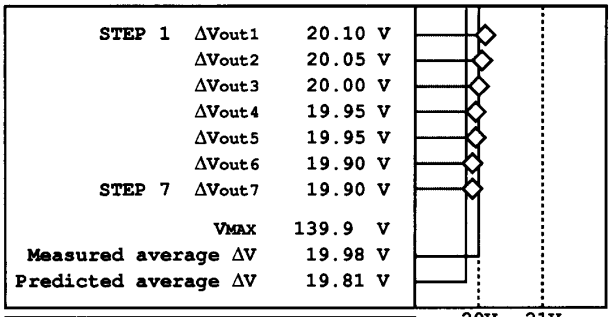
The basic circuit was built as shown in Fig. 2, with the addition of resistors $R_{G1} = 470\ \Omega$ (in series with gate of M_1, added to damp out transients) and $R_{D3} = 22\ \Omega$ (in drain of M_3, to limit current when discharging C_1 and C_{LOAD}). M_1 and M_3 were Zetex BS107P N-channel MOSFETs [12]. D_1 was a switching-type diode with low capacitance. ($V_{TH1} + V_{D1}$) was measured to be 1.51 V.

Table I gives the basic circuit test parameters, measured amplitudes of the output voltage steps ΔV_{out1} through ΔV_{out7}, the maximum voltage V_{MAX}, the average step size, and the measured current drawn from the high-voltage supply. Also given in Table I are values predicted by (3) and (4) for ΔV_{out} and I_{supply}.

The results show a step-size nonuniformity (difference between largest and smallest step) of 1.0% of the average step size. The average step differed from the predicted step by 0.17 V (0.9% of average step). This error is well within the measurement error of the oscilloscope, and shows good agreement with (3).

TABLE I
Basic Circuit Test Results

ΔVin = 23.30 V		C1 = 0.01μF
T = 180μs		CLOAD = 1000pF
STEP 1	ΔVout1	20.10 V
	ΔVout2	20.05 V
	ΔVout3	20.00 V
	ΔVout4	19.95 V
	ΔVout5	19.95 V
	ΔVout6	19.90 V
STEP 7	ΔVout7	19.90 V
	VMAX	139.9 V
Measured average ΔV		19.98 V
Predicted average ΔV		19.81 V
Measured Isupply		8.66 mA
Predicted Isupply		7.78 mA



B. Step Size: Symmetric Circuit

Figure 6 shows the schematic of the symmetric circuit as built. R_{G1} and R_{G2} were added to damp out transients that occurred for some V_{in} transitions; R_{D3} and R_{D4} were added to limit current when discharging C_1 and C_{LOAD}. M_4 was returned to -2 V so that R_{D4} draws a small current during the RESET interval, causing M_1 to conduct. Then V_1 is initialized to $-V_{TH1}$, so that the first step is the same size as the following steps.

Two versions of the symmetric circuit were tested, one emphasizing high speed and the other a heavy capacitive load. Tables II and III give the test parameters, results, and predictions from equations (9) and (10) for ΔV_{out} and I_{supply}. The effective values for the BS107P MOSFET capacitances (including measured strays from the circuit wire runs) were $C_{gd} = 4$ pF, $C_{gs} = 56$ pF, and $C_{ds} = 4$ pF [12]. ($V_{TH1} + V_{TH2}$) was measured to be 1.72 V.

In the high-speed tests, the step-size nonuniformity was 0.5 V (2.5% of avg. step), and the average step differed from the predicted value by 0.65 V (3.3% of avg. step). In taking the data for Table II, it was observed that the size of the output step depended on the rise time t_R of the input signal V_{in}. For $t_R > 200$ ns, output step size was constant, but as t_R decreased the output step size increased. For $t_R = 10$ ns, the output step size increased by about 2.2 V. As t_R decreased, the step size was also more nonuniform and deviated more from the predicted value. The dependence on t_R is probably due to the time- and voltage-dependent nature of the MOS capacitances, since there was no dependence on rise time observed in taking the data for Table III, where C_1 and C_{LOAD} were much larger. Fig. 7(a) is an oscilloscope photo of V_{in} and V_{out} for the high-speed test driving a waveform of eight steps equally spaced at 20 V, for a maximum voltage of 140 V.

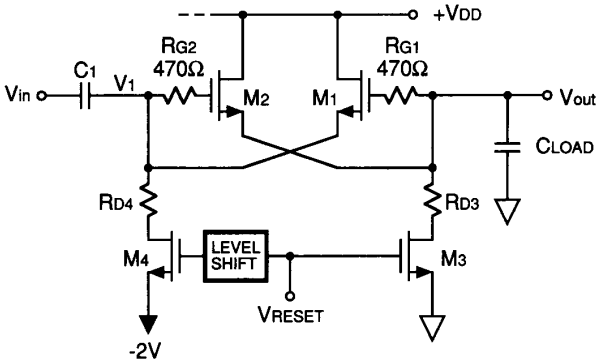


Fig. 6. Symmetric circuit as built.

In the heavy capacitive load test, the nonuniformity was improved, and the measured step sizes agree with the prediction of (9) to within a few percent.

C. Power Consumption

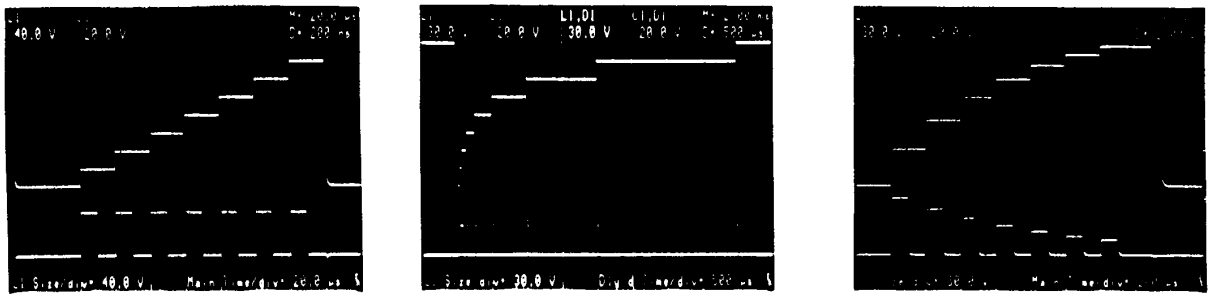
In all cases, the measured supply current exceeded the predicted value by about 10%. In the symmetric circuit,

TABLE II
SYMMETRIC CIRCUIT TEST RESULTS (HIGH SPEED)

ΔVin = 21.50 V		C1 = 225pF		RD3 = 220Ω
T = 1.8ms		CLOAD = 2144pF		RD4 = 2.2kΩ
STEP 1	ΔVout1	19.7 V		
	ΔVout2	20.0 V		
	ΔVout3	20.1 V		
	ΔVout4	20.1 V		
	ΔVout5	20.1 V		
	ΔVout6	20.0 V		
STEP 7	ΔVout7	19.6 V		
	VMAX	139.6 V		
Measured average ΔV		19.94 V		
Predicted average ΔV		20.59 V		
Measured Isupply		2.12 mA		
Predicted Isupply		1.95 mA		

TABLE III
SYMMETRIC CIRCUIT TEST RESULTS (LARGE C_{LOAD})

ΔVin = 21.50 V		C1 = 0.01μF		RD3 = 22Ω
T = 1.8ms		CLOAD = 0.1μF		RD4 = 470Ω
STEP 1	ΔVout1	20.10 V		
	ΔVout2	20.10 V		
	ΔVout3	20.00 V		
	ΔVout4	20.00 V		
	ΔVout5	19.95 V		
	ΔVout6	19.95 V		
STEP 7	ΔVout7	19.95 V		
	VMAX	140.1 V		
Measured average ΔV		20.01 V		
Predicted average ΔV		19.72 V		
Measured Isupply		9.66 mA		
Predicted Isupply		8.56 mA		



a) High speed test, Vout at 40V/div.

b) Log characteristic by varying Vin timing; Vout at 30V/div.

c) Log characteristic by varying Vin amplitude; Vout at 30V/div.

Fig. 7. Oscilloscope photos, symmetric circuit. Upper trace: V_{out}. Lower trace: V_{in} at 20 V/div.

at least part of the excess power consumption can be attributed to excess current drawn during the RESET interval. From Fig. 4, it can be seen that if C_1 and C_{LOAD} discharge at different rates, a large positive V_{GS} will develop across either M_1 or M_2, drawing a large current from V_{DD}. It was observed experimentally that equalizing the $(R_{D3} + r_{on3}) \cdot C_{LOAD}$ and $(R_{D4} + r_{on4}) \cdot C_1$ time constants minimized the excess power consumption.

D. Tailoring Output Waveforms

Tailoring of the output waveform can be achieved through a change in timing or input step size. Figs. 7(b) and 7(c) show approximations to a logarithmic characteristic by varying the input signal timing and step size respectively.

E. Step Amplitude Temperature Dependence

For both circuits, the temperature dependence of V_D and V_{TH} will cause the output step amplitude ΔV_{out} to vary with the temperature of the active devices M_1 and D_1 (basic circuit) or M_1 and M_2 (symmetric). The temperature coefficient of V_D is approximately -2.1 mV/°C; for MOSFET's the V_{TH} variation can range from -2 to -5 mV/°C [6]. The result will be a temperature coefficient for ΔV_{out} of order $+5$–$+10$ mV/°C. For moderate temperature excursions this error will be less than the step-size nonuniformities measured in Tables I–III. From (3) and (9) we see that first-order temperature compensation can be achieved by including in the input step amplitude ΔV_{in} an appropriate amount of V_D and/or V_{TH} from a device at the same temperature as the active devices.

F. Additional Modifications

If more precise step sizes are required for repetitive waveforms, it is possible to improve accuracy by sampling the output and applying some form of feedback [13]. Modifying the output step size is simple since the input step size can be controlled at V_{in}.

The observed droop was consistent with the resistive load of the 10 MΩ oscilloscope probe. Increasing the duty cycle of V_{in} as a method of reducing droop was experimentally verified. One potential disadvantage of the circuits described here is that the output cannot drive a resistive load. By adding a source follower to buffer the output, it should be possible to drive a moderate load without droop.

V. Conclusion

Two circuits have been described which provide a simple means for generation of a high-voltage step waveform. Low-power operation while driving significant capacitive loads at high speeds has been demonstrated. The output step size and supply current performance can be predicted to within a few percent using equations derived from a simple model of MOS stray capacitances. Tailoring of high-voltage output waveforms by control of the lower voltage input signal has been demonstrated.

Acknowledgment

The author thanks Prof. Anton Mavretic and Prof. Emile Gergin, both of Boston University, for their discussions and support.

References

[1] I. P. Kaminow and E. H. Turner, "Electrooptic light modulators," *Proc. IEEE*, vol. 54, pp. 1374–1390, 1966.
[2] I. P. Kaminow, *An Introduction to Electrooptic Devices*. New York: Academic, 1974.
[3] N. Theophanous *et al.*, "A high-voltage electrooptic drive amplifier using a power MOSFET pair," *IEEE Trans. Instrum. Meas.*, vol. 37, pp. 49–52, Mar. 1988.
[4] P. A. Ekstrom *et al.*, "High-voltage linear pulse amplifier," *Rev. Sci. Instr.*, vol. 51, pp. 1700–1703, Dec. 1980.
[5] R. K. Tyson, *Principles of Adaptive Optics*. Boston, MA: Harcourt Brace Jovanovich, 1991, pp. 143–145.
[6] P. Horowitz and W. Hill, *The Art of Electronics*. New York: Cambridge Univ. Press, 1980.
[7] Voltage Multipliers, Inc., *Power Semiconductor Short Form Catalog 1989–90*, p. 2, 1989.
[8] Maxim Integrated Products, *1992 New Releases Data Book*, Section 4, 1992.
[9] Supertex Inc., *Databook 1988–89*, p. 3–4, 1988.
[10] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. Fort Worth, TX: Holt, Rinehart and Winston, 1987.
[11] International Rectifier Corp., *HEXFET Power MOSFET Designer's Manual*, 1987.
[12] Zetex Inc., *Technical Handbook MOSFETs*, 1991.
[13] P. T. Krein *et al.*, "An improved high-voltage waveform generator," *J. Phys. E: Sci. Instrum.*, vol. 16, pp. 1234–1237, Dec. 1983.