A SIMPLE METHOD FOR RELATING TIME- AND FREQUENCY-DOMAIN MEASURES OF OSCILLATOR PERFORMANCE

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ABSTRACT

This paper presents a simple technique for linking time domain (jitter) and frequency domain (phase noise) measures of oscillator performance. The key concept is the definition of a single figure-of-merit in the time- or frequency-domain that relates system-level performance (such as jitter or phase noise) to circuit-level parameters (such as power dissipation and signal amplitude). This technique is particularly applicable to circuit- and system-level design of voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs). The technique allows VCO and PLL design and characterization to take place in the domain (time or frequency, PLL open-loop or closed-loop) that provides the most insight into sources of jitter, while allowing a direct link to system-level performance as measured in any other domain. The methodology also speeds simulation since only the open loop VCO need be simulated, which allows a substantial savings in simulation time. Design examples and experimental results are presented for existing PLLs showing good agreement to the theoretical predictions.

I. INTRODUCTION

In a phase-locked loop (PLL), phase noise of the voltage controlled oscillator (VCO) often determines the limits of system performance in the time domain (jitter) or frequency domain (phase noise). There have recently been many studies in the literature [1-10] on the subject of phase noise in oscillators. Taken together, these studies are seen to have addressed a wide diversity of material in the field, ranging from general high-level tutorials to detailed analysis of noise mechanisms in specific oscillator architectures.

This paper presents a simple technique for linking time domain (jitter) and frequency domain (phase noise) measures of oscillator performance at the system level. The technique applies for any oscillator dominated by $1/f^2$ phase noise. Section I.A of this paper reviews concepts of phase noise for VCOs. Section I.B reviews the effect on VCO phase noise of closed loop PLL operation. Section I.C describes phase noise measurements and defines the frequency domain figure-of-merit N_1. Section I.D describes jitter measurements and defines the time domain figure-of-merit κ. Section II covers the development of the mathematical relationships among the time and frequency domain measurements. Section III covers design examples and experimental verification.

A. Review of phase noise concepts

Phase is simply a number - an angle - the argument of a trigonometric function:

$$V(t) = V_0 \sin(\underbrace{\omega t + \phi_0}_{PHASE}) \quad (1)$$

where ϕ_0 is an initial phase at the (arbitrary) time t=0. Frequency is simply the time derivative of phase: that is, the rate at which phase increases with time. Conversely, phase is the integral of frequency:

$$\Phi(t) = \int_0^t \omega(t)dt + \phi_0 \quad (2)$$

Since the voltage at the input of a VCO controls frequency, white noise at the input of an open-loop VCO is integrated to give a nonstationary "random walk" in phase at the VCO output. This nonstationarity prevents us from straightforwardly using the usual transform tools to move between the time and frequency domains.

We cannot measure phase directly; we can only observe a signal (usually voltage) which is a function of phase.

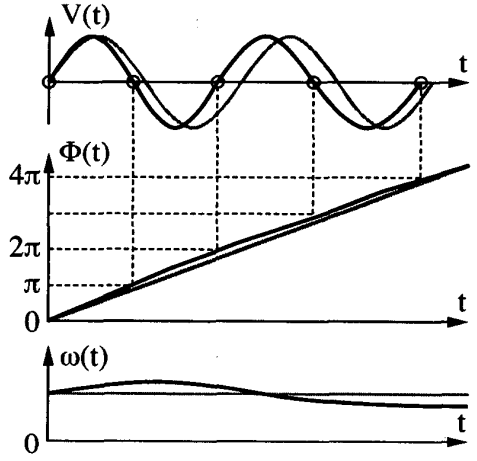


Fig. 1. Jitter, phase error, frequency error.

Fig. 1 shows different ways of characterizing phase noise from observations of the voltage.

Although phase is a continuous time variable, it is often more convenient to measure it using a sampling approach: that is, to record the times when the phase of the waveform equals a known value. For example, as shown in Fig. 1, when the voltage waveform crosses zero in a positive going direction we know the phase is a multiple of 2π. When there is no phase noise, frequency is constant, phase increases uniformly, and the zero crossing times are evenly spaced at intervals of the period $T = 1/f_0$.

In the presence of phase noise, as shown in Fig. 1, the zero crossing times are not evenly spaced. In the time domain, the effect of phase noise is characterized as jitter: variations in the zero crossing times from the ideal.

Phase noise can also be characterized in the frequency domain. An ideal sine wave in the time domain corresponds to an ideal impulse in the (single sided) frequency domain. In the frequency domain, phase noise is characterized by the magnitude of the "close in" sidebands around the ideal impulse in frequency.

B: PLL Closed Loop Error Analysis

Fig. 2 shows a block diagram of the PLL as a control system, where the controlled variable is phase [11]. θ_i is the input phase from the reference that the PLL is tracking. θ_O is the phase of the PLL output. θ_n represents the phase noise of the VCO referred to its output. Note that, although Fig. 2 shows the VCO as the source of the phase noise, the technique developed in this paper applies to any phase noise mechanism that can be referred to an equivalent $1/f^2$ noise source at the VCO output.

In many applications, the loop transfer function is overdamped [10], and the noise transfer function from θ_n to θ_O can be approximated as

$$\frac{\theta_o}{\theta_n} = \frac{s}{s + 2\pi f_L} \qquad (3)$$

A typical Bode plot of (3) is shown in Fig. 3. The loop bandwidth f_L is determined by K_d, K_O and F(s). As mentioned in part I.A, θ_n can be represented by integrated white noise giving a $1/f^2$ power spectral density (psd).

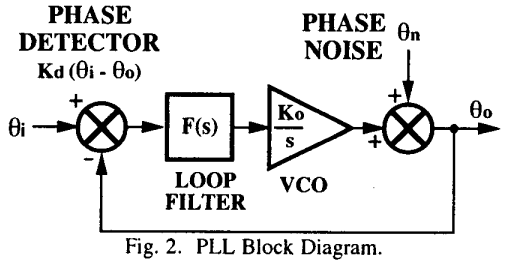


Fig. 2. PLL Block Diagram.

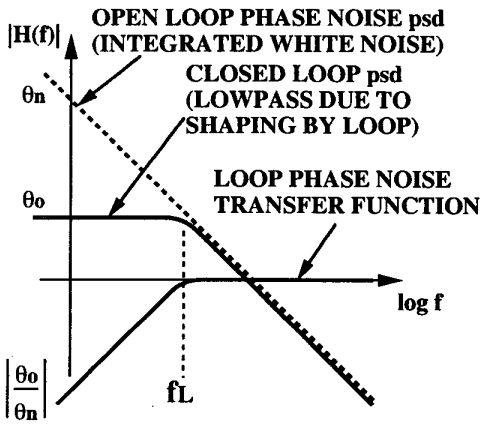


Fig. 3. PLL output phase noise psd.

When this is passed through the loop filter, the result is the lowpass noise process shown. Although the open loop VCO noise process is nonstationary, the process at the output of the closed loop VCO is stationary, due shaping of the noise by the loop filter.

C. Measuring phase noise: Frequency domain

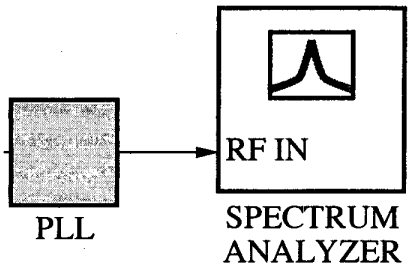
The phase noise power spectral density $S_\phi(f)$ is measured in the frequency domain using a spectrum analyzer or, for higher accuracy, a phase noise measurement system [12]. The frequency domain is appropriate for measuring phase noise in applications such as frequency synthesis for wireless communication [6]. Even in applications for which PLL performance is specified as jitter in the time domain, understanding the frequency domain performance of the PLL can be important as a guide to design for improved jitter. This is because, as mentioned in the section 1.B, the frequency response of the PLL loop filter shapes the open-loop phase spectrum of the voltage controlled oscillator (VCO), which influences the jitter of the PLL output.

Case (i): Frequency domain, VCO open loop

With the VCO operating open loop, $S_\phi(f)$ as measured on the spectrum analyzer has the characteristic shown in Fig. 4a. Since the VCO integrates phase noise, the noise power is proportional to $1/f^2$, where f is the offset from the center frequency f_0. The proportionality constant N_1 is a frequency domain figure-of-merit.

Case (ii): Frequency domain, PLL closed loop

When the loop is closed around the VCO, $S_\phi(f)$ has the characteristic shown in Fig. 4b. Since the PLL drives the VCO to track the transmit clock, the noise power levels off for offset frequencies below the loop bandwidth f_L.



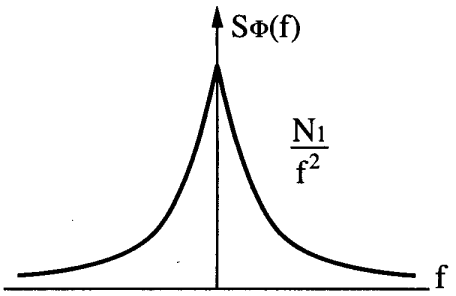
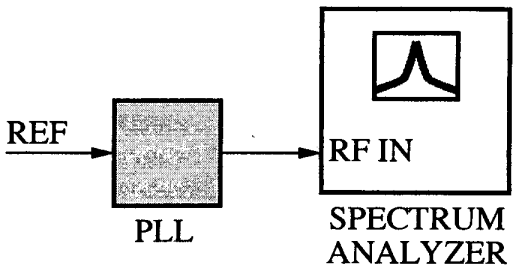


Fig. 4a. Frequency domain, VCO open loop.



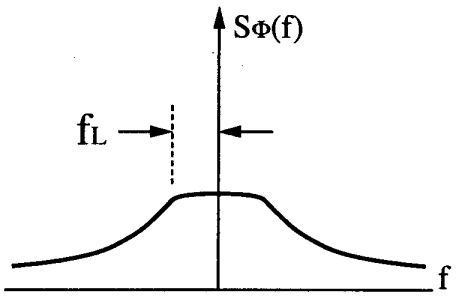


Fig. 4b. Frequency domain, VCO closed loop.

C. Measuring jitter: Time domain

Jitter can be measured in the time domain using an instrument such as communications signal analyzer (CSA) [13].

Case (iii): Time domain, closed loop, input referenced

This measurement is made as shown in Fig. 4c. The PLL reference is used as the CSA trigger; the PLL output is observed on the CSA. The CSA compares the phase difference between transitions in the input and output waveforms. Ideally, with no jitter, the difference would be constant. In reality, in the presence of jitter, a distribution is observed. The CSA records a histogram of this distribution as shown in Fig. 4c. The standard deviation σ_x is taken as a measure of jitter.

Case (iv): Time domain, closed loop, self referenced

This measurement is made as shown in Fig. 4d. The PLL output is used as both the trigger and the input to the CSA. The CSA compares the phase difference between transitions in the output waveform, separated by a delay derived from the CSA's internal time base. As in the previous case, a distribution of phases is observed. In this measurement, technique, however, the standard deviation $\sigma_{\Delta T}$ is observed to depend on the delay ΔT between the edges being measured. The standard deviations $\sigma_{\Delta T}$ can be plotted as a function of delay ΔT; a plot of the form as shown in Fig. 4d results. The advantage of this measurement technique is that it requires access only to the recovered clock, and the plot provides more information than the single number which

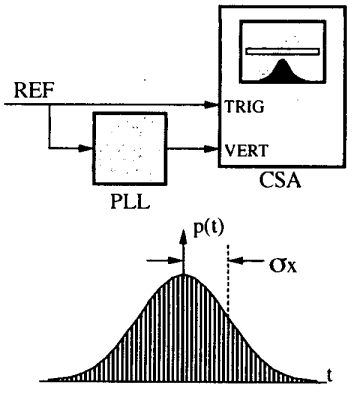


Fig. 4c.
Time domain, closed loop, input refd.

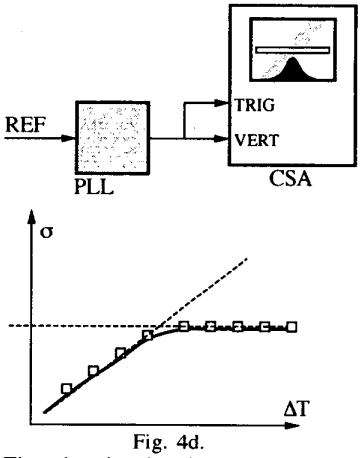


Fig. 4d.
Time domain, closed loop, self refd.

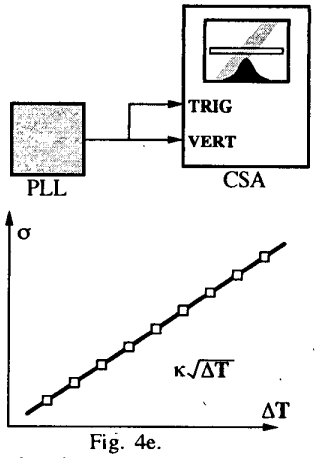


Fig. 4e.
Time domain, open loop, input refd.

is the result of case (iii).

Case (v): Time domain, open loop, self referenced

This measurement is made similarly to that shown in Fig. 4d, except that the PLL loop is opened so that the VCO free runs. Again, the standard deviations $\sigma_{\Delta T}$ are plotted as a function of delay; in this case a plot of the form as shown in Fig. 4e results. The standard deviation is proportional to the square root of delay; the constant of proportionality is the time domain figure-of-merit κ.

As in case (iv) the plot provides more information than the single number which is the result of case (iii); another advantage is that no reference is required and the VCO can run open loop.

II. THEORETICAL DEVELOPMENT

The major contribution of this paper is a mathematical methodology for linking all of the performance measures in cases (i) through (v). Note that the performance measures in the "open loop" portion of the figure correspond to nonstationary processes. This is shown in the unbounded standard deviation as delay time goes to infinity in Fig. 4e, and the nonconvergent noise power integral as offset frequency goes to zero in Fig. 4a.

Following is the derivation of these mathematical relationships.

Case (i): Frequency domain, VCO open loop

When the VCO is free running (PLL open loop), we assume the phase noise psd to be dominated by integrated white noise. With this assumption, the psd at the VCO output is modeled by

$$S_{\phi OL}(f) = \frac{N_1}{f^2} \tag{4}$$

where f is the offset frequency from the "carrier" (VCO free-running frequency) [9]. The value of N_1 for a particular VCO can be determined from a spectrum analyzer measurement. Since (4) goes to infinity as f approaches 0, the integral of phase noise power over all frequencies does not converge.

Note that this model implies that this methodology, although developed for PLL/VCO design, applies to any oscillator with a psd that fits a $1/f^2$ model.

Case (ii): Frequency domain, PLL closed loop

From section I.B and Fig. 3, however, we see that the effect of the loop filter is to make the closed loop psd of the form

$$S_{\phi CL}(f) = \frac{N_1/{f_L}^2}{1+\left(f/f_L\right)^2} \tag{5}$$

where f_L is the loop bandwidth, which is known by design.

Case (iii) Time domain, closed loop, input referenced

Equation (5) can be integrated over all frequencies to give the average power of the jitter process, which gives the variance of jitter performance, σ_x^2:

$$\int_{-\infty}^{+\infty} \frac{N_1/{f_L}^2}{1+\left(f/f_L\right)^2} = \frac{N_1\pi}{f_L} = {\sigma_x}^2 \tag{6}$$

Note that (6) gives rms jitter in units of radians; expressing rms jitter in units of time gives

$$\sigma_x = \frac{1}{f_0}\sqrt{\frac{N_1}{4\pi f_L}} \tag{7}$$

Case (iv): Time domain, closed loop, self referenced

There is also an indirect Fourier transform relationship between (5) and the plot of jitter as a function of delay in the self referenced time domain measurement. An analysis of the jitter process [10] shows that

$${\sigma_{\Delta T}}^2 = 2\left({\sigma_x}^2 - R_{XX}(\Delta T)\right) \tag{8}$$

where $R_{XX}(\Delta T)$ is the autocorrelation of the jitter process. By the Wiener-Khinchine theorem, $R_{XX}(\Delta T)$ is directly related to the psd by a Fourier transform. By taking the inverse Fourier transform of (5), substituting into (8), we obtain an expression for the closed-loop, self-referenced jitter $\sigma_{\Delta T}$ as a function of delay ΔT:

$${\sigma_{\Delta T}}^2 = 2{\sigma_x}^2\left(1 - e^{-2\pi f_L \Delta T}\right) \tag{9}$$

Case (v): Time domain, open loop, self referenced

Now all that remains is to link (9) with the open loop plot of $\sigma_{\Delta T}$. From the spectrum analyzer results, we see that the open loop spectrum can be considered to be the limiting case of the closed loop spectrum as f_L approaches zero. If we take the limit of (9) as f_L approaches zero, using the result for ${\sigma_x}^2$ from (7), we obtain an expression for the open-loop, self-referenced jitter $\sigma_{\Delta T}$ as a function of delay ΔT:

$${\sigma_{\Delta T}}^2 = 4\pi^2 N_1 \Delta T \tag{10}$$

Note that (10) can be expressed in the form

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \tag{11}$$

with

$$\kappa = 2\pi\sqrt{N_1} \tag{12}$$

Thus the link is established from the open loop frequency domain phase noise measure (characterized by the figure-of-merit N_1) to the open loop time domain measure (characterized by the figure-of-merit κ). The mathematical relationships linking the performance measures in Figs. 4a through 4e are summarized in table form in Fig. 5. This table is a powerful design aid for rapidly

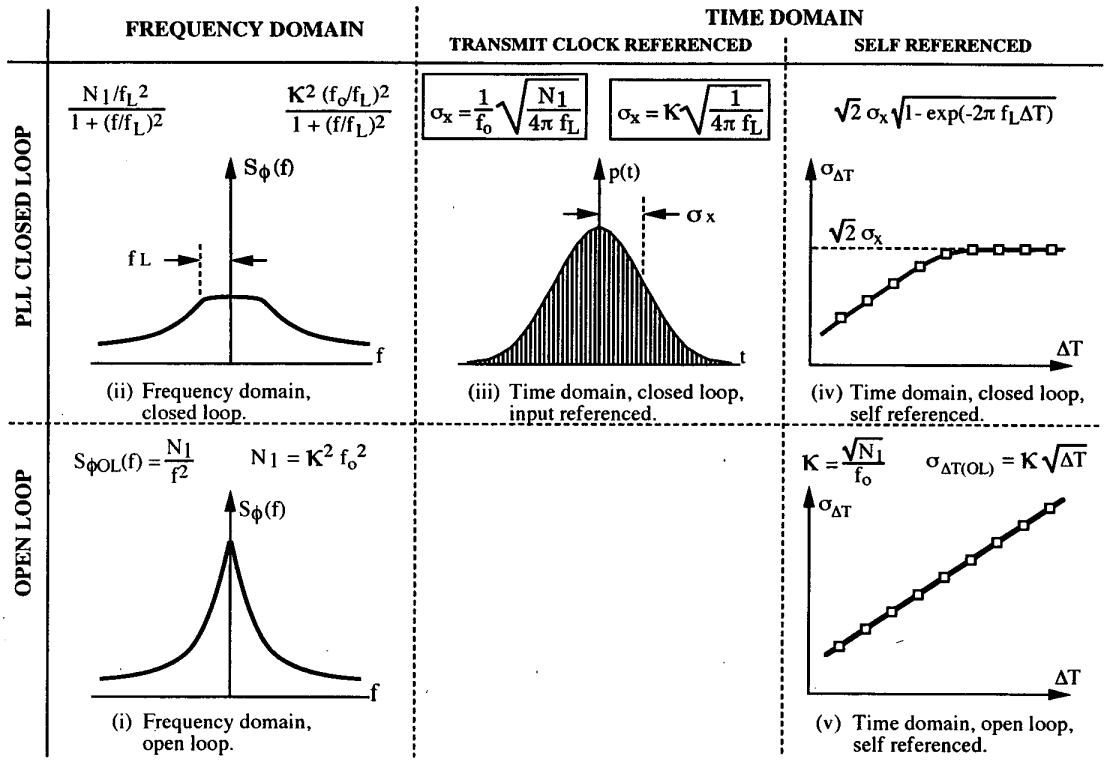


Fig. 5. Mathematical relationships among performance measures.

relating oscillator performance in any of the domains indicated.

It should be emphasized that a key concept in this technique is the use of a single figure-of-merit, N_1 or κ, to relate system-level performance (such as jitter or phase noise) to circuit-level parameters (such as power dissipation and signal amplitude). For example, in [2] expressions are developed for contributions to system-level κ as a function of power dissipation in the delay stage of a ring oscillator.

III. APPLICATION

A. Design Example

Consider the following design problem: A VCO with center frequency of f_0 = 622MHz and phase noise -106dBc at a 1MHz offset is to be used in a PLL. Assuming the VCO is the dominant source of jitter, what is the required loop bandwidth f_L to realize a jitter of σ_x=10 ps rms?

The first step is to determine the figure-of-merit N_1 from the offset frequency specification (converting from dBc/Hz):

$$10^{(-106/10)} = \frac{N_1}{(1MHz)^2} \Rightarrow N_1 = 25.1Hz \tag{13}$$

From Fig. 5 case (iii), the required value of f_L is obtained by solving

$$10ps = \frac{1}{622MHz}\sqrt{\frac{25.1Hz}{4\pi f_L}} \Rightarrow f_L = 51.6kHz \tag{14}$$

B. Experimental Verification

The measurements in this section were made using a Tektronix CSA803 communications signal analyzer [13] and a Hewlett-Packard HP4195A spectrum analyzer [14]. The device under test is the Analog Devices AD802 clock recovery phase locked loop [15].

Fig. 6 shows a spectrum analyzer plot for the open loop VCO. The superimposed curve is for an N_1 value of 157 Hz with loop bandwidth of 98 kHz, which gives a good fit to (5). The measured jitter σ_X was 66.7 ps rms. The predicted value from (7) is

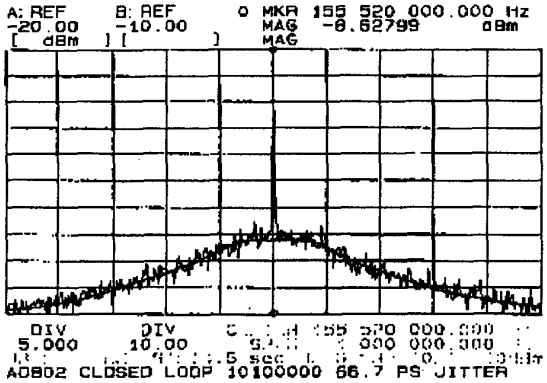


Fig. 6. Closed loop phase noise plot.

$$\frac{1}{155MHz}\sqrt{\frac{157Hz}{4\pi(98kHz)}} = 73ps\ rms \tag{15}$$

which is within 10% of the CSA measured value.

IV. CONCLUSIONS

This paper has described a technique for relating five different measures of oscillator jitter and phase noise. The technique improves the design process by allowing VCO and PLL design to take place in the domain (time/frequency, open/closed loop) that provides the most insight into sources of jitter, while allowing a direct link to the applicable performance measure. The technique also speeds simulation since only the open loop VCO need be simulated, which allows a substantial savings in simulation time. Experimental results on an existing PLL show good agreement to the theoretical predictions.

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