

A CMOS analog integrated circuit for detector readout at a 50MHz pixel rate

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ABSTRACT

This paper describes a high speed, low noise analog integrated circuit which has been designed to interface with charge-coupled device (CCD) arrays in high speed CCD camera systems. This IC performs the analog signal processing functions required between the CCD output and analog-to-digital converter (ADC) input. Channel gain can be adjusted from 2.7 to 12 in 16 steps as specified by a 4 bit digital word. The chip operates from power supply voltages of $\pm 5V$, dissipates 380 mW / channel, and has an input referred noise of 260 μV rms.

1. INTRODUCTION

1.1 Application

This work involves design of analog signal processing electronics for use in a high speed CCD camera. Figure 1 shows a typical block diagram of such a camera system. A digital control block provides timing signals to the CCD, analog signal processing block, and ADC. Level shifting drivers translate the digital logic signals to the voltage levels required by the CCD. As directed by the timing signals, the CCD shifts photogenerated charge packets from each pixel to produce an analog output signal. The CCD output signal is a pulse waveform, in which the amplitude of each pulse represents the light intensity in a corresponding pixel. Depending on the CCD array format, there may be one, two, or many analog output channels. The CCD output is the input to the analog signal processing (ASP) block.

Figure 2 shows the CCD analog output waveform v_{CCD} in more detail. The signal is a negative-going pulse, the amplitude of which is proportional to incident light intensity for the corresponding pixel. The IC described in this paper can process pulses with a peak amplitude from 250mV to 750mV. The duration of the signal pulse is half the pixel period. This leads to the requirement for high speed design in the signal processing electronics; for a pixel readout rate of 50MHz, the pixel period is $1/50\text{MHz} = 20\text{nsec}$. Thus the signal pulse is only available for $T_{PIXEL}/2 = 10\text{nsec}$.

The desired waveform at the input to the ADC is also shown in Figure 2. Since the only part of the input waveform that carries intensity information is the pulse amplitude, the output is a sampled version of the pulse that is held for the entire pixel period. Holding the desired value results in a waveform that eases bandwidth requirements for the ADC.

Additionally, it is desired in this application that the signal be inverted so that a more positive voltage corresponds to an increased light intensity. The ASP output signal range should match the input full scale range of the ADC, which is either 2V or 3V. Offset voltage at the output should be adjustable to compensate for offset errors in the signal processing chain as well as in the CCD and ADC.

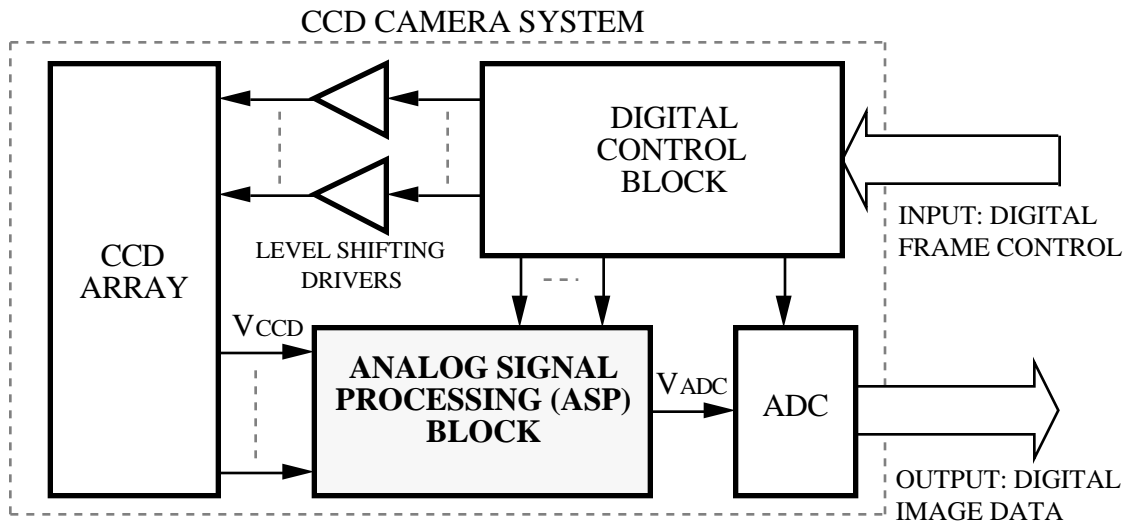


Figure 1. CCD Camera System Block Diagram.

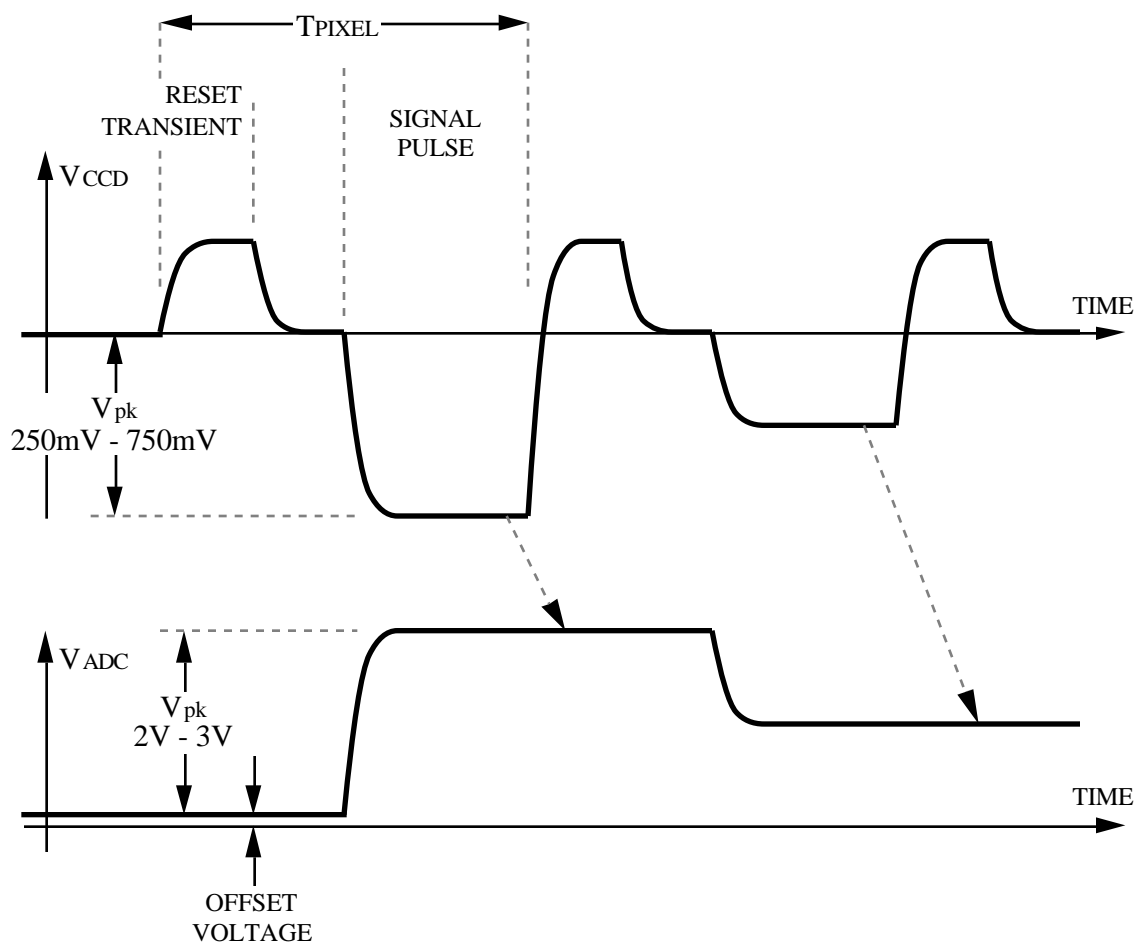


Figure 2. CCD output voltage waveform.

In addition to the desired negative-going signal pulse at the CCD output, there is a positive-going transient that results from resetting the gate voltage of the output amplifier on the CCD. This transient can be of order 500mV or greater. The signal processing electronics must be able to tolerate this transient without affecting the shape of the signal pulse.

To process the analog output from the CCD and provide a signal of suitable amplitude and drive for the ADC input, the ASP block must be able to perform the following analog functions:

- wideband, low-noise, linear gain
- sample-and-hold amplification
- offset adjustment or cancellation

The ADC converts the output of the analog signal processing block to digital form. The output of the camera is a sequence of digital words representing the sampled pixel intensities.

1.2 Advantages of CMOS IC approach

Previously, the analog signal processing functions for high speed, low noise applications have been performed with discrete ¹ or hybrid ² circuitry. For the CCD camera system, the advantages of an ASIC approach to the ASP block design are as follows:

- **Reduced camera size**
All analog signal processing circuitry is contained in one package, consuming less board space outside the CCD.
- **Reduced power**
In a discrete design, signals must traverse many board-level chip-to-chip connections. Driving the capacitance of these interconnections with high-speed signals dissipates substantial power. With an ASIC approach, most high-speed signals run on low-capacitance on-chip paths. The reduced capacitance requires a lower current to drive the signal at the same speed.
- **Reduced assembly cost**
The ASIC is a single package; a discrete design approach requires multiple packages and components.
- **Reduced test cost**
The ASIC is a stand-alone functional block which can be pre-tested.
- **Comparable or reduced total cost**
Depending on ASIC technology chosen, the cost of the analog ASIC will be comparable to or lower than the cost of equivalent discrete parts.
- **Improved performance**
The ASIC circuit design is optimized for CCD signals. By contrast, a discrete design must use general-purpose components which trade off performance to be suitable for many applications.

2. CIRCUIT DESIGN

2.1 Definition of specification

The performance "must-haves" and system-level goals for the ASIC were defined as follows:

- Process
For minimum cost, the fabrication process chosen was a 1.2 μ m, double-poly, double-metal CMOS process. No special analog structures (such as linear capacitors) are required.
- Number of channels
The ASIC will have 2 channels. The channels will be powered separately to minimize crosstalk and allow power saving by shutting off the second channel in systems where only one channel is required.
- On-chip functionality

The functional block diagram of one channel is shown in Figure 3.

The input to the ASIC is the CCD output voltage V_{CCD} . The input is AC coupled through capacitor C1. This will allow use of the ASIC even if the CCD output rides on a DC level which exceeds the ASIC power supply voltage. Analog switch SW1 clamps the DC voltage on C1 to the correct value during the line interval.

The goal is to process signals at a 50 MHz pixel rate ($T_{PIXEL} = 20\text{ns}$) with an amplitude ranging from 250mV to 750mV. Integrating this high an operating speed and achieving the required low noise performance was the most challenging technical aspect of this research. The slowest pixel rate will be 500kHz ($T_{PIXEL} = 2\mu\text{s}$). This limit is to preserve accuracy of AC-coupled waveforms in the presence of droop.

The first stage seen by the input signal is a low noise preamplifier with a fixed inverting gain of approximately -3. This value is high enough so that the input stage is the dominant noise contributor, but not so high that frequency response is compromised in a gain-bandwidth tradeoff. The preamp also provides single-ended to differential conversion, so the on-chip signal can be processed with differential techniques.

Switches SW2A and SW2B and capacitor C2 form a sample-and-hold circuit that samples the pulse at the preamp output as directed by the external PIXEL S/H logic signal. Sampling has benefits for both digital and analog camera systems. In digital systems, sampling and holding the CCD output eases requirements on the dynamic performance of the ADC input. In analog systems, sampling reduces the bandwidth of the analog output signal.

The hold capacitor C2 is buffered by a variable gain amplifier, which also provides for an adjustable gain from 0.9 to 4. This allows the flexibility to adjust the input-to-output gain of the signal processing chain from -2.7 to -12. This range will accommodate most combinations of CCD output voltage swing and ADC input full scale range.

The gain of the amplifier is determined by external coarse and fine gain controls. Coarse gain control is provided by a 4 bit digital word which allows selection of one of 16 gain values. Fine gain control, if necessary, is provided with a voltage controlled gain input that allows adjustment of gain to span the range between adjacent steps.

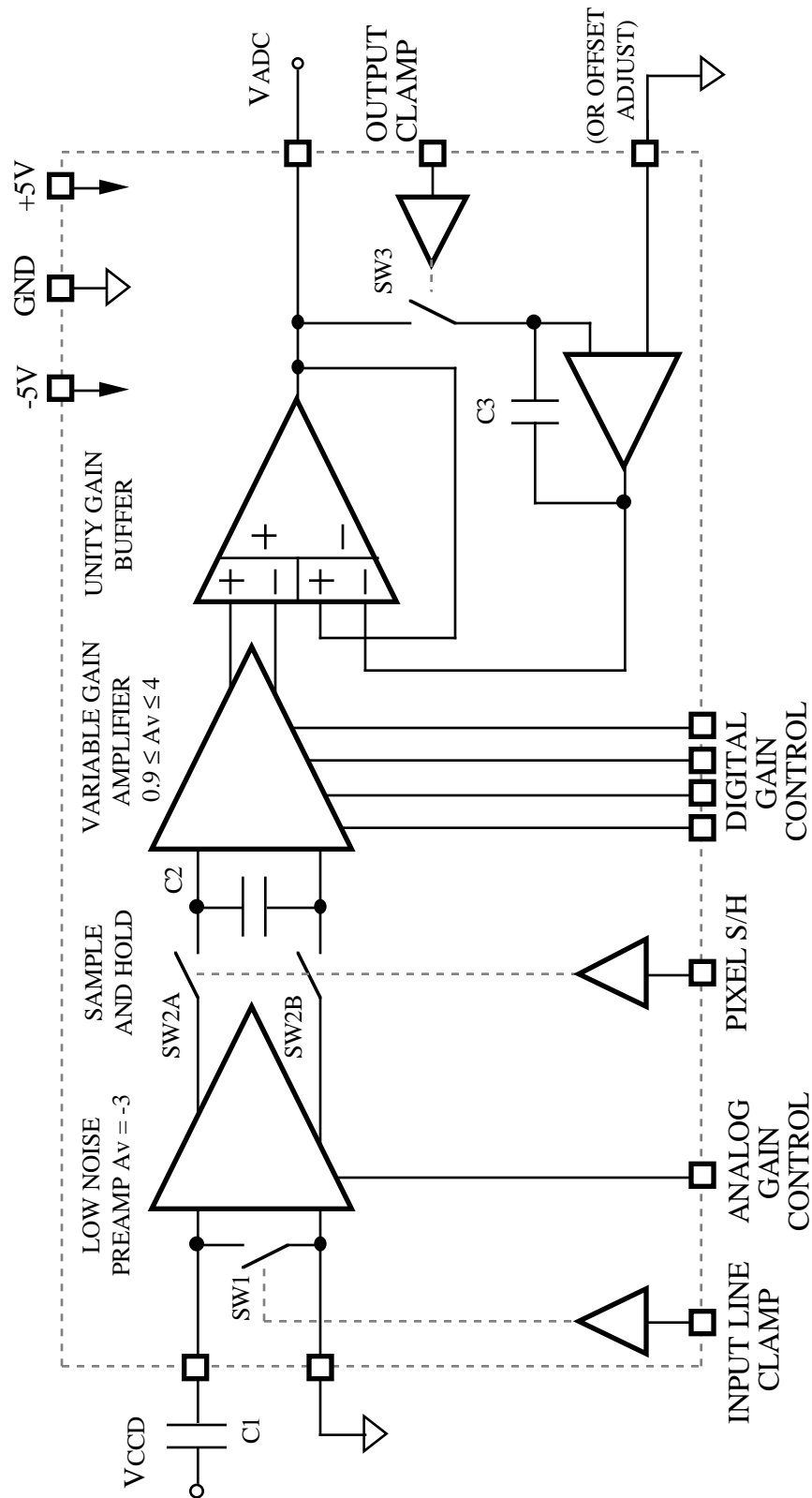


Figure 3. CMOS IC Block Diagram.

The output of the variable gain amplifier is DC restored by subtracting a DC voltage stored on capacitor C3. The correct DC voltage is established by turning on switch SW3 during the line interval. The baseline voltage is provided by an external pin, allowing flexibility for offset adjustment or restoration to a voltage other than ground. A unity-gain buffer provides current drive for the load connected at the ASIC output V_{ADC} .

- Power supplies

The required power supply voltages are $\pm 5V$ ($\pm 5\%$). The majority of power consumption is in the input stage (for low noise) and output stage (for driving the load capacitance at high speed). Each of the 2 channels on chip will be powered separately to allow power saving when only one channel is required.

2.2 Input stage

The system requirements affect the design of the input stage in the following areas:

- low noise
- moderate gain (approximately 3)
- wideband performance

The wideband performance is needed to process the 10-nsec-wide pulses from the CCD output. This stage also converts the single-ended input signal to differential form for on-chip processing. Advantages of differential signal processing include:

- inherent immunity to common-mode noise sources such as power supply ripple
- insensitivity of linearity performance to second order distortion effects
- inherent cancellation of charge injection in subsequent sample-and-hold stage

The gain of -3 in the preamplifier is sufficient so that the input stage dominates the noise performance of the system. The overall system-level goal is specified in terms of causing no more than a 10% degradation in the typical CCD noise floor of 50 e^- rms:

$$\sqrt{55^2 - 50^2} = 22.9 \text{ } e^- \text{ rms} \quad (1)$$

The design goal was chosen to be 20 e^- rms. Assuming an array responsivity of $5\mu V/e^-$, this corresponds to an input voltage noise of 100 μV rms. For settling of a 10nsec wide pulse, a time constant of 1nsec gives a bandwidth of

$$\frac{1}{2\pi(1\text{ns})} = 160 \text{ MHz} \quad (2)$$

Assuming a single pole rolloff, this gives the required input noise density e_n :

$$e_n \sqrt{\frac{\pi}{2}} 160 \text{ MHz} = 100 \mu V \text{ rms} \rightarrow \boxed{e_n = 6.3 \text{ nV}/\sqrt{\text{Hz}}} \quad (3)$$

This gives the noise and bandwidth specifications which are necessary for circuit-level design of the input stage.

2.3 Sample-and-hold

This stage samples the amplified pulse from the input stage, as directed by the external PIXEL S/H logic signal. Note that, due to the internally differential architecture, the sample-and-hold amplifier pedestal appears as a common mode term at the (differential) input of variable gain amplifier. The result is inherent first-order cancellation of the pedestal.

2.4 Variable gain amplifier

The required input-to-output gain is set by the goal of interfacing to an ADC with full scale input range of 2V or 3V. The desired range of input amplitudes for V_{PEAK} ranges from 0.25V to 0.75V. The maximum and minimum gains are therefore:

$$A_{V(min)} = \frac{2}{0.75} = 2.7 \quad A_{V(max)} = \frac{3}{0.25} = 12 \quad (4, 5)$$

A key feature of this chip is a digitally programmable gain stage that provides for an adjustable gain from 0.9 to 4. This allows the flexibility to adjust the overall input-to-output gain of the IC signal processing chain from -2.7 to -12. This range will accommodate most combinations of CCD output voltage swing and ADC input full scale range. The gain will be set by an external 4-bit digital word.

This amplifier uses an open-loop, degenerated differential pair to achieve high speed performance while maintaining acceptable linearity. The gain is determined by the ratio of load resistance and degeneration resistance. Variation in gain is achieved by switching in different values of resistance. Gain stability over temperature is achieved by making the gain dependent on the ratio of resistances (actually the inverse of MOSFET transconductances), which tend to track over temperature. The goal for linearity performance is an output error less than 1% of the output full scale range.

2.5 Output stage

The differential output of the variable gain amplifier is converted to single-ended form with a differential difference amplifier³. The baseline voltage is provided by an external pin, allowing flexibility for offset adjustment or restoration to a voltage other than ground. A unity-gain buffer provides current drive for the load connected at the IC output. The output must be able to drive a "typical" ADC input of $30pF \parallel 12k\Omega$ to 3V at the full speed pixel rate of 50MHz.

The timing can be configured to reset the dark level offset to nominal zero during each line interval. If desired, the zero level can be further adjusted with an externally applied trim voltage. This voltage is subtracted out at the output stage, thus minimizing the input-referred noise due to the externally supplied voltage.

3. TEST RESULTS

The circuitry used to test chip performance is shown in Fig. 4. A video DAC was used to provide a high speed pulse waveform to simulate the CCD output. The DAC input is ramped in linear steps over its full scale range to test the linearity of the chip. To produce a "worst-case" dynamic waveform that fully exercises the amplifier and sample-and-hold, the input is alternated between the pulse amplitude and zero. The output of the chip was observed on a Tektronix CSA803 Communications Signal Analyzer.

3.1 Speed

Figure 5 shows the input and output waveforms at a pixel rate of 50MHz. Although the measured waveform shows some degradation due to limitations in the test fixture, functional operation at 50MHz is seen.

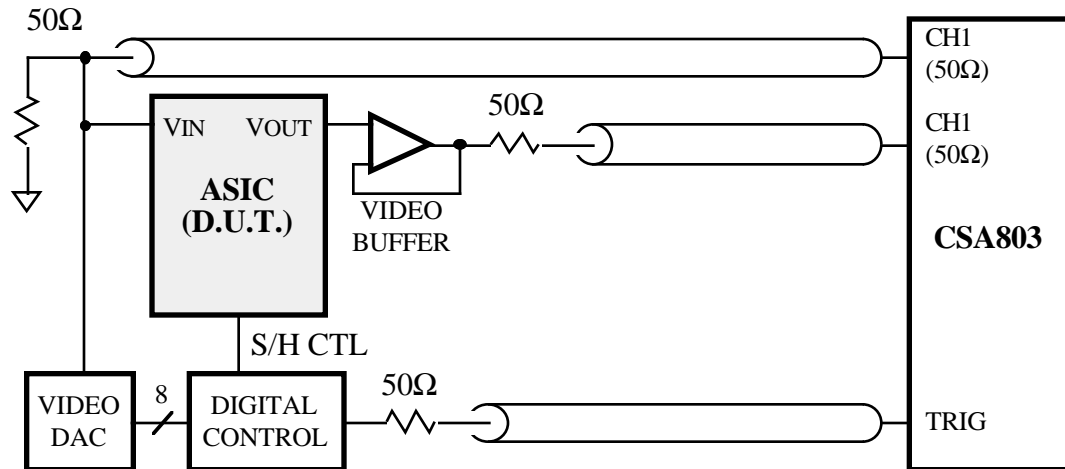


Fig. 4. Test fixture.

3.2 Gain linearity

Figure 6 shows the input-output linearity error as a percentage of full scale range. This linearity was obtained under dynamic conditions at a pixel rate of 10MHz. (It was not possible to obtain linearity data at full speed due to limitations in the test fixture.) The worst case linearity is within the $\pm 1\%$ specification goal.

3.3 Noise

Figure 7 shows the measured noise of 1.67 mV rms at the chip output. This was obtained under maximum gain conditions, with an attenuation of 2X due to the termination of the line to the CSA803. When this noise was referred to the chip input, and the measured noise of the test fixture (851 μ V rms, output referred) was removed, the resulting input referred noise was 260 μ V rms, which is 52 e^- with an array responsivity of 5 μ V/ e^- . This is more than a factor of two worse than the design goal for noise. At present, work is continuing to determine if this noise is caused by limitations in the test fixture, or is due to the chip itself.

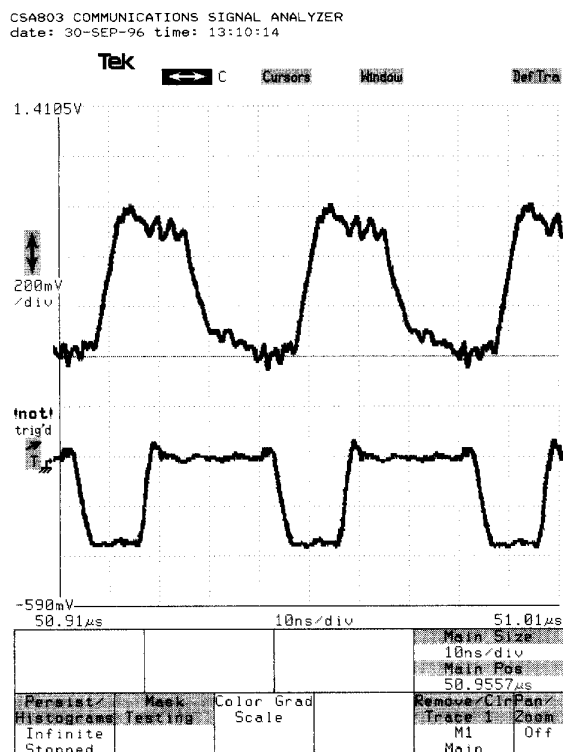


Fig. 5. Output at 50 MHz pixel rate.
Top: output; bottom: input

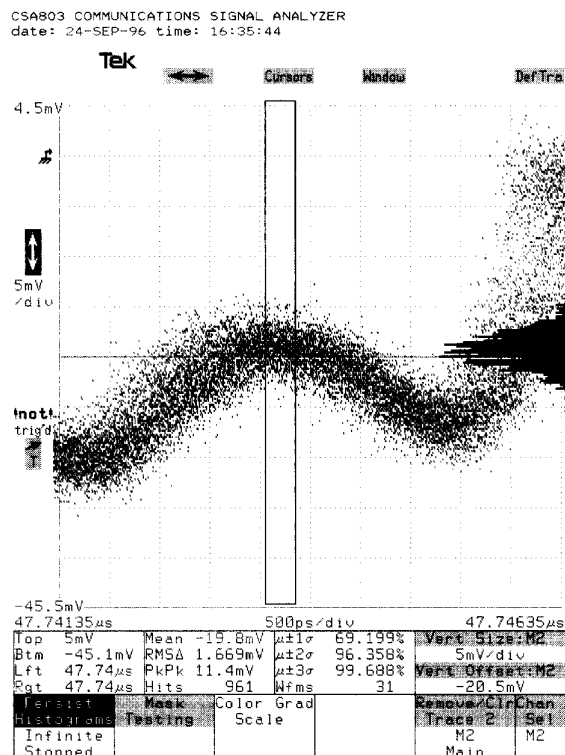


Fig. 7. Output noise of 1.67mV rms.

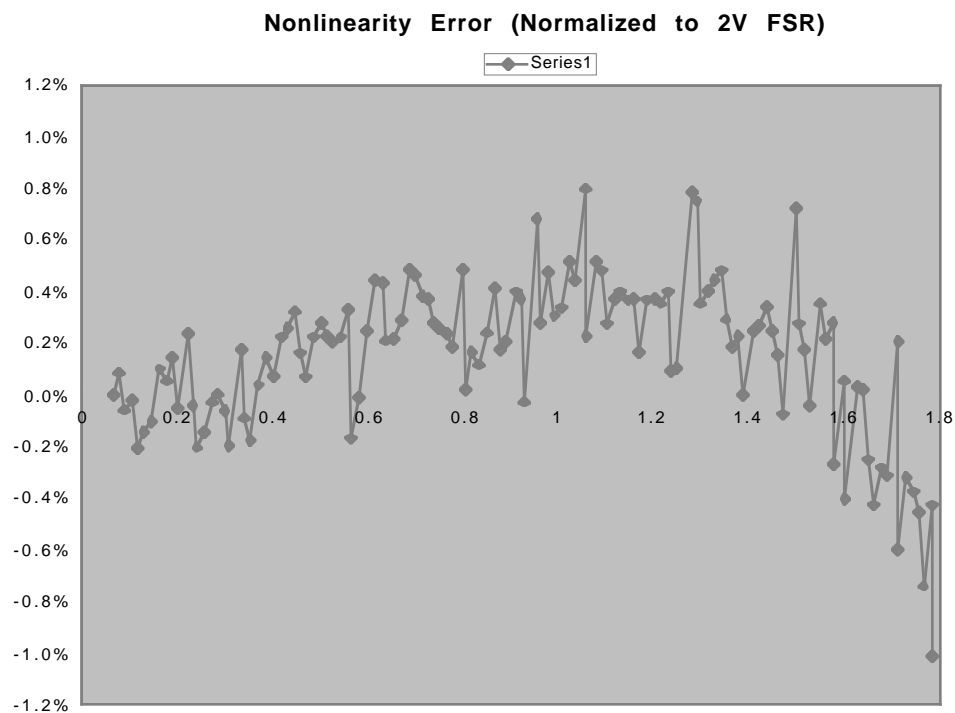


Fig. 6. Measured nonlinearity, dynamic conditions, as fraction of full scale.

4. CONCLUSION

An analog integrated circuit has been designed to interface with CCD arrays in high speed camera systems. This IC performs the analog signal processing functions required between the CCD output and analog-to-digital converter (ADC) input. This IC has been fabricated in a low cost, 1.2 μm "digital" CMOS process requiring no special analog structures. Functional operation at a pixel rate of 50MHz has been verified. Input referred noise has been measured at 260 μV rms. Dynamic linearity has been measured at better than $\pm 1\%$ at a pixel rate of 10MHz. The chip consumes 380 mW / channel from power supplies of $\pm 5\text{V}$.

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