"Split-ADC" Digital Background Correction of Open-Loop Residue Amplifier Nonlinearity Errors in a 14b Pipeline ADC

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***Abstract*—The "Split ADC" architecture concept is applied to correction of errors due to nonlinearity of an open-loop residue amplifier in a pipeline ADC. Determination of calibration parameters and correction of errors takes place entirely in the background in the digital domain; no interaction with analog circuitry is required. An algorithm exhibiting convergence of calibration parameters in fewer than 100 000 conversions is presented.**

***Index Terms*—Analog–digital conversion, adaptive systems, calibration, self-calibrating, digital background calibration, mixed analog-digital integrated circuits, pipeline ADC.**

I. Introduction

THE use of open-loop residue amplification in pipelined ADCs has been the subject of recent investigation due to the power advantages over more precise closed-loop techniques, as well as the general appeal of relaxing accuracy requirements on analog circuitry in deep submicron CMOS. Due to the nonlinearity of the open-loop amplifier, digital calibration is used to restore acceptable linear performance for the overall ADC. Previous work [1] has described statistically based methods for determining the required calibration coefficients, which have the drawback of relatively long adaptation times.

The "Split ADC" concept [2-3] has been applied to correct linear gain errors in algorithmic and pipeline ADCs, and has the advantage of faster calibration convergence. The purpose of this paper is to present an algorithm applying the split ADC approach to digital background correction of errors in pipeline ADCs arising from the nonlinearity of open-loop residue amplifier stages. Compared with [1], the novel contribution of this work is the dramatically reduced time for calibration convergence by adopting the split-ADC approach to correct amplifier nonlinearity errors, thereby making calibration of converters in the 14b to 16b range feasible.

This paper is organized as follows: Section II provides a description of the pipeline ADC investigated for this work and a general overview of the split ADC concept. Section III describes the theory behind the digital correction technique and the background calibration algorithm. Experimental results from circuit- and behavioral-level simulations are presented in Section IV.

II. Background

A. Split ADC

The concept of the split ADC architecture is shown in Figure 1. The ADC is split into two channels, each converting the same input and producing individual output codes x_A and x_B. The average of the two outputs is reported as the ADC output code x. The background calibration signal is developed from the difference Δx between codes x_A and x_B. If both ADCs are correctly calibrated, the two outputs will agree and the difference Δx will be zero. In the presence of nonzero differences, the pattern of "disagreements" in Δx can be examined in an error estimation process to adjust

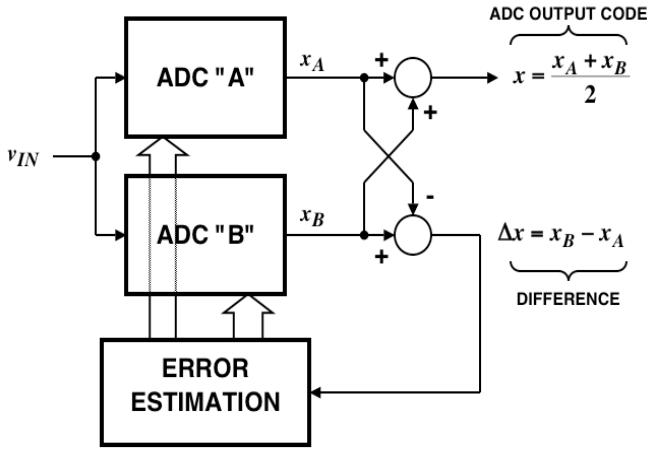

Fig. 1. Split ADC concept.

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calibration parameters in each ADC and drive the difference and the ADC errors to zero.

Comparison with statistical background calibration techniques in [1] shows the advantage of using the difference Δx for the calibration signal: the magnitude of the unknown ADC input signal is greatly reduced by the subtraction in the calibration signal path. Thus, as discussed in [2-4], it is not necessary to accumulate a large number of conversions to decorrelate the input signal, which is required in the case of statistically based digital background calibration techniques.

B. Pipeline ADC

A block diagram of the ADC investigated in this work is shown in Figure 2. The pipeline ADC is split into two identical halves, each processing the same input signal. A single 4-bit pipeline stage with open loop reside amplification similar to that of [1] was designed in a 0.25 µm CMOS process. This block was used for all stages of the pipeline. Improvements from options such as stage scaling and optimization of stage resolution were not investigated, in order to simplify the design process and focus on the digital correction and background calibration issues. The calibration parameters required to describe each stage for digital correction are the linear gain G of the stage amplifier and a parameter p characterizing the amplifier nonlinearity.

Also shown in Figure 2 is a block diagram of each residue stage. As in [1], the S/H, ADC, and DAC functions are combined in a switched capacitor network. The ADC decision D, ($-1 \le D \le +1$) is fed to a DAC; the DAC output corresponding to D is subtracted from the sampled input v_{IN} and the difference is applied to the input of an open loop amplifier with nominal gain G. Ideally the residue amplifier would implement

$$v_R = G\left[v_{IN} - D \cdot V_{REF}\right] \tag{1}$$

As in [1, 2] the stage is capable of operating in distinct residue modes as determined by a mode select bit M. Due to the redundancy afforded by the choice of stage gain G and ADC resolution, either residue mode will allow correct operation of the entire ADC. The key to the split ADC concept is that use of different residue modes allows the "A" and "B" converters to proceed along different decision trajectories D_{iA}, D_{iB}. Despite the different trajectories, however, if the calibration parameters used in digital correction are correct, then the converters should arrive at the same result, since both see the same input. Errors in the calibration parameters will result in a nonzero difference Δx which can be used in an iterative feedback loop to null out errors in the estimated calibration parameters.

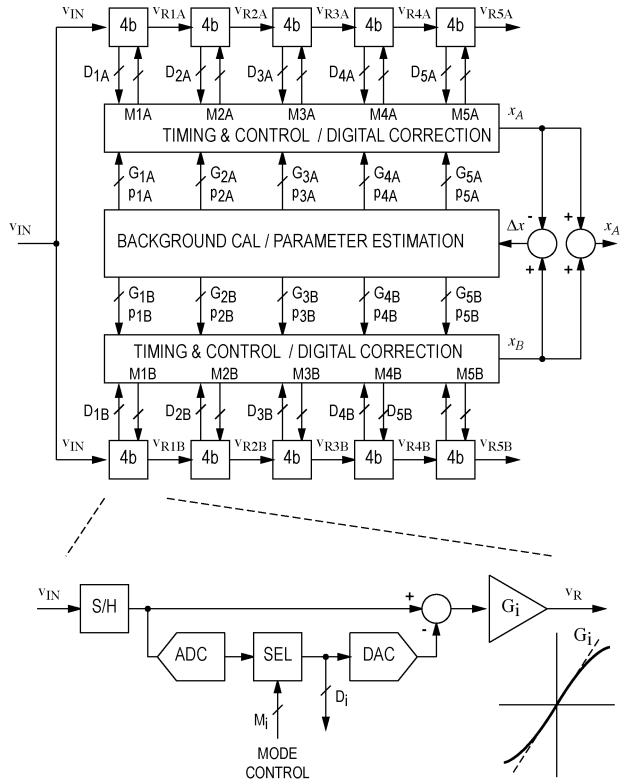

Fig. 2. Pipeline ADC block diagram.

III. ERROR ESTIMATION

A. Digital Error Correction

If the pipeline stages are linear and the stage gains G_i known, it can be shown that the corrected digital outputs are determined from the stage decisions D_i by [1]

$$x = D_1 + \frac{1}{G_1}D_2 + \frac{1}{G_1G_2}D_3 + \frac{1}{G_1G_2G_3}D_4 + \frac{1}{G_1G_2G_3G_4}D_5 \tag{2}$$

Equation (2) can be rewritten as

$$x = D_1 + \frac{1}{G_1}\underbrace{\left(D_2 + \frac{1}{G_2}D_3 + \frac{1}{G_2G_3}D_4 + \frac{1}{G_2G_3G_4}D_5\right)}_{D_b} \tag{3}$$

in which the notation D_b indicates the results of decisions D_2 through D_5 in the backend of the pipeline ADC. To simplify the following discussion, we will make the following assumptions:

i) errors in stages 2-5 are negligible; the only errors to be calibrated are the gain error and nonlinearity error of stage 1. In practice, the technique to be described could be extended to calibrate stage 2 errors if necessary.

ii) offset contributes only to overall ADC offset and has negligible effect on nonlinearity.

B. Pipeline ADC Error Modeling

Figure 3 shows a simplified model of the open-loop gain stage, with exaggerated nonlinearity for illustration purposes.

As shown in [1], the differential pair gate overdrive V_{OV}

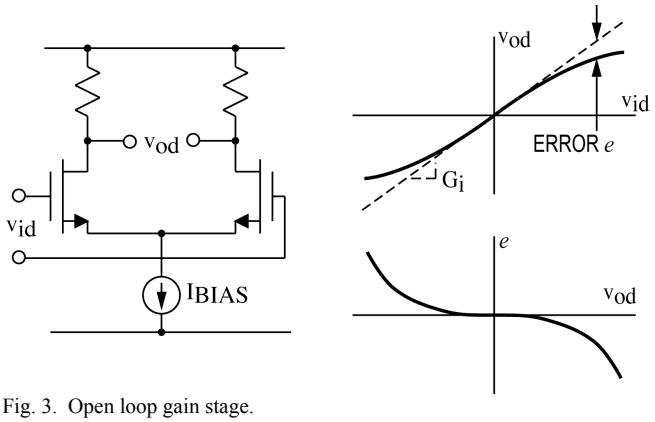

Fig. 3. Open loop gain stage.

can be chosen so that third order nonlinearity dominates; in this case the v_{id} to v_{od} relationship can be described by

$$v_{od} = Gv_{id} - \underbrace{\frac{\alpha G}{V_{OV}^{2}} v_{id}^{3}}_{e(\alpha, v_{id})} \tag{4}$$

in which $e(\alpha,v_{id})$ is the error due to the stage nonlinearity and α is a parameter determined by a power series fit to the specific residue amplifier characteristic.

One possible strategy for error correction would be to determine the parameter α using a background calibration; then if v_{id} were known, it would be possible to calculate the correction ε using the cubic term of (4); however, v_{id} is not known directly. What is known is the output v_{od}, which is measured by the back-end ADC pipeline stages and is represented in digital form as D_b. Shown in Figure 3 is a qualitative plot of the behavior of the nonlinearity error, which is a function of both the output voltage v_{od} (or, equivalently, D_b) and the cubic nonlinearity parameter α. Note that α is defined in terms of voltages v_{id} and v_{od} ; since we will be working with the digital representation D_b, we define a parameter p to capture the cubic nonlinearity in the digital domain. Since the function $e(p, D_b)$ is not available in an analytically convenient form, a table lookup approach is taken [1, 2] for calculating the quantity to be used in digital correction.

C. Estimation of Calibration Parameters

A block diagram of the calibration algorithm is shown in Figure 4. To correct for the additional nonlinearity error, the approach of (3) is modified by including a correction term for the nonlinearity defined in (4) as follows:

$$x = D_1 + \frac{1}{\hat{G}_1} D_b + e\left(\hat{p}_1, D_b\right) \tag{5}$$

where $\hat{G}_1$ and $\hat{p}_1$ represent estimates in the digital domain of the values of G_1 and p_1 describing analog domain behavior of the first stage amplifier. Fractional errors in these estimates can be defined as

$$\hat{G}_1 = G_1\left(1 + \varepsilon_{G1}\right) \tag{6}$$

$$\hat{p}_1 = p_1\left(1 + \varepsilon_{p1}\right) \tag{7}$$

Applying the definitions of (6) and (7) to (5) for each of the "A" and "B" ADCs in the split gives the following, (assuming the errors are small):

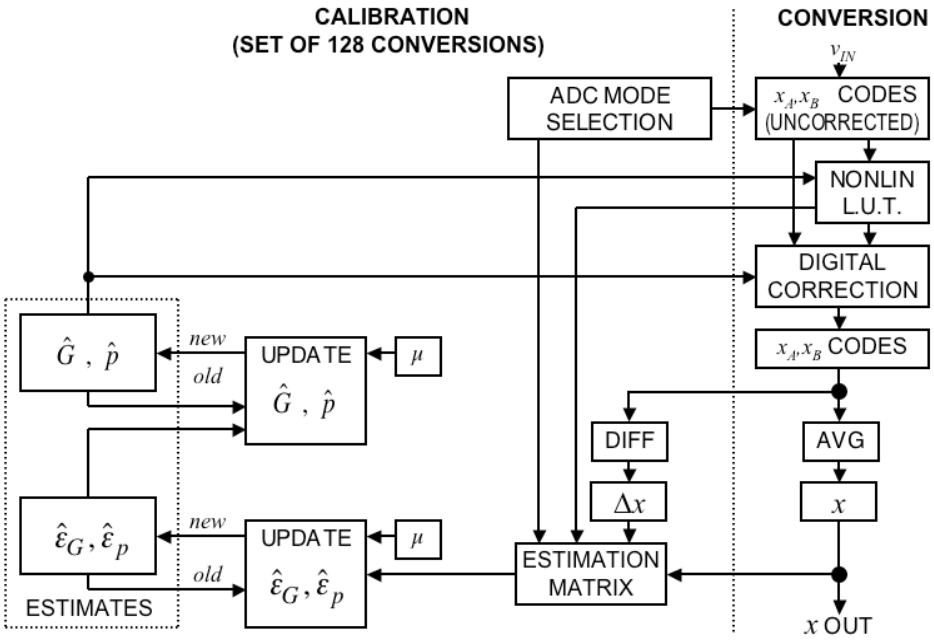

Fig. 4. Calibration algorithm block diagram.

$$x_A = D_{1A} + \frac{1}{\hat{G}_{1A}} D_{bA} + e\left(\hat{p}_{1A}, D_{bA}\right) + \left[\frac{-1}{G_{1A}} D_{bA}\right]\varepsilon_{G1A} + \left[e\left(p_{1A}, D_{bA}\right)\right]\varepsilon_{p1A} \qquad (8a)$$

$$x_B = \underbrace{D_{1B} + \frac{1}{\hat{G}_{1B}} D_{bB} + e\left(\hat{p}_{1B}, D_{bB}\right)}_{CORRECT\ CODE\quad x} + \underbrace{\left[\frac{-1}{G_{1B}} D_{bB}\right]\varepsilon_{G1B} + \left[e\left(p_{1B}, D_{bB}\right)\right]\varepsilon_{p1B}}_{ERROR} \qquad (8b)$$

Note that in (8a) and (8b), the output code from each ADC is expressed in terms of an error adding to the correct output code x. For the calibration parameter estimation loop, taking the difference cancels the correct code component leaving only terms in the parameter estimation errors:

$$\Delta x = x_B - x_A = \left[\frac{1}{G_{1A}} D_{bA}\right]\varepsilon_{G1A} + \left[-e\left(p_{1A}, D_{bA}\right)\right]\varepsilon_{p1A} + \left[\frac{-1}{G_{1B}} D_{bB}\right]\varepsilon_{G1B} + \left[e\left(p_{1B}, D_{bB}\right)\right]\varepsilon_{p1B} \qquad (9)$$

The coefficients in (9) are already calculated when performing the digital correction of (5). Observations of Δx values from several conversions are grouped in an iterative matrix solution procedure as used in [2, 3] to refine $\hat{G}$ and $\hat{p}$, driving the error in these estimates to zero. An LMS procedure updates the parameter estimates, as (for example):

$$\hat{G}_{(new)} = \hat{G}_{(old)} - \mu\,\varepsilon_G \qquad (10)$$

in which μ controls the convergence of the iteration.

IV. RESULTS

The system was simulated behaviorally using MATLAB. System parameters are given in Table 1. The amplifier nonlinearity parameter corresponded to a maximum error of 2% referred to the ±0.8V swing at the output of the residue amplifier, which was obtained from circuit-level simulation.

Figure 5 shows ADC integral nonlinearity (INL) before calibration with errors of ≈ ±30 LSB at the 14b level. After calibration, INL improves to +0.5/-0.8 LSB as shown in Figure 6. The adaptation transient is shown in Figure 7. In fewer than 100 000 conversions, calibration has converged to sufficient accuracy for noise-floor-limited performance from the ADC. This represents a better than two orders-of-magntiude improvement in convergence time over [1].

Table 1. System simulation parameters

PARAMETER		VALUE
Input full scale range	V_{FS}	±1.5 V
Residue Amplifier Gain	G	6.13
Initial Gain Estimate		6.05
Amplifier Nonlinearity Parameter	α	0.133
Initial Nonlinearity Estimate		0
Differential pair overdrive bias	V_{OV}	0.25 V
LMS parameter	μ	1/256
Conversions per matrix iteration group		32
Sub-ADC transition level error range		±10 mV
Input Referred Noise		-86 dBFS

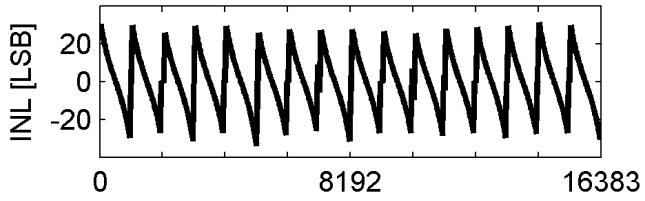

Fig. 5. Integral nonlinearity, uncalibrated.

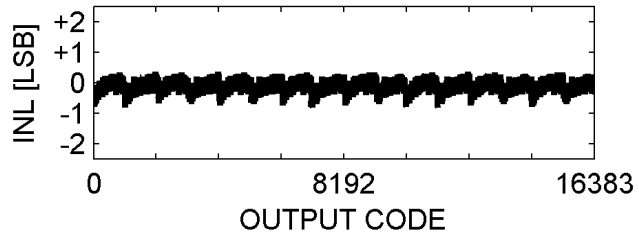

Fig. 6. Integral nonlinearity, calibrated.

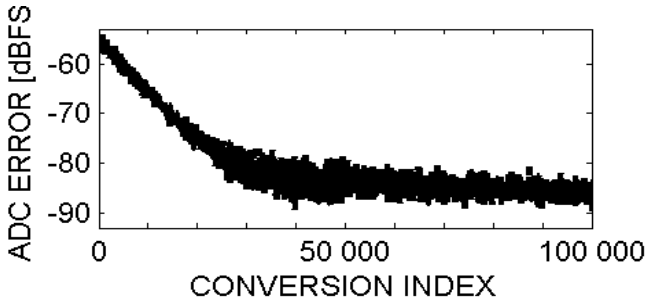

Fig. 7. Convergence of ADC error vs. conversion index.

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