# B1L-A.4 "Split-ADC" Digital Background Correction of Open-Loop Residue Amplifier Nonlinearity Errors in a 14b Pipeline ADC

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# Outline

- Background
  - –Goals
  - –Pipeline ADC Review
  - –Previous Self-Calibration Techniques
- "Split ADC" Architecture
  - –Area / Noise / Speed / Power Implications
  - –Design Details
  - –Results
- Conclusion

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# Goals

## General: Take advantage of CMOS scaling

- Digital
  - Relax requirements on analog precision
  - All calibration / complexity in digital domain
- Background
  - Calibration continuous in background
- Deterministic
  - Short time constant for adaptation
  - No requirements on input signal behavior

## Specific Implementation:
## 14b Pipeline ADC

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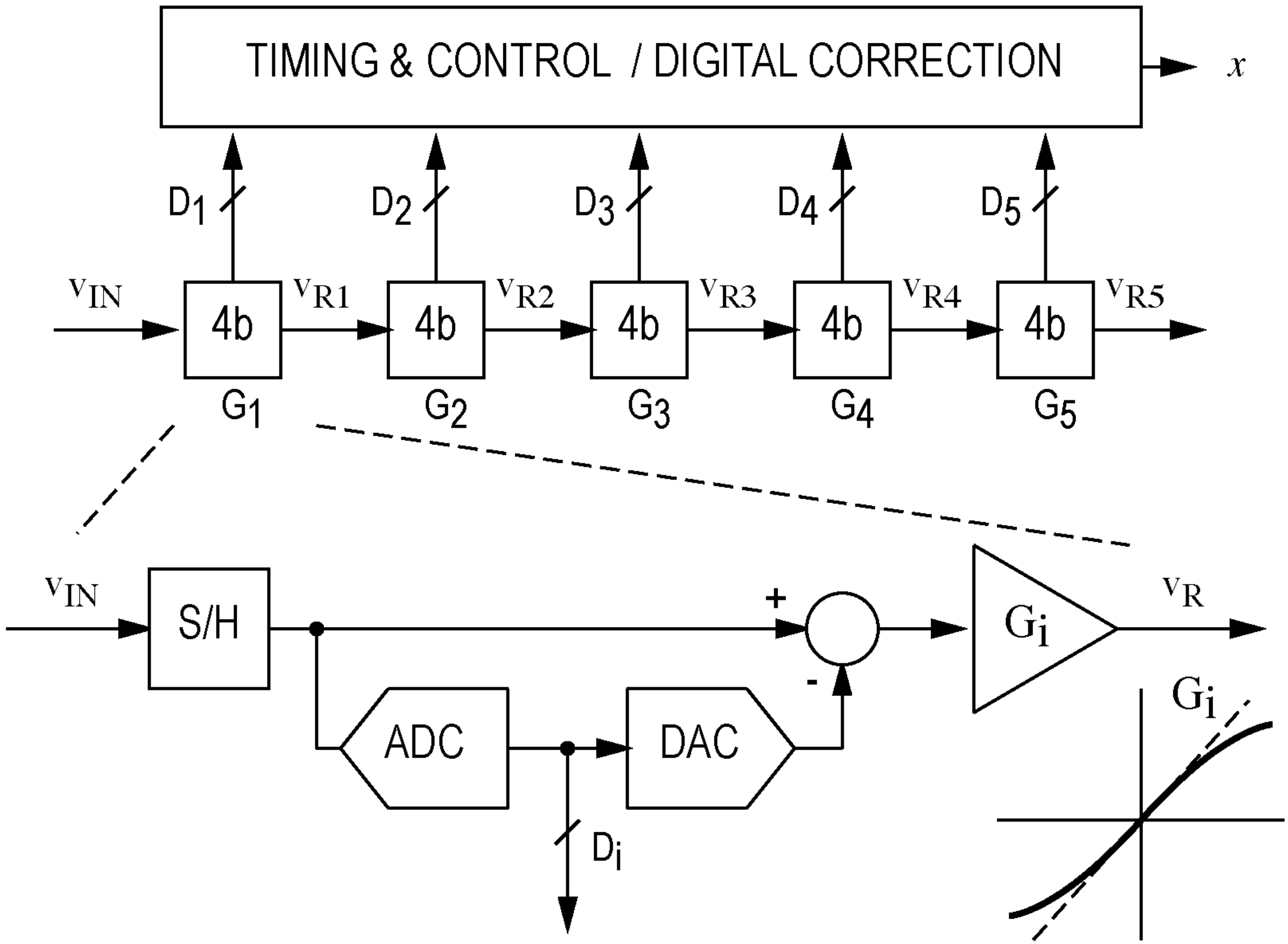
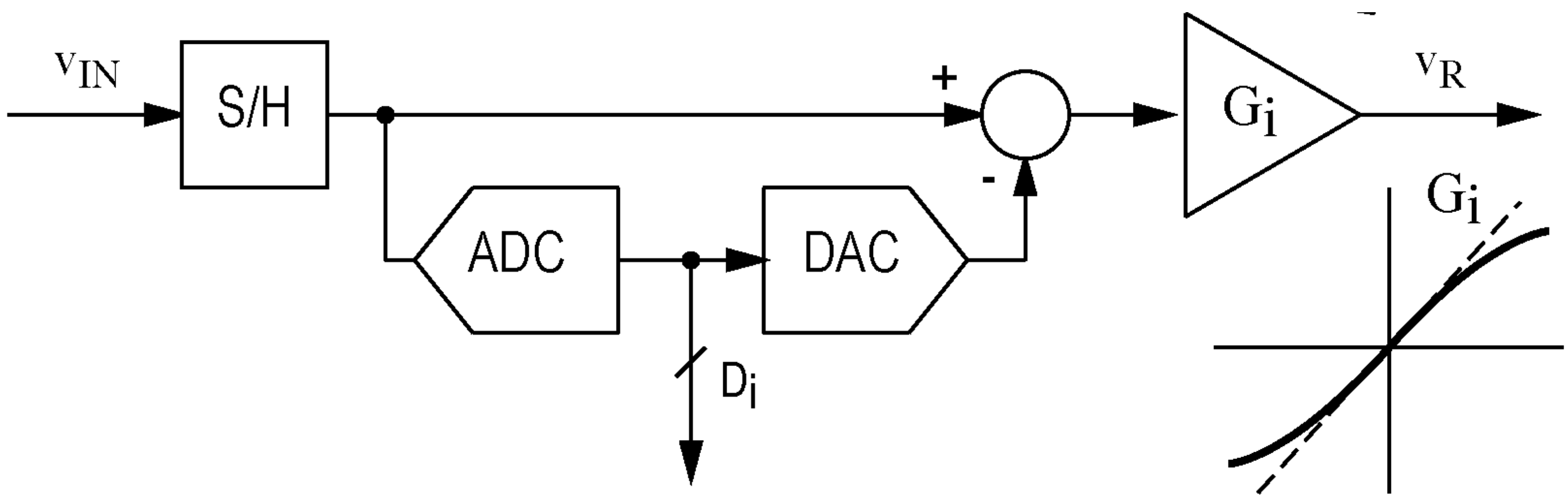
# Pipeline ADC Review



# Residue Expression

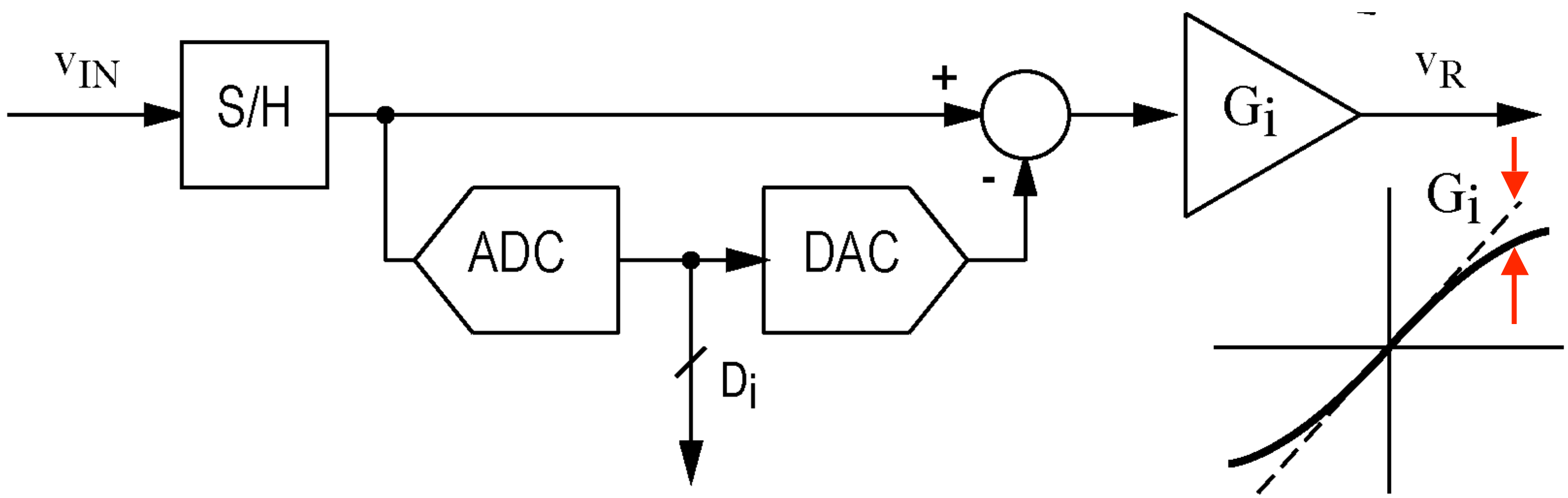
- **Linear gain:** $v_R = G_i\left(v_{IN} - D_i \cdot V_{REF}\right)$



# Residue Expression

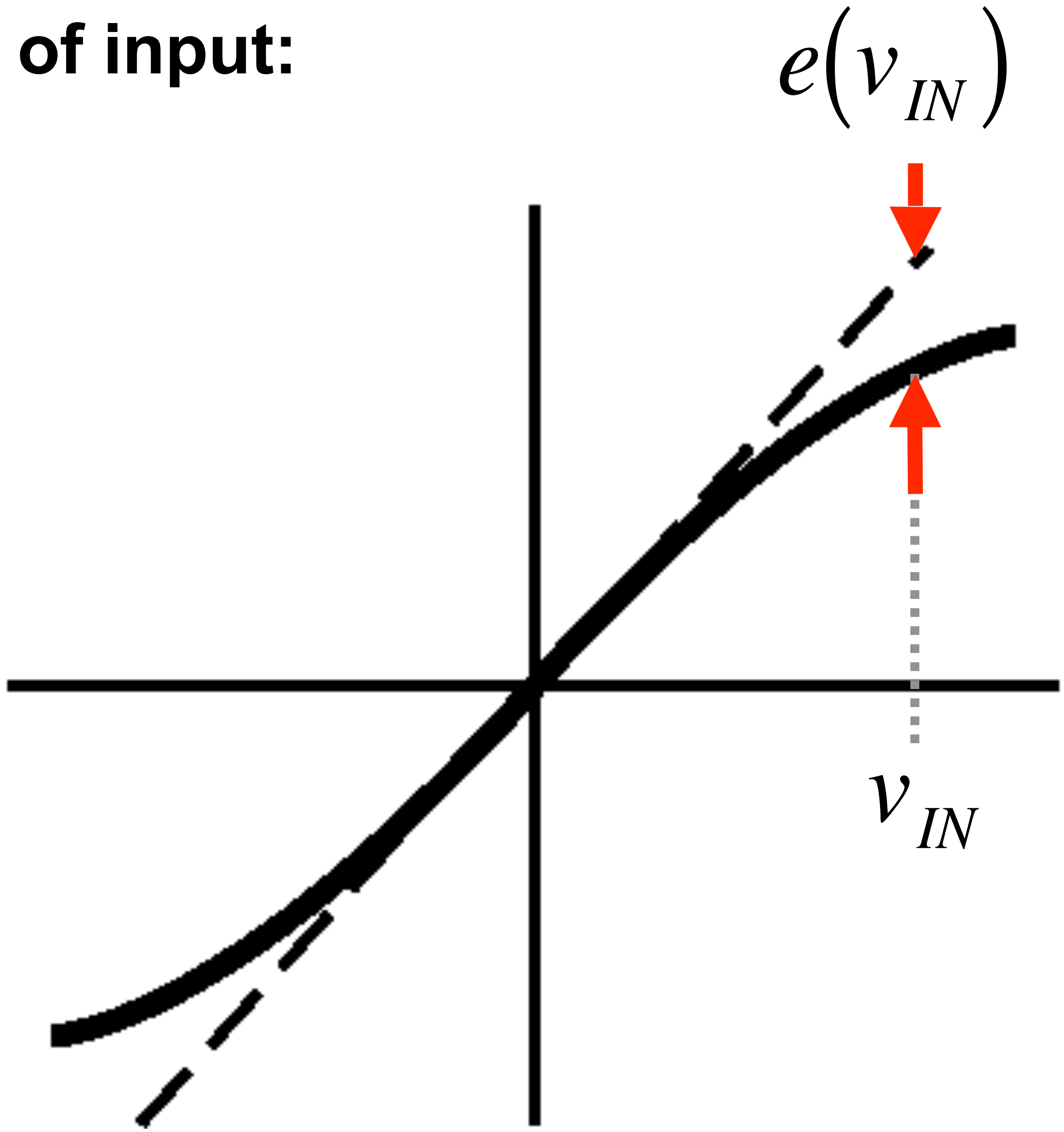
- **Linear gain:** $v_R = G_i\left(v_{IN} - D_i \cdot V_{REF}\right)$

- **Nonlinearity error:** $v_R = G_i\left(v_{IN} - D_i \cdot V_{REF}\right) - e$



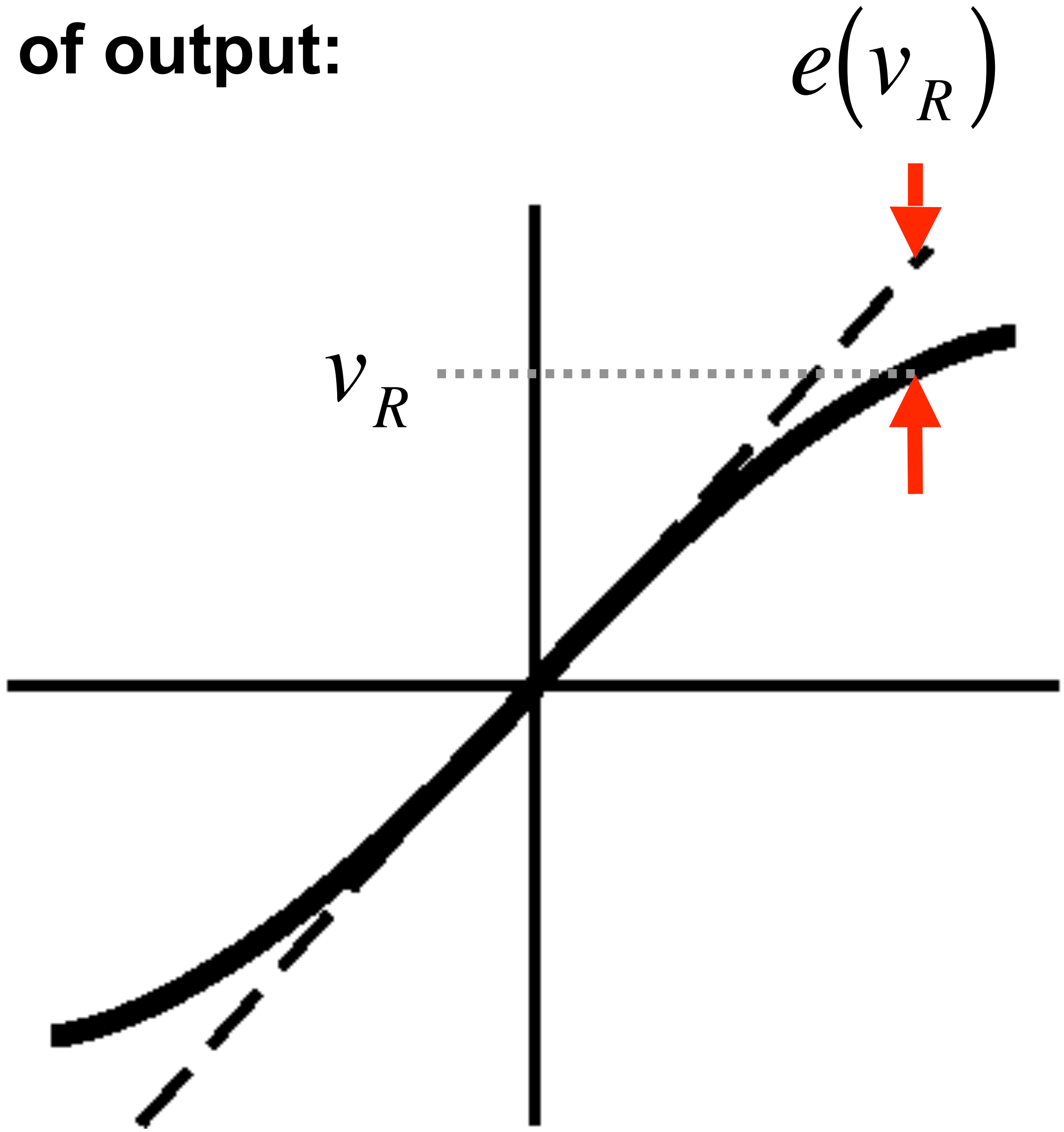
# Nonlinearity Error

- **Function of input:**



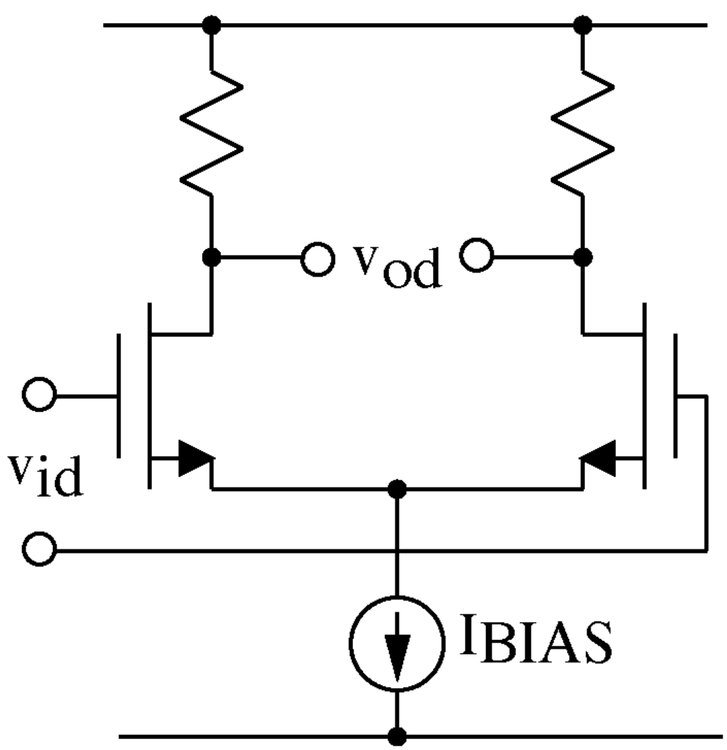
# Nonlinearity Error

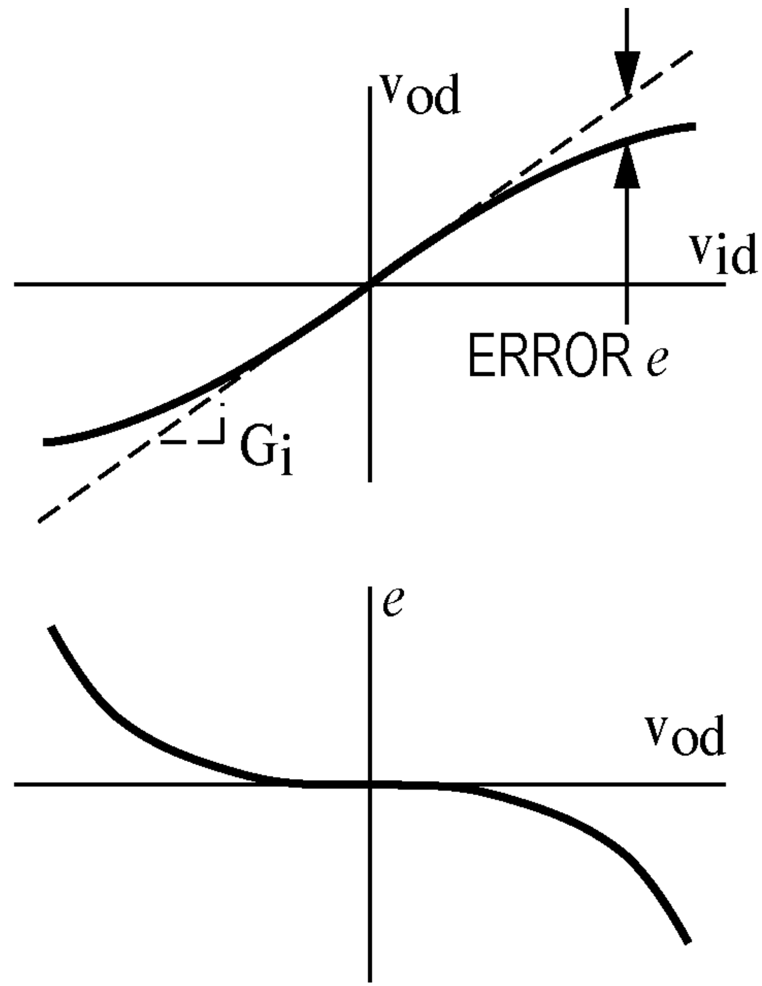
- **Function of output:**



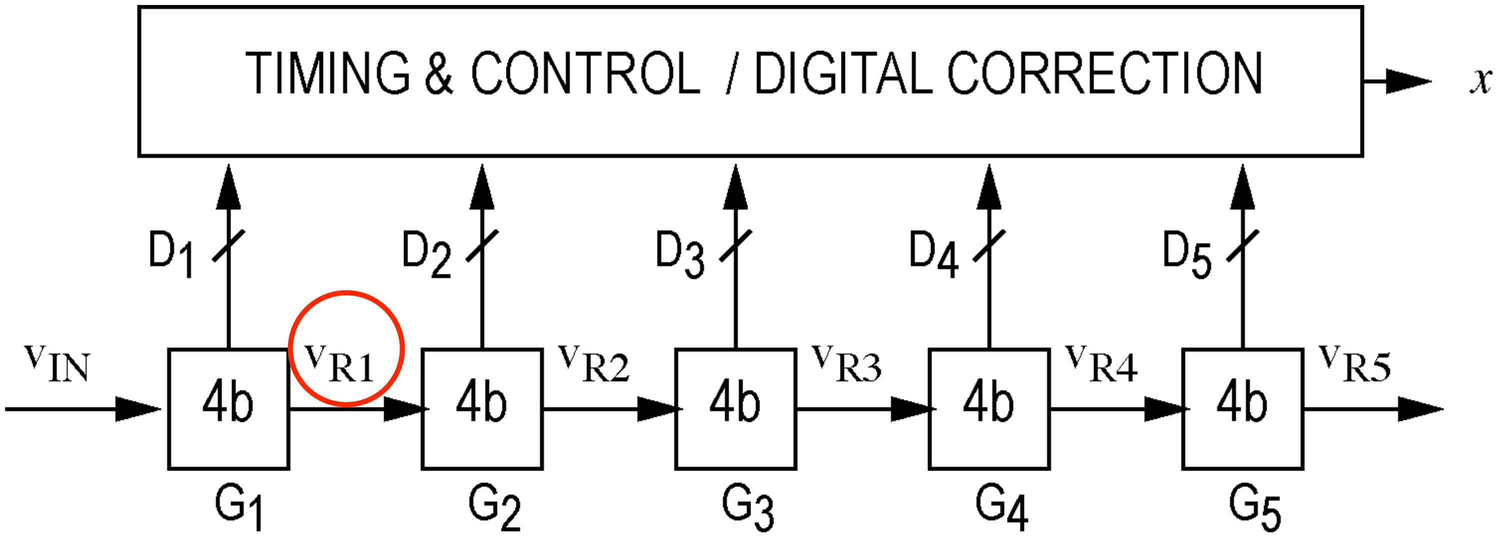
# Open-Loop Differential Pair

- **Nonlinearity error:**



# Pipeline ADC Review

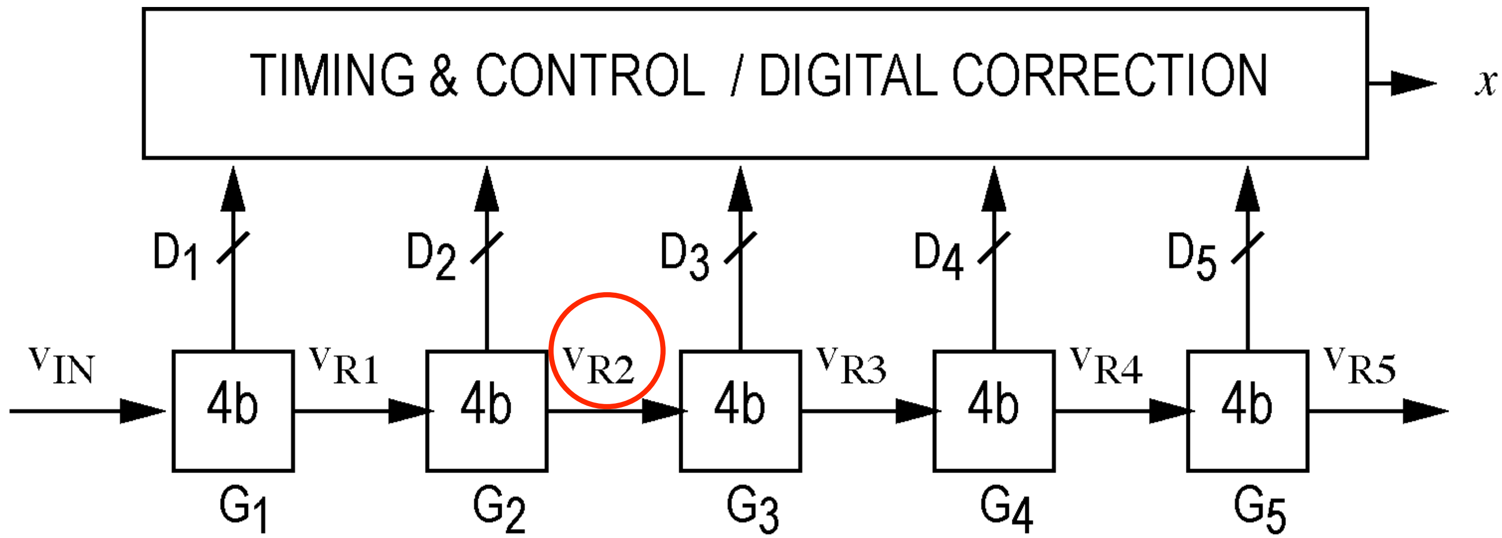



- **Residue 1**

$$v_{R1} = G_1\left(v_{IN} - D_1 \cdot V_{REF}\right)$$

**(assumes linear gain)**

# Pipeline ADC Review

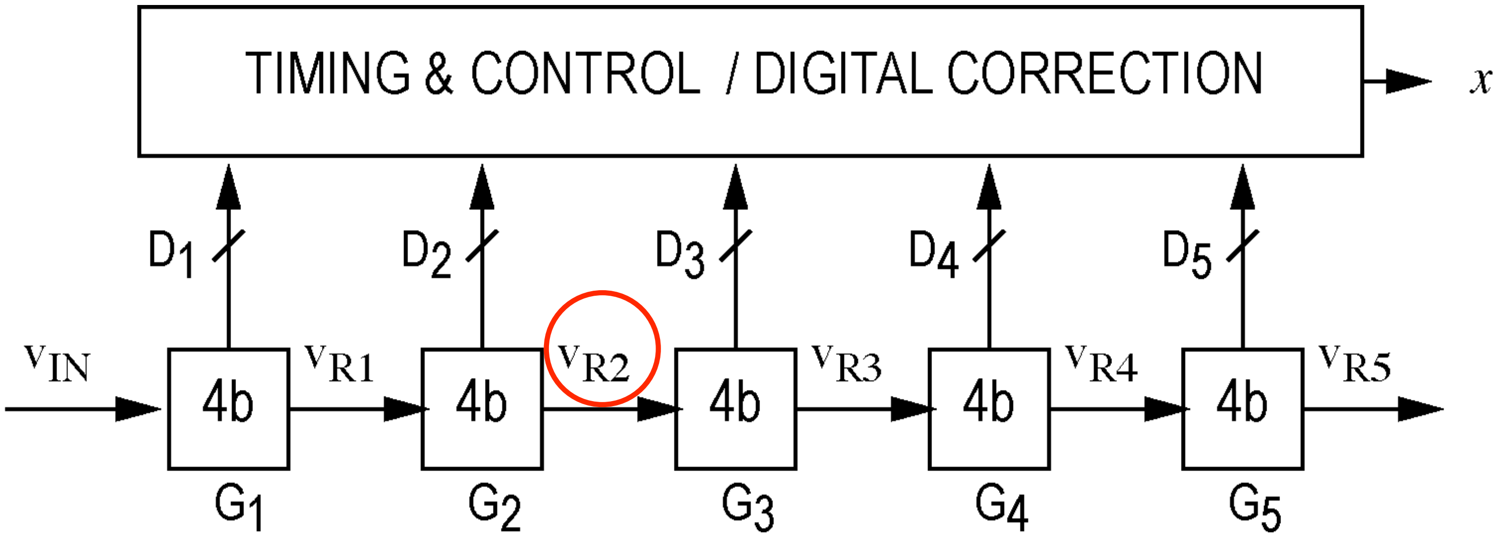



- **Residue 2**

$$v_{R2} = G_2\left(v_{R1} - D_2 \cdot V_{REF}\right)$$

$$v_{R2} = G_2\left(\left[G_1\left(v_{IN} - D_1 \cdot V_{REF}\right)\right] - D_2 \cdot V_{REF}\right)$$

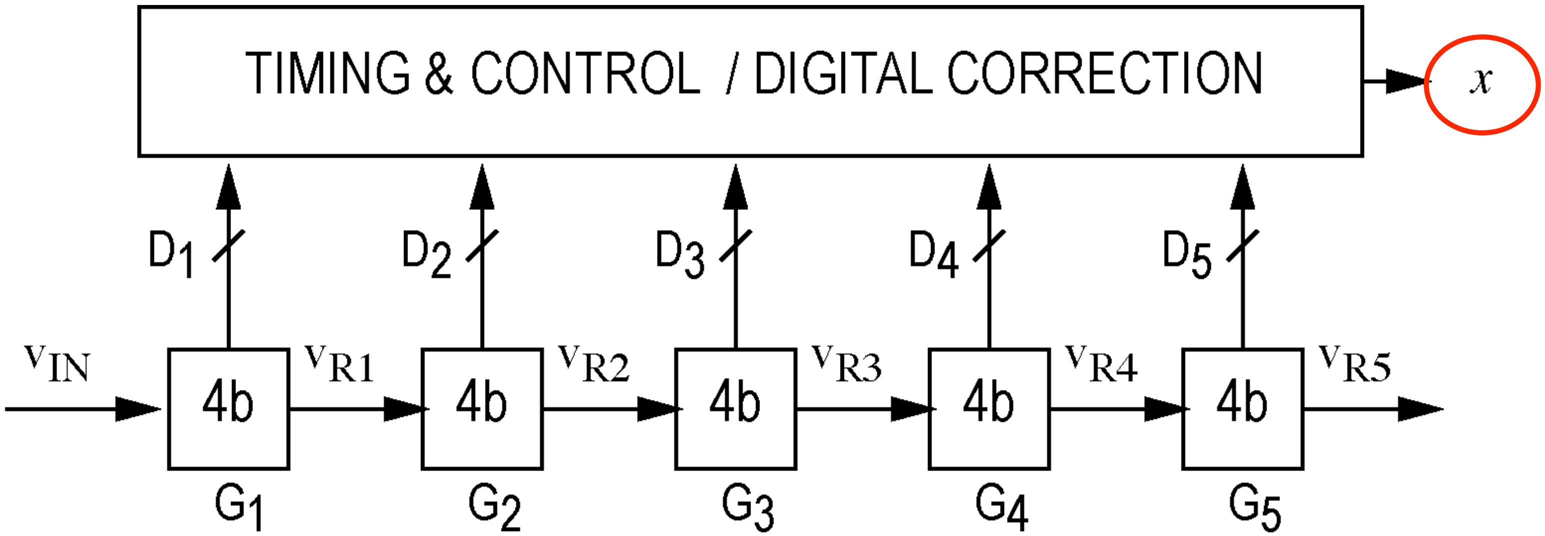
# Pipeline ADC Review




- **Solve for** $v_{IN} / V_{REF}$

$$\frac{v_{IN}}{V_{REF}} = \underbrace{D_1 + \frac{1}{G_2 \cdot G_1} D_2}_{\substack{OUTPUT \quad CODE \\ x}} + \underbrace{\frac{1}{G_2 \cdot G_1} v_{R2}}_{\substack{QUANTIZATION \\ ERROR}}$$

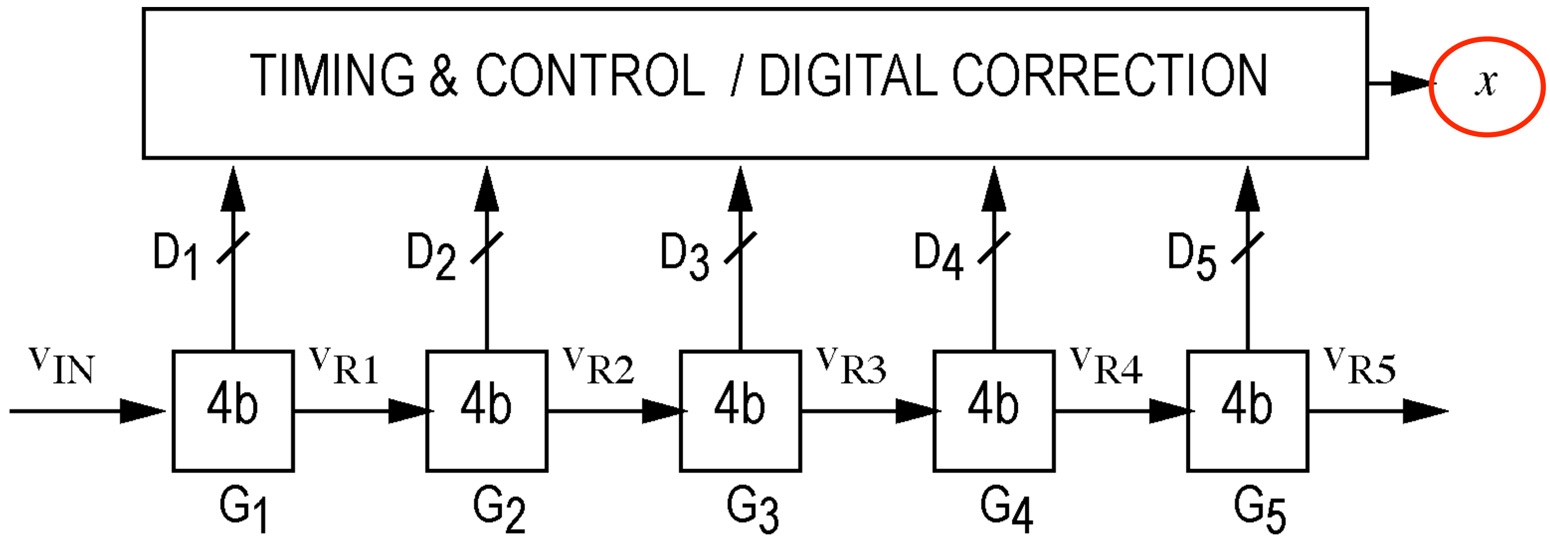
# Pipeline ADC Review




- **All stage results:**

$$x = D_1 + \frac{1}{G_1} D_2 + \frac{1}{G_1 G_2} D_3 + \frac{1}{G_1 G_2 G_3} D_4 + \frac{1}{G_1 G_2 G_3 G_4} D_5$$

# Pipeline ADC Review




- $D_b$: Result of "back end" digitizing $v_{R1}$

$$x = D_1 + \frac{1}{G_1}\underbrace{\left(D_2 + \frac{1}{G_2}D_3 + \frac{1}{G_2G_3}D_4 + \frac{1}{G_2G_3G_4}D_5\right)}_{D_b}$$

# Digital Correction: Gain

- $D_b$: Result of "back end" digitizing $v_{R1}$

$$x = D_1 + \frac{1}{\hat{G}_1} D_b$$

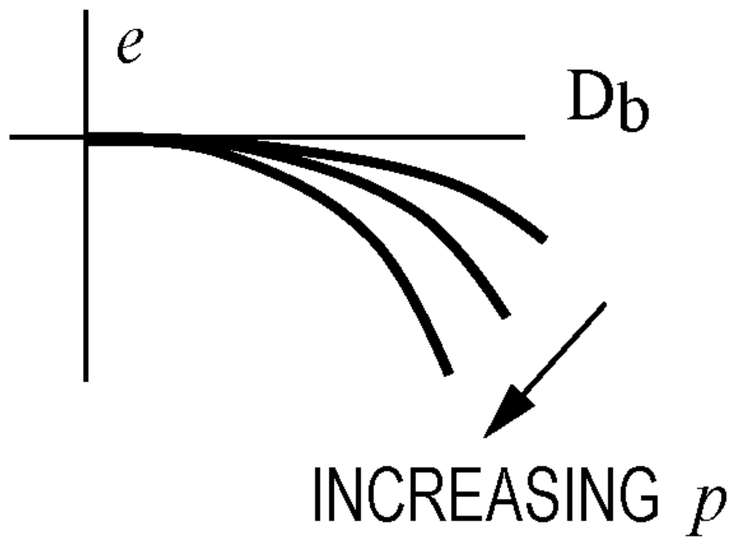
- $\hat{G}_1$: Digital estimate of analog gain $G_1$

# Digital Correction: Nonlinearity

- $D_b$: Result of "back end" digitizing $v_{R1}$

$$x = D_1 + \frac{1}{\hat{G}_1} D_b + e\left(\hat{p}_1, D_b\right)$$

- $\hat{p}_1$ : Estimate of nonlinearity parameter $p_1$




Murmann ..., "A 12b 75MS/s Pipelined ADC using open-loop residue amplification," ISSCC2003

# Digital Calibration

- $D_b$: Result of "back end" digitizing $v_{R1}$

$$x = D_1 + \frac{1}{\hat{G}_1} D_b + e\left(\hat{p}_1, D_b\right)$$

**How to estimate $G_1$, $p_1$ …**

- Digitally
- In the background
- Without a known input?

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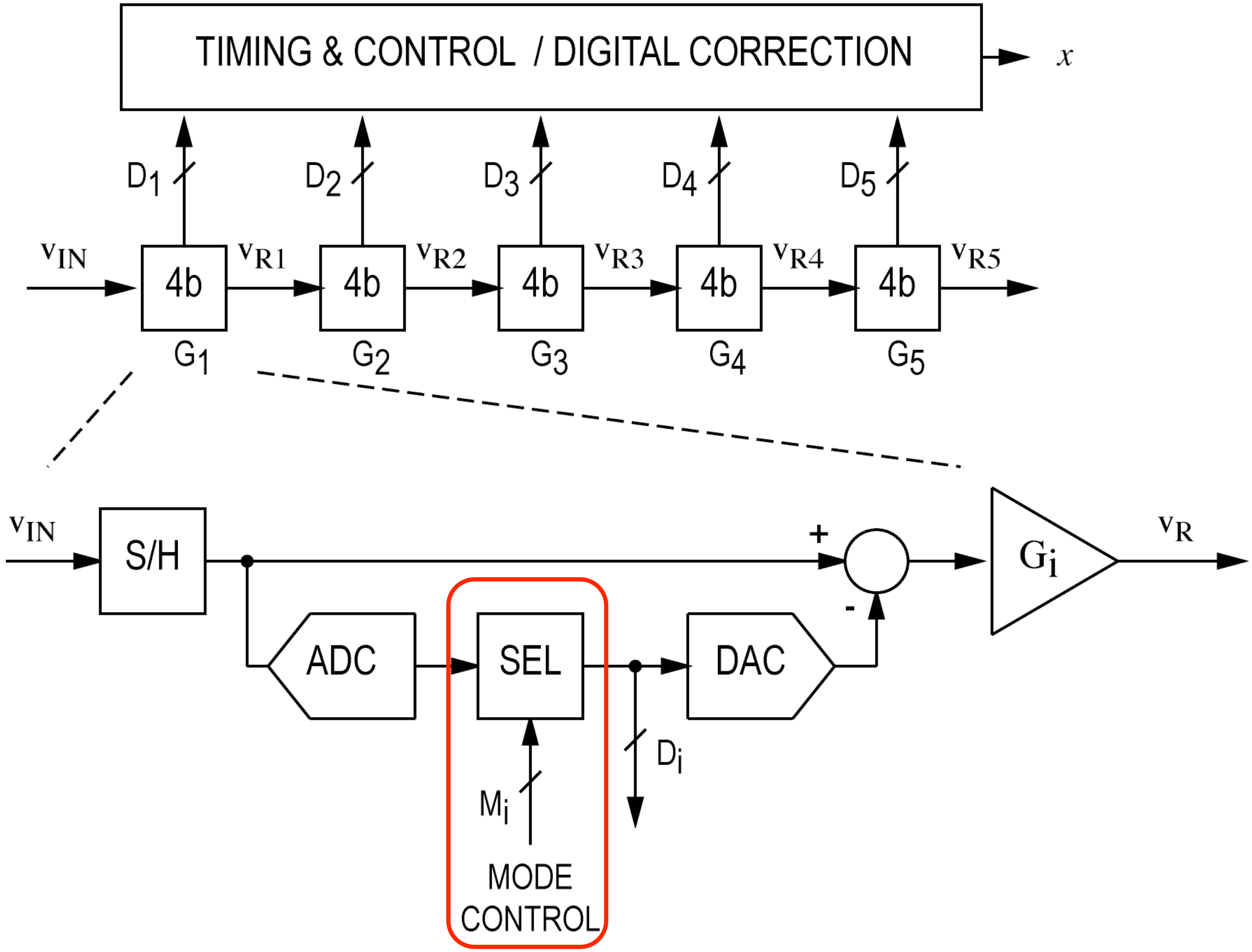
# Previous Work

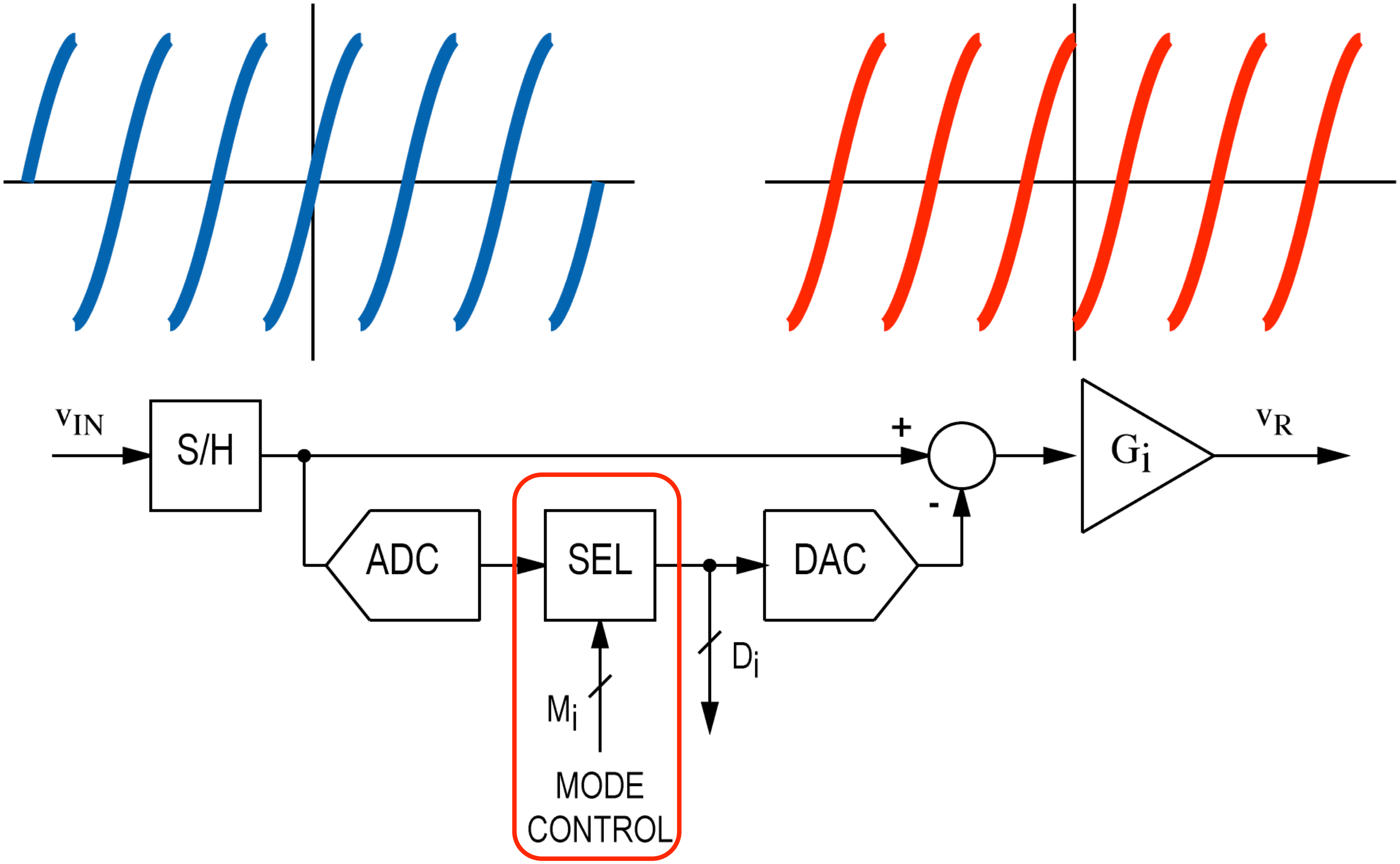
- **Multiple-mode residue amplifier**




**Murmann ..., "A 12b 75MS/s Pipelined ADC using open-loop residue amplification," ISSCC2003**

# Previous Work

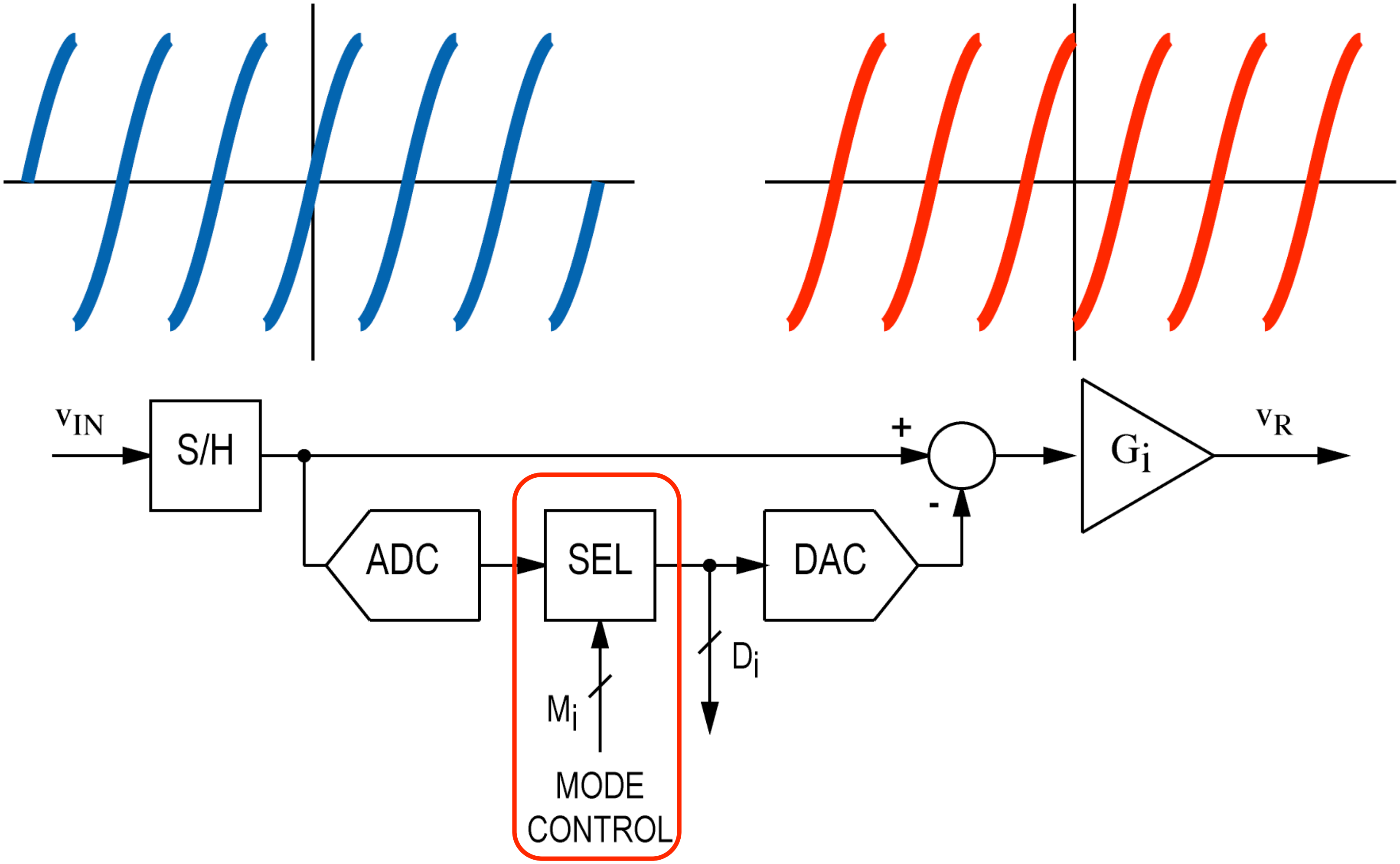
- PR choice between residue amplifier modes
- Compare statistics of results from each mode




Murmann ..., "A 12b 75MS/s Pipelined ADC using open-loop residue amplification," ISSCC2003

# Difficulty

- About $2^{2N}$ samples needed to decorrelate calibration signal from unknown ADC input

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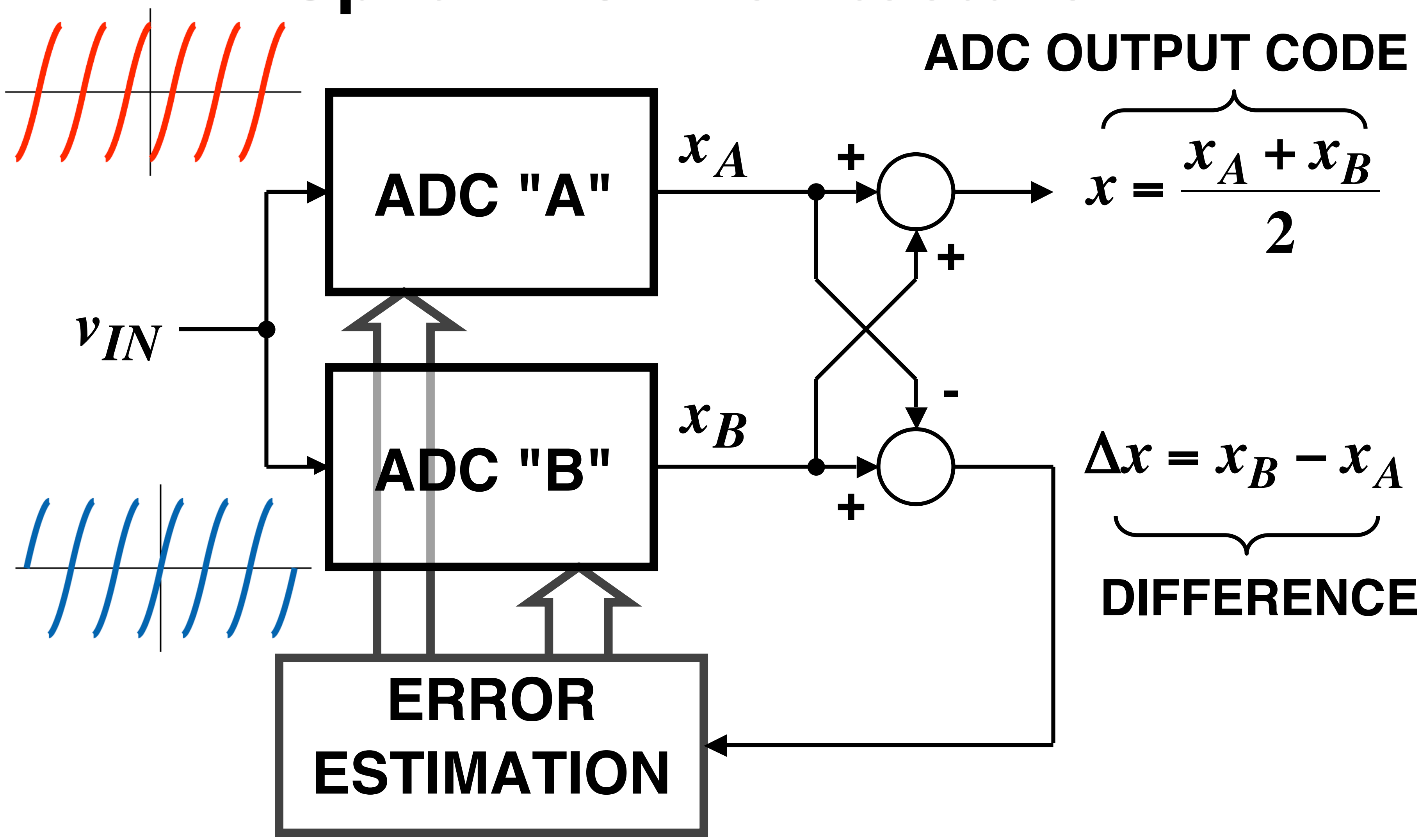
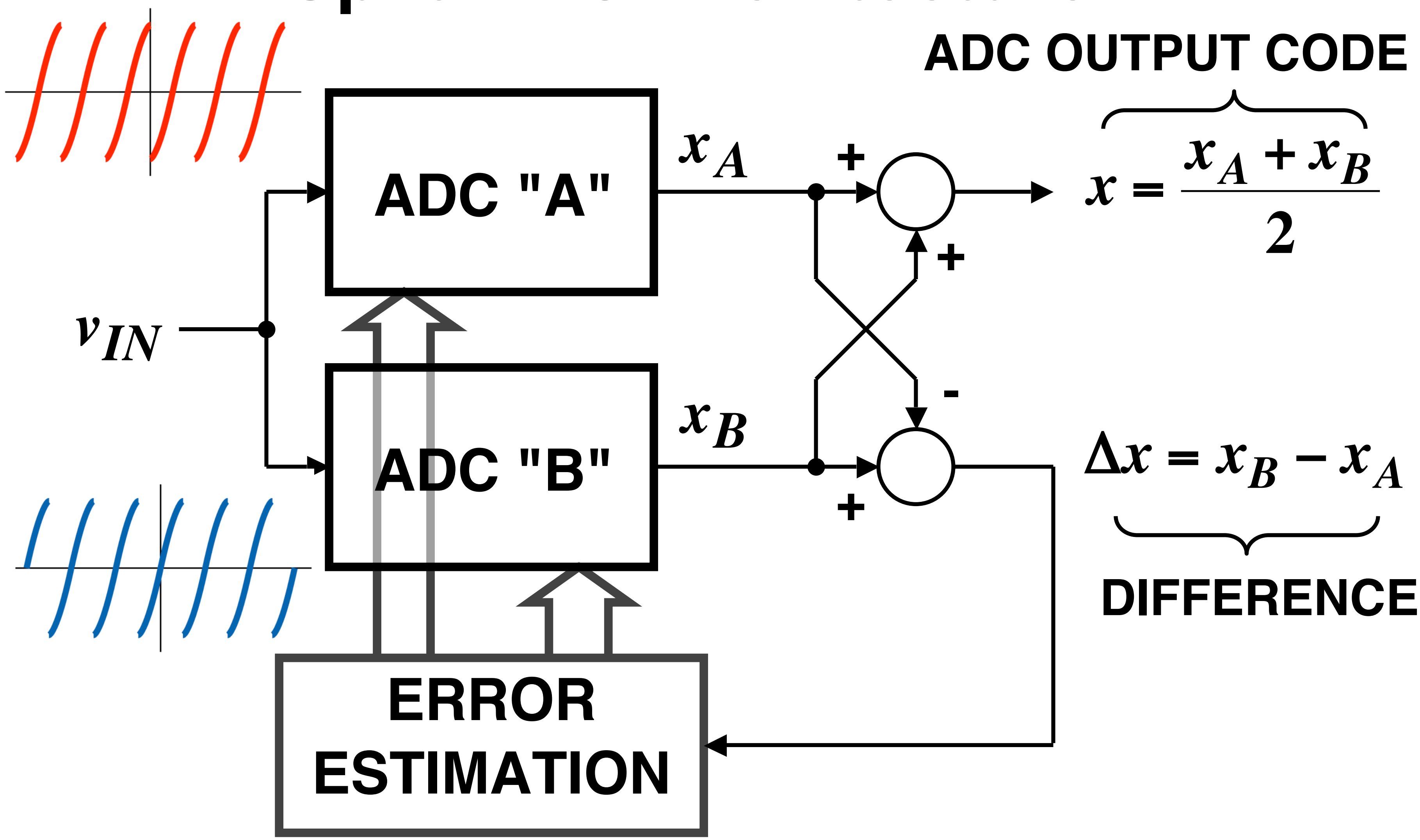
# Split ADC Architecture




- Split ADC into identical halves
- Use different residue mode on each side

# Split ADC Architecture




- Average of A, B results is ADC output code
- Calibration signal developed from difference

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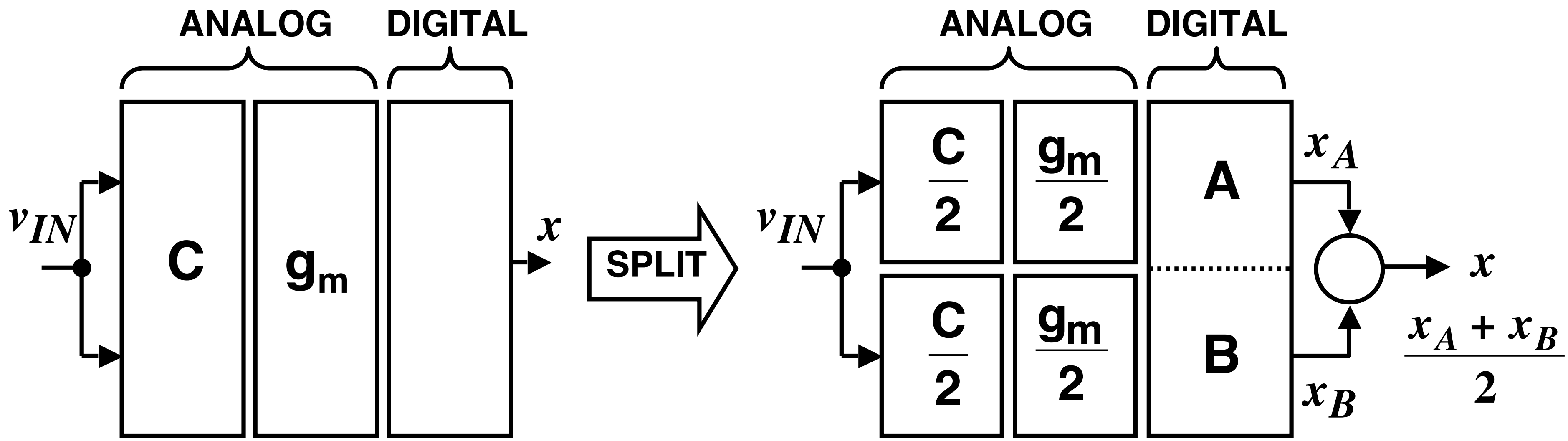
# Same Area, Noise, Speed, Power




| | | |
|---|---|---|
| **Speed** | $f_T = b\left(\frac{g_m}{C}\right)$ | $f_T = b\left(\frac{g_m/2}{C/2}\right) = b\left(\frac{g_m}{C}\right)$ |
| **Power** | $P = p \cdot g_m$ | $P = p \cdot \frac{g_m}{2} + p \cdot \frac{g_m}{2} = p \cdot g_m$ |
| **Noise** | $\sigma_x = n\sqrt{\frac{kT}{C}}$ | $\sigma_x = \sqrt{\left(\frac{1}{2}n\sqrt{\frac{kT}{C/2}}\right)^2 + \left(\frac{1}{2}n\sqrt{\frac{kT}{C/2}}\right)^2} = n\sqrt{\frac{kT}{C}}$ |

- **Negligible impact on analog complexity**

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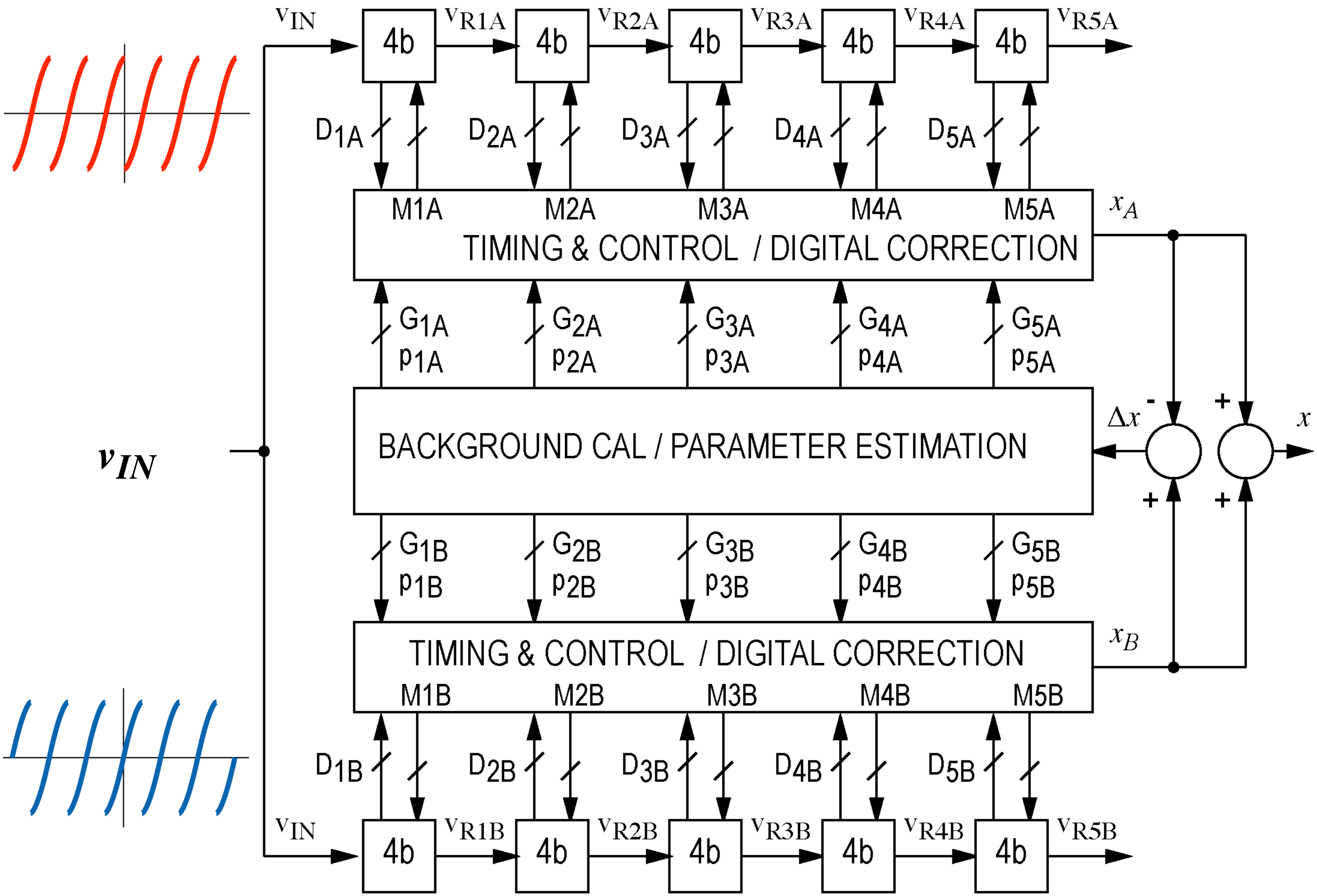
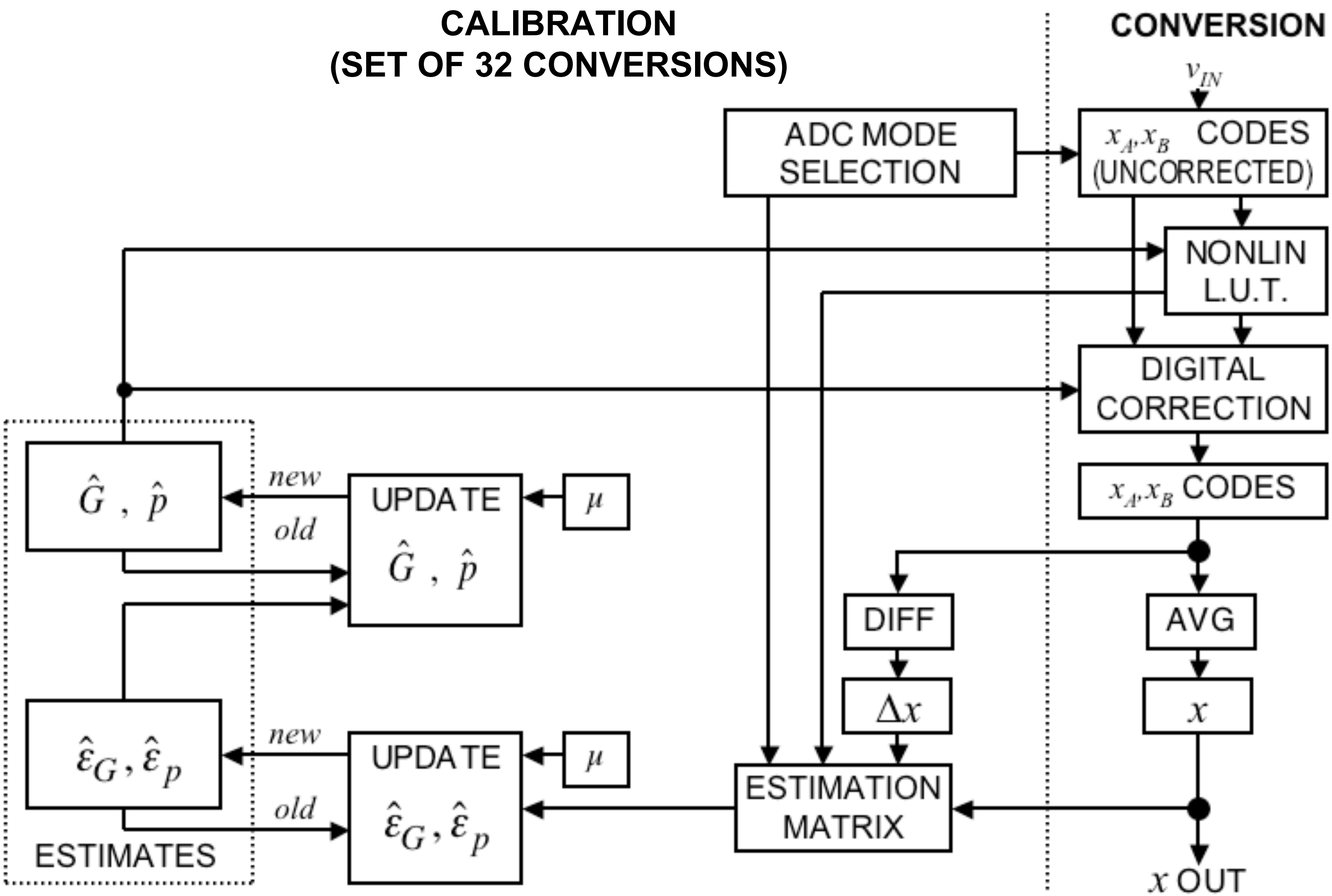
# Block Diagram

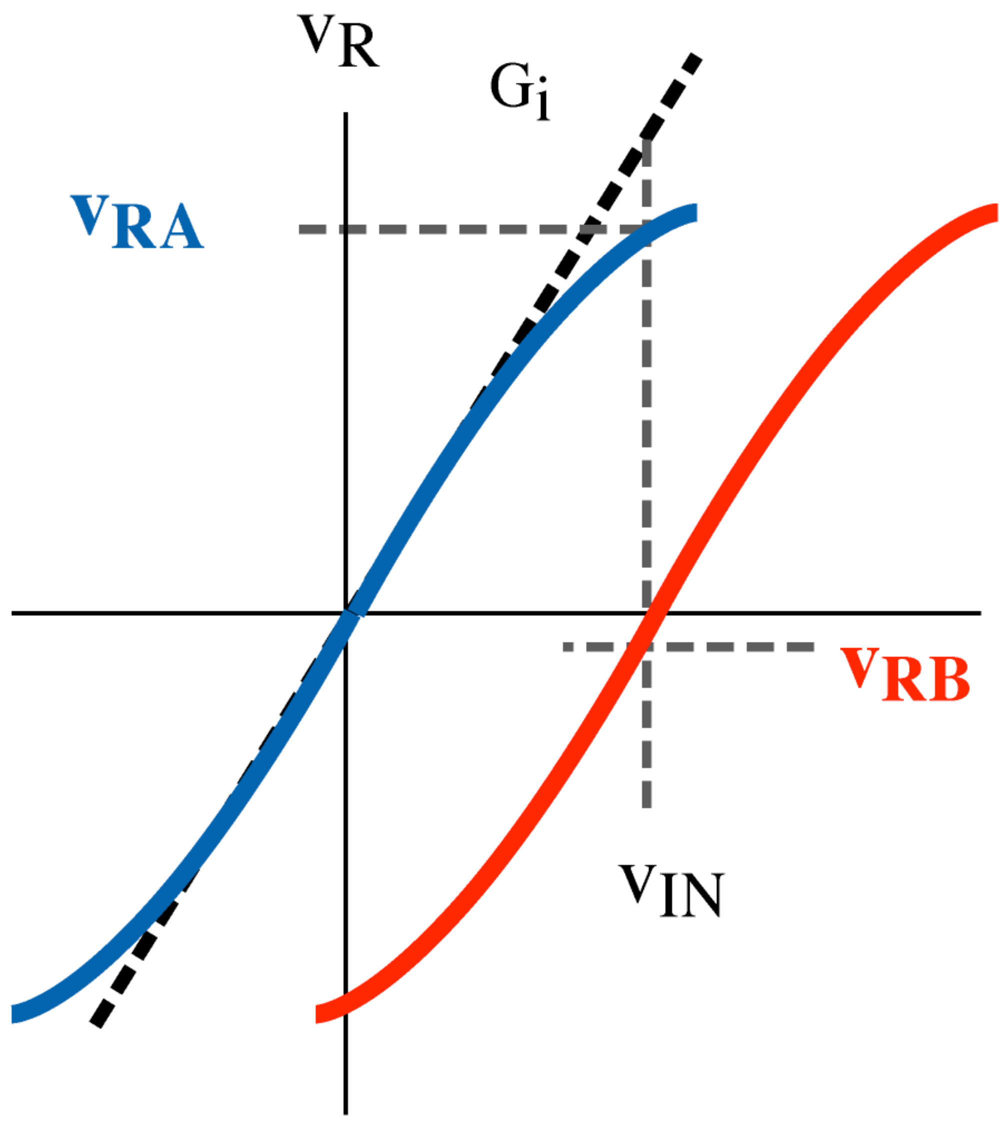


# Digital Correction



# Calibration: Intuitive View

- **A, B residue modes**
- **Larger** $v_{RA} \Rightarrow$ **Corrected code** $x_A$ **more sensitive to nonlinearity**
- **Nonzero** $\Delta x = x_B - x_A \Rightarrow$ **More likely due to error in A parameters** $\Rightarrow$
- **Adjust** $G_{1A}, p_{1A}$



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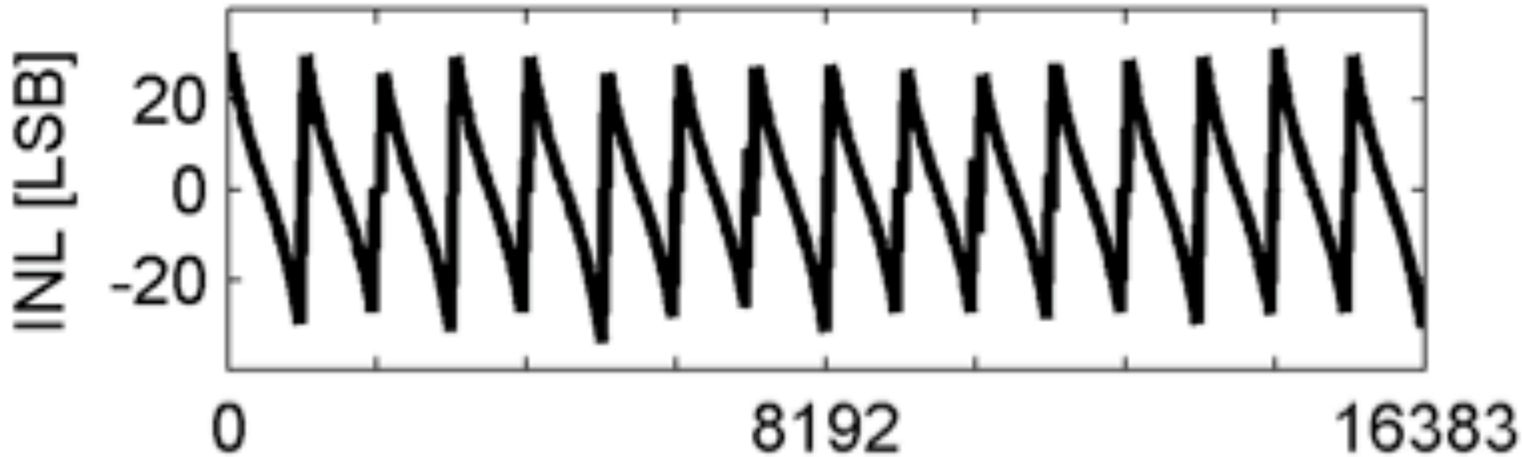
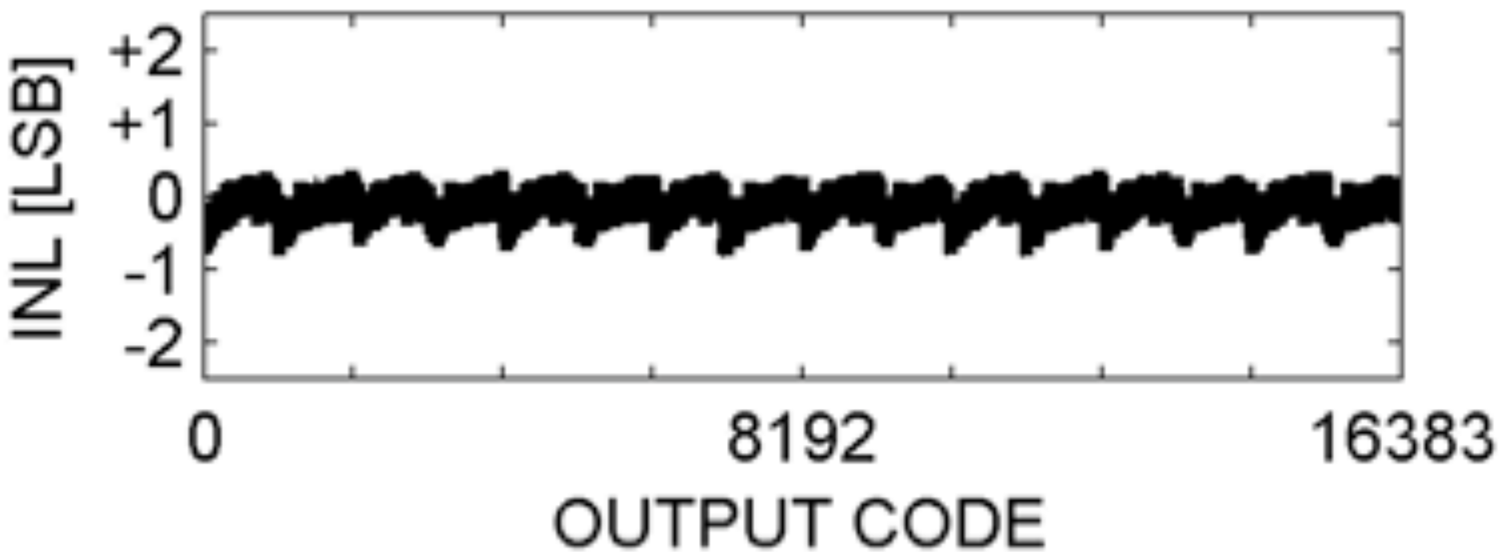
# MATLAB Simulation Parameters

| PARAMETER | | VALUE |
|---|---|---|
| Input full scale range | $V_{FS}$ | ±1.5 V |
| Residue Amplifier Gain | $G$ | 6.13 |
| Initial Gain Estimate | | 6.05 |
| Amplifier Nonlinearity Parameter | $\alpha$ | 0.133 |
| Initial Nonlinearity Estimate | | 0 |
| Differential Pair Overdrive Bias | $V_{OV}$ | 0.25 V |
| LMS Parameter | $\mu$ | 1/256 |
| Conversions per Matrix Iteration Group | | 32 |
| Sub-ADC Transition Level Error Range | | ±10 mV |
| Input Referred Noise | | -86 dBFS |

# Simulated INL

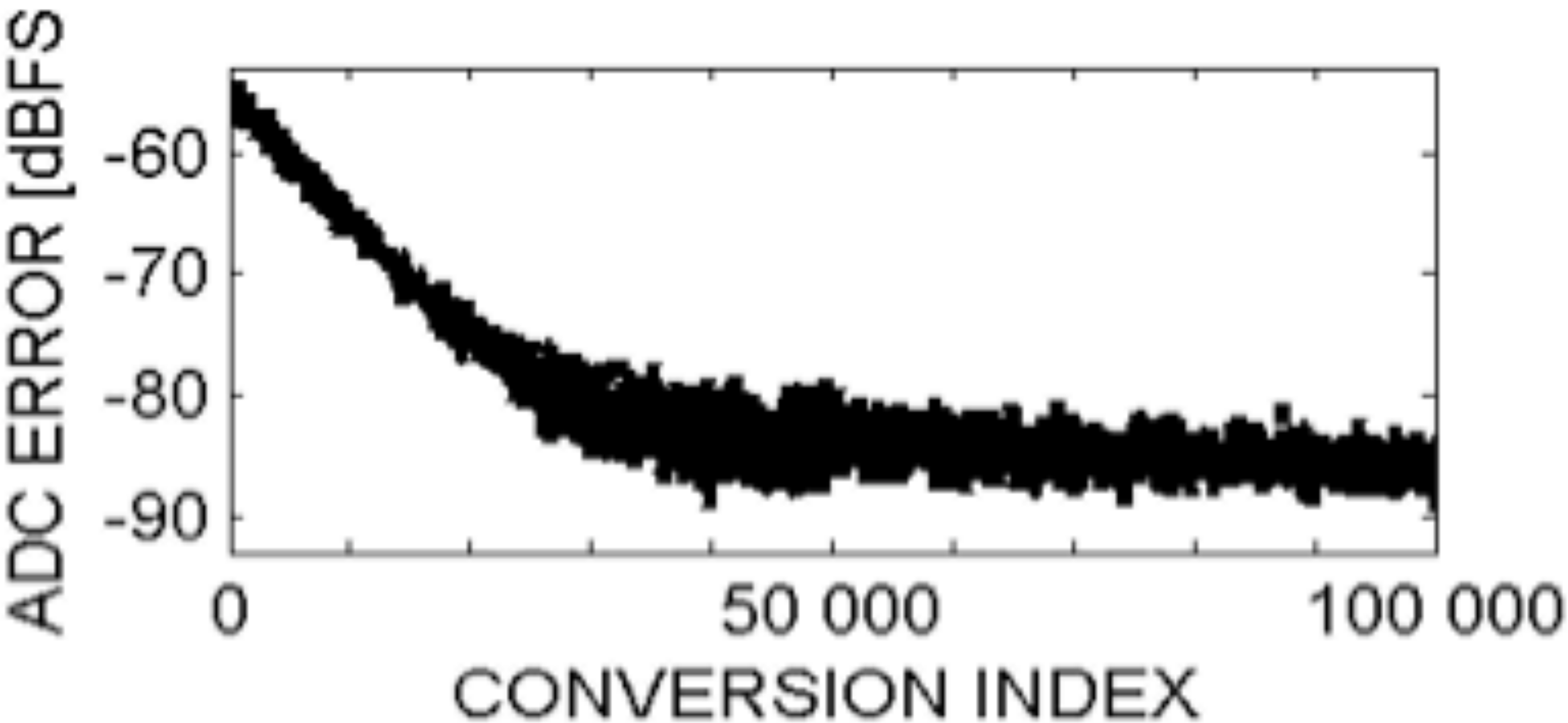



Integral nonlinearity, uncalibrated.




Integral nonlinearity, calibrated.

# Calibration Convergence




- **Long decorrelation times not necessary**

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# Conclusion

- "Split ADC" architecture
  - Average: Output code
  - Difference: Drive to zero to correct errors
  - Deterministic: Converges rapidly
    - Suitable for high resolution ADCs
  - Negligible effect on analog
    Area, power, noise, speed
  - Complexity moved into digital domain
- 14b Pipeline ADC
  - Correct gain, nonlinearity errors
  - Self-calibration in ~ 50,000 conversions

# Acknowledgments


- Analog Devices
  - Precision Nyquist Converters group
  - Michael Coln
  - Brian Larivee
  - Bob Adams
  - Bob Brewer
  - Larry DeVito
  - Paul Ferguson
  - Colin Lyden
  - Katsu Nakamura
  - Richard Schreier
  - Larry Singer
- Stanford University
  - Boris Murmann