# A 50A, 1-μs-RISE-TIME, PROGRAMMABLE ELECTRONIC LOAD INSTRUMENT FOR MEASUREMENT OF MICROPROCESSOR POWER SUPPLY TRANSIENT PERFORMANCE

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**Abstract** - *A prototype instrument has been developed which is capable of providing a transient current of up to 50A with a rise time as low as 1μs. The minimum current, maximum current, and rise time are digitally programmable. This instrument, which simulates the transient current loads drawn by a high-speed microprocessor, allows measurement of the transient performance of switch-mode power supplies designed for use in PC systems. The frequency and duty cycle of the load transient waveform is determined by a digital input signal.*

## I. Introduction

In recent years, as the microprocessor has undergone a rapid evolution in design and performance, the requirements on power supplies for these microprocessors have become more demanding [1]. The most recent generation of microprocessors require power supplies that can produce tens of amperes of current, as well as transient currents (when the operating mode of the processor changes) as large as 50A in 1μs. Since standard electronic load test instrumentation at these large currents is capable of rise times no less than approximately 10μs [2], an order-of-magnitude improvement over existing capabilities is necessary to test power supplies designed for microprocessor applications.

The instrument described in this paper is a programmable load that simulates the conditions that an actual microprocessor would impose on the power supply, including current transients of up to 50A with rise time less than 1μs.

This paper is organized as follows: Section II covers the development of the instrument requirements. Section III describes the principal engineering challenges associated with the specification requirements. Section IV covers the system design at the block diagram level, with a discussion of architecture choices within each of the blocks. Experimental results are presented in Section V.

## II. Instrument Requirements

The specifications for this instrument were determined by the performance requirements of the power supplies to be tested. Figure 1 shows the required current transient waveform. For the microprocessor application, the power supply must be capable of a maximum transient current $I_{TRAN}$ of up to 50A. The minimum constant current $I_{MIN}$ ranges from 1 to 5A. The rise time $t_R$ and fall time $t_F$ can be as short as 1μs. Compliance voltage requirements for the transient current source are determined by the microprocessor power supply voltage, which ranges from 1.1V to 1.85V.

For the design of the test instrument, the transient current $I_{TRAN}$ and the minimum current $I_{MIN}$ are digitally programmable by the user, allowing for flexible application. The rise time $t_R$ is also digitally programmable (for simplicity of design in this prototype implementation, the rise and fall times are nominally equal). The timing of the transient current pulse is determined by an external square wave applied by the user. The instrument is capable of operating at a repetition frequency from DC to 100kHz with a duty cycle variable from 10% to 90%. For ease of testing, the compliance range of the transient current source extends to –0.1V. This allows the transient current source to be tested on a stand-alone basis, with the output connected to ground through a current sensing resistance.

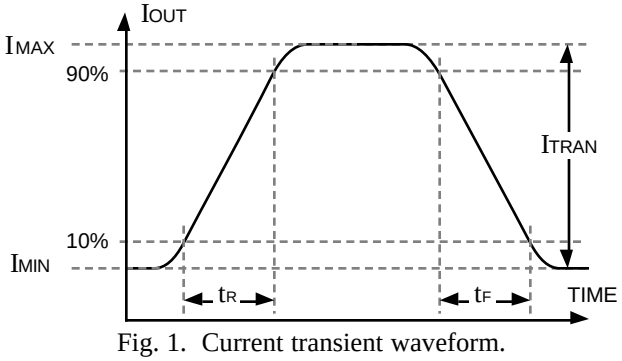


Fig. 1. Current transient waveform.

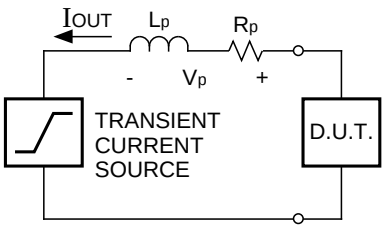


Fig. 2. Parasitic L / R model.

## III. Challenges

The specification requirements represent several engineering challenges for the design of the instrument.

### A. Inductance

A 50A current transient with a rise time of 1µs represents a large dI/dt which can create a significant voltage drop in any parasitic inductance in the transient current path, both in the test instrument and in connections to the power supply device under test. Similarly, at high current levels, even a small amount of parasitic series resistance results in an appreciable voltage drop, thus introducing difficulty in monitoring and controlling the output current.

As can be seen from Figure 2, for a transient output current $I_{OUT}$, the total voltage drop due to parasitic inductance $L_P$ and parasitic resistance $R_P$ is

$$V_P = L_P \frac{dI_{OUT}}{dt} + I_{OUT} R_P \tag{1}$$

To maintain reasonable voltage compliance requirements on the transient current source, a total parasitic voltage drop of $V_P$=500mV was chosen as the initial system design target. Budgeting an equal distribution of no more than 250mV to each of the resistive and inductive components of $V_P$ in (1) gives maximum target values of $L_P$ and $R_P$ as follows

$$L_P \frac{50A}{1\mu s} \le 0.25V \Rightarrow L_P \le 5nHy \tag{2}$$

$$50A \cdot R_P \le 0.25V \Rightarrow R_P \le 5m\Omega \tag{3}$$

Achieving these extremely low values required careful physical design of the prototype printed circuit board. The problem of parasitic inductance and resistance also influenced the choice of system architecture, as described in section IV.A.

### B. Power Dissipation

Large quantities of current also introduce power dissipation issues. Figure 3 shows the transient current source

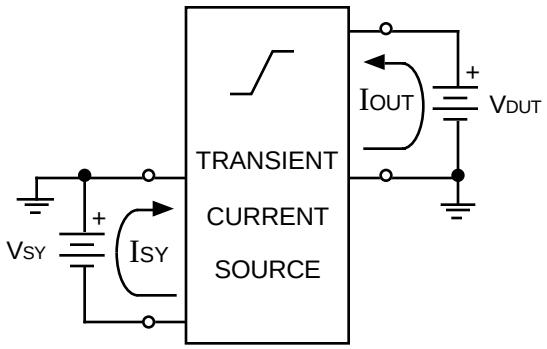


Fig. 3. Power dissipation model.

with its power supply voltage $V_{SY}$. When the output current $I_{OUT}$ flows from the DUT, the associated current from the instrument's $V_{SY}$ supply is $I_{SY}$. The total power dissipated by the instrument will be

$$P = I_{SY} \cdot V_{SY} + I_{OUT} \cdot V_{DUT} \tag{4}$$

Compliance voltage considerations for the transient current source required a 5V power supply for $V_{SY}$. In the worst case when $V_{DUT}$=+1.85V and $I_{OUT}$=$I_{SY}$=50A, the total power dissipation is

$$P = 50A \cdot 5V + 50A \cdot 1.85V = 343W \tag{5}$$

This large power dissipation influenced the choice of system architecture, as described in section IV.B.

## IV. System Design

Figure 4 shows the system level block diagram. The total output current is the sum of a constant programmable current and the transient current. The transient current is realized as the sum of eight current source stages operating in parallel. Within each stage, a constant programmable current is steered by a MOSFET differential pair. The rise time of the output current is controlled by the slope of the differential voltage signal at the input of the MOSFET differential pair. The design choices that led to this system architecture are described in this section

### A. Continuous Current vs. Switched Current

One disadvantage of the implemented design is its poor efficiency, since the maximum current $I_{SS}$ always flows whether it is "steered" to the D.U.T. by the MOSFET differential pair or simply "thrown away" to ground. This is shown in simplified form in Figure 5a. The programmable current $I_{SS}$ is determined by MOSFET M1, bias voltage $V_{BIAS}$, and source degeneration resistor $R_S$.

An alternative approach would be to switch the gate of M1, so that current only flows when required by the D.U.T. This is shown in simplified form in Figure 5b.

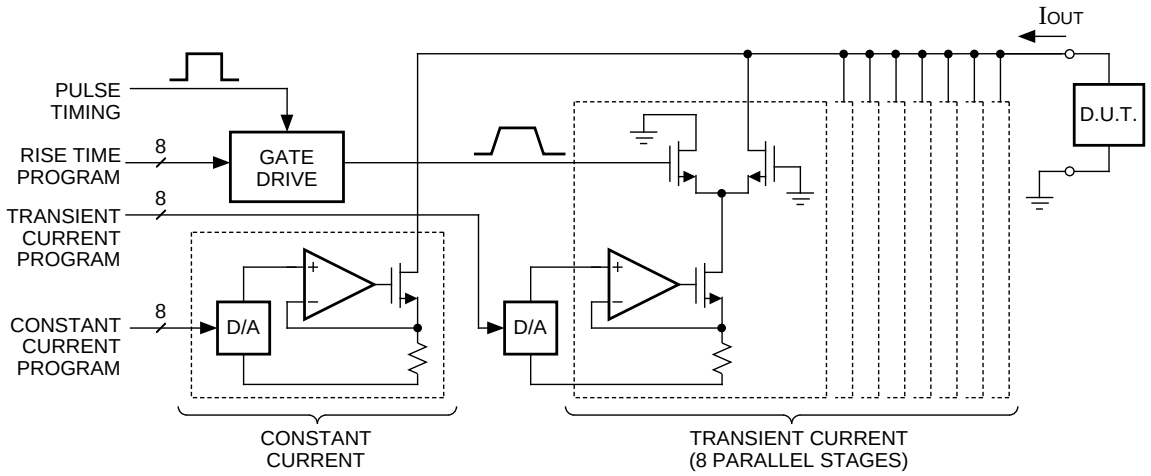


Fig. 4. System block diagram.

Although this approach would improve efficiency, there are severe disadvantages in this application:

1) For the transient current path (indicated with heavy lines in Figures 5a and 5b), the physical distance would be longer in Figure 5b. This makes it much more difficult to meet the parasitic resistance and inductance requirements described in section III.A.
2) In the approach in Figure 5b, the instrument power supply $V_{SY}$ would also "see" the transient current, whereas in the approach of Figure 5a, $V_{SY}$ "sees" only a constant current. Thus the requirements on $V_{SY}$ are relaxed in the approach of Figure 5a.
3) The requirements on the quality of the switching signal $V_{GATE}$ are much more difficult in the case of Figure 5b. In the case of Figure 5b, any overshoot or ringing on $V_{GATE}$ will be passed directly to the output current. In the case of Figure 5a, $V_{GATE}$ need only switch the differential pair. Once the linear range of the differential pair is exceeded, any overshoot or ringing on $V_{GATE}$ will have no effect on the output current.

## B. Single vs. Parallel Current Sources

As shown in the block diagram of Figure 4, the total 50A transient current is realized as the sum of 8 transient current sources operating in parallel. The multiple parallel stage approach was chosen for two main reasons:

1) Power dissipation: The continuous current approach described in section IV.A results in significant power dissipation, as quantified in Eq. (5). Dissipating of order 300W in a single stage would require complex and costly heat sinking. With a parallel approach, the large power dissipation of (5) is distributed over many stages, and conventional heat sinks with small cooling fans are practical.

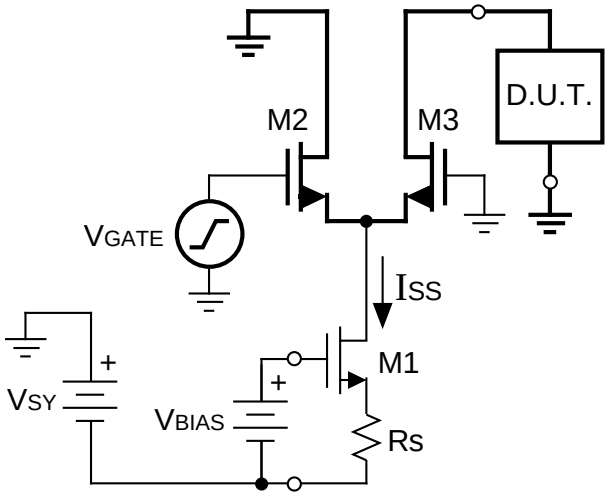


Fig. 5a. Continuous current.

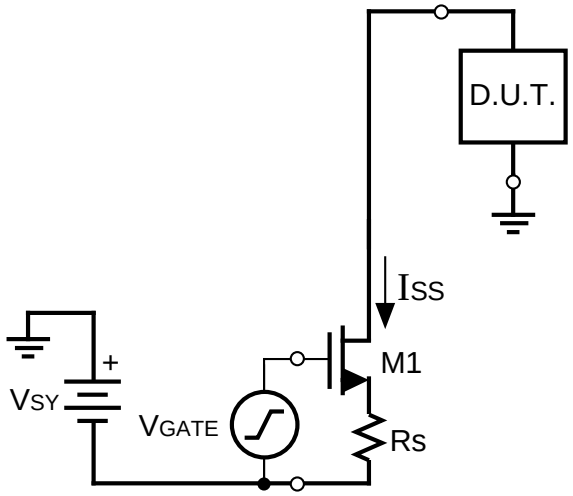


Fig. 5b. Switched current.

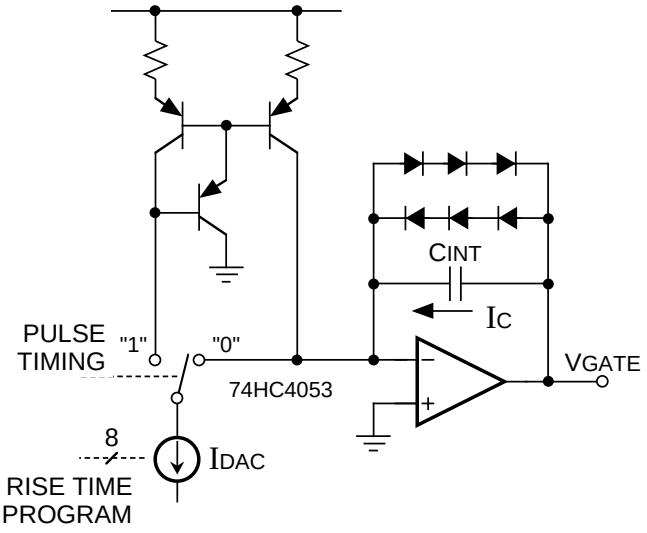


Fig. 6a. Gate drive simplified circuit diagram.

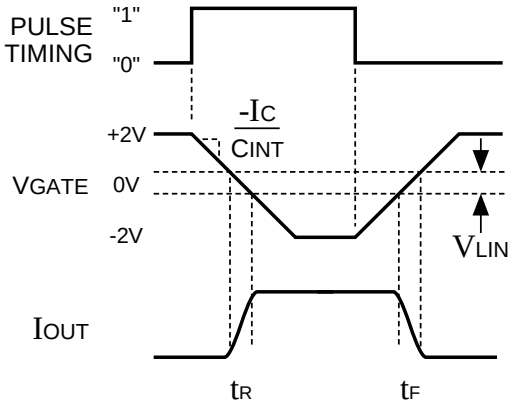


Fig. 6b. Gate drive waveforms.

2) Maximum current: Although there are power MOSFETs able to carry the maximum current of 50A, the selection of devices is limited. The parallel approach with 8 channels requires each channel to carry a maximum current of just over 6A. This lower current allows selection of the power MOSFET from a significantly wider range of devices, allowing better optimization of the price/performance characteristic tradeoff.

## C. Rise Time Programming: Analog vs. Digital

With the differential pair current steering architecture of Figure 5a, the rise time of the output current is determined by the slope of the gate drive signal $V_{GATE}$. For the most complete flexibility, $V_{GATE}$ could be developed using a digital approach, in which the appropriate gate drive waveform for a particular rise time would be calculated in the digital domain (possibly using digital signal processing (DSP) techniques) and converted to an analog $V_{GATE}$ drive waveform using a high speed, high resolution digital-to-analog (D/A) converter. This digital approach offers the possibility of completely arbitrary current waveforms. A preliminary analysis of the D/A requirements to achieve a 1µs programmable rise time indicated conversion speed of order 100MHz, with D/A resolution of order 12 to 16 bits. This level of performance would add significant cost and complexity.

In this system, a simpler analog programming approach was taken. A simplified schematic of the circuit implementation is shown in Figure 6a; the associated waveforms are shown in Figure 6b. The gate drive waveform is developed by a clamped integrator which ramps between voltage limits of approximately ±2V. The slope of the $V_{GATE}$ ramp (which determines the switching speed of the current-steering differential pair) is set by

$$\left|\frac{dV_{GATE}}{dt}\right| = \frac{I_{DAC}}{C_{INT}} \tag{6}$$

in which $I_{DAC}$ is the DC output current of the DAC (set by the 8-bit rise time programming word), and $C_{INT}$ is the value of the integrating capacitor. When the pulse timing input is equal to logic "0", $I_C = I_{DAC}$ and $V_{GATE}$ ramps up from –2V to +2V with a slope of $+I_{DAC}/C_{INT}$. As $V_{GATE}$ passes through the linear range of the differential pair, the output current is switched. When the pulse timing input is equal to logic "1", $I_{DAC}$ is switched through the PNP transistor current mirror, $I_C = -I_{DAC}$ and $V_{GATE}$ ramps down from +2V to -2V with a slope of $-I_{DAC}/C_{INT}$. Assuming the current mirror to be ideal, the rise and fall times are equal and are given by

$$t_R = t_F = \frac{V_{LIN}}{I_{DAC}/C_{INT}} \tag{7}$$

in which $V_{LIN}$ is the linear range of the differential pair.

Note that the ±2V maximum and minimum levels of the $V_{GATE}$ waveform are set only approximately by the diode clamping network in the integrator feedback. This is not a problem, however; as indicated in section IV.A, only the slope of $V_{GATE}$ is important for determining the output rise time; all that is required of the maximum and minimum values of $V_{GATE}$ is that they be sufficient to fully switch the current steering differential pair. As a result, the approach shown in Figure 6a provides a gate drive waveform that implements programmable rise time with a simple, low cost circuit.

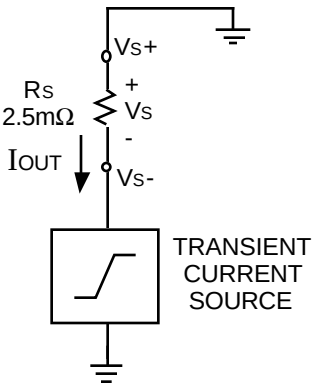


Fig. 7. Measurement configuration.

## V. Measured Results

Figure 7 shows the measurement configuration for the results that will be presented. For test purposes, the output current is determined from the voltage drop across a 2.5mΩ sense resistor $R_{SENSE}$ in series with the output current path. Figure 8 shows an oscilloscope display of the voltages $V_{S+}$ and $V_{S-}$ at each end of the sense resistor. Also shown is the difference $V_S = V_{S+} - V_{S-}$ which corresponds to $I_{OUT}$ at a scale of 20A/div. The transient current source is configured for maximum current at minimum rise time; the measured current is 52.4A with a rise time of 820ns.

Note the overshoot in the voltage waveforms of $V_{S+}$ and $V_{S-}$ due to the parasitic inductance in the $I_{OUT}$ current path. The additional voltage drop is less than 50mV, well within the 500mV budgeted for current source voltage compliance in section III.A. Note also the absence of overshoot in the current waveform, indicating well controlled switching of current by the differential pairs in the transient current stages.

Figure 9 shows a plot of measured rise times as a function of the rise time programming word. Rise times were measured for three different values of current being switched: 10A, 30A, and 50A. For shorter rise times, as the digital programming word increases, the incremental change in rise time decreases. This nonlinear characteristic is actually beneficial in the test environment, since it allows the user to vary the test rise time with finer resolution for high slew rates, where power supply problems are more likely to occur.

## VI. Conclusion

A prototype instrument has been developed which is capable of providing a transient current for testing of microprocessor power supplies. A system architecture incorporating a parallel stage, current steering approach with analog programming of rise time results in a simple, low cost system. Measurements show a maximum transient current of 50A with a rise time less than 1µs. The minimum current, maximum current, and rise time are digitally programmable.

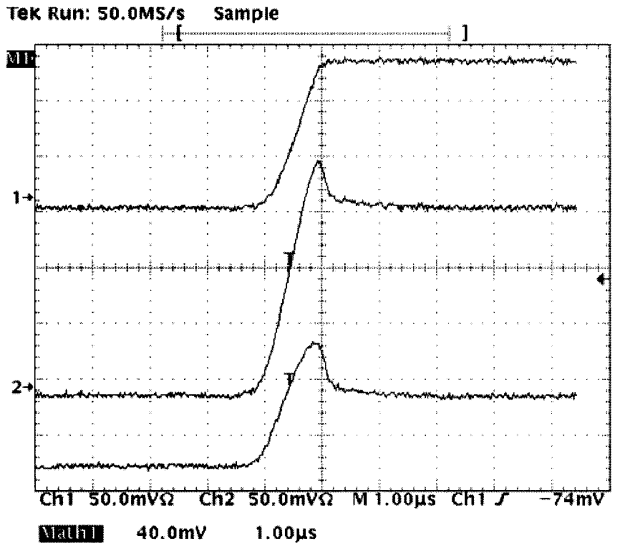


Fig. 8. Maximum current, minimum risetime transient

Top: $I_{OUT}$ at 20A/div Horizontal scale: 1µs/div
Middle: $V_{S-}$ at 50mV/div
Bottom: $V_{S+}$ at 50mV/div

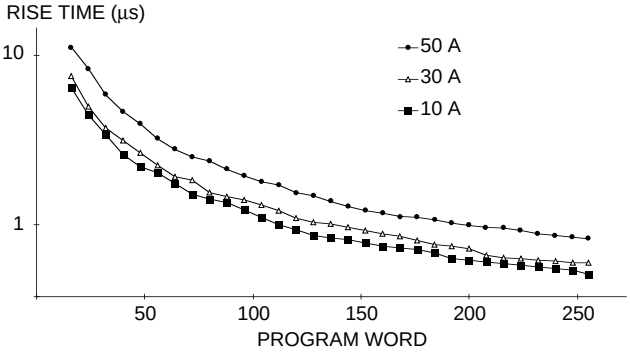


Fig. 9. Measured rise time as a function of program word.

## References

[1] "Fueling the Megaprocessor – DC-to-DC converter design," Texas Instruments (formerly Unitrode Corp. Application Note U-157).

[2] "HP60507B Electronic Load Specification," Agilent Technologies (formerly Hewlett-Packard Corp.)