is particularly suited to high precision filtering applications. The designed transconductor accomplishes 1.2GHz of cutoff frequency, almost 100dB of DC gain and a power consumption of 5mW.

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Interpolating ring VCO with *V*-to-*f* linearity compensation

J.A. McNeill

Indexing terms: Voltage controlled oscillators, Voltage-frequency convertors

The nonlinearity of interpolating ring voltage controlled oscillators is inherent because the interpolation is linear in delay. Linearity can be restored with a correction based on the predictable curvature of an unbalanced Gilbert translinear cell. Experimental results show *V*-to-*f* linearity better than 0.2% over a ±10% frequency range about 155MHz.

Introduction: Interpolating ring VCOs have been reported in high speed phase-locked loop (PLL) applications such as clock and data recovery [1–3] and frequency synthesis [4]. This type of VCO has the advantages of being fully integrable with high operating frequency and reasonable tuning range. One disadvantage that has been observed [3] is significant *V*-to-*f* nonlinearity. This can be detrimental in a PLL, because the slope of the *V*-to-*f* characteristic influences closed loop performance parameters such as loop bandwidth [5].

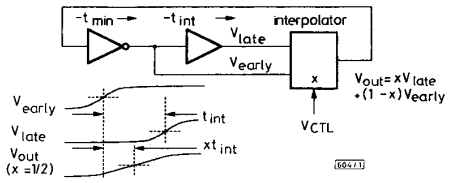

Fig. 1 *Interpolating ring VCO block diagram*

Fig. 1 shows a block diagram of an interpolating ring VCO with inverting delay t_{min}, noninverting delay t_{int}, and an interpolator whose output is the weighted sum of its inputs:

$$V_{out} = xV_{late} + (1-x)V_{early} \quad (1)$$

Fraction x ranges from 0 and 1 and is determined by the VCO control voltage V_{CTL}. Fig. 1 also shows an idealised timing diagram. If t_{int} is of the order of the signal rise time, the linear combination of amplitude is also a linear interpolation in delay [2]. The delay from V_{early} to V_{out} is $x \cdot t_{int}$, and the VCO frequency is

$$f = \frac{1}{T} = \frac{1}{2(t_{min} + xt_{int})} \quad (2)$$

In previous work x has been linearly related to V_{CTL}. For example, the interpolator in [2] is shown in Fig. 2. The contribution to V_{out} of V_{early} and V_{late} is determined by the tail currents I_{early} and I_{late} of Q_{1A}/Q_{1B} and Q_{2A}/Q_{2B}. Degenerated pair Q_{3A}/Q_{3B} apportions I_{EE} to I_{early} or I_{late}:

$$I_{late} = xI_{EE} \quad (3)$$

$$I_{early} = (1-x)I_{EE} \quad (4)$$

assuming transistor $\beta \to \infty$. Thus x is linear in V_{CTL}:

$$x = \frac{I_{late}}{I_{EE}} = \frac{V_{CTL}}{2 \cdot I_{EE} \cdot R_D} + \frac{1}{2} \quad (5)$$

The reason for the inherent *V*-to-*f* nonlinearity is now apparent from eqns. 2 and 5: V_{CTL} causes a linear change in x and a linear interpolation in delay time; but frequency is the inverse of time. The nonlinearity of eqn. 2 worsens rapidly as tuning range increases [1].

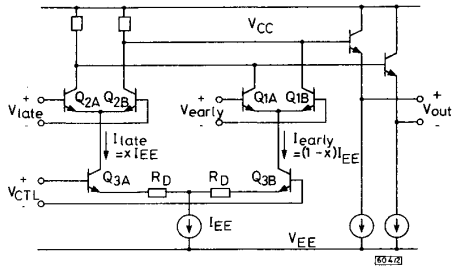

Fig. 2 *Interpolating circuit (after [2] Fig. 3)*

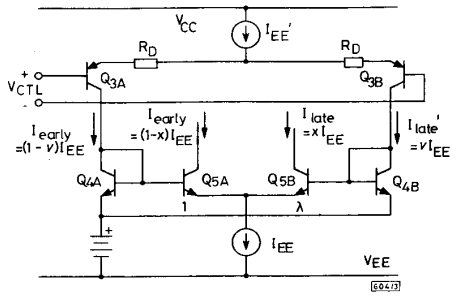

Fig. 3 *Translinear circuit for nonlinearity compensation*

Linearising V-to-f characteristic: The linearising technique is shown in Fig. 3. The circuit uses the Gilbert translinear principle [6] in the configuration of Q_{4A}/Q_{4B} and Q_{5A}/Q_{5B}, with Q_{5A}/Q_{5B} emitter areas unbalanced by a factor λ. The input to the cell is the current pair I_{late}' and I_{early}'. As in eqns. 3 and 4, Q_{3A}/Q_{3B} apportions I_{EE}' to I_{early}' or I_{late}':

$$I'_{late} = vI'_{EE} \quad (6)$$

$$I'_{early} = (1-v)I'_{EE} \quad (7)$$

As in eqn. 5, the apportioning fraction v is linear in V_{CTL}. This pair of currents flows through diode-connected transistors Q_{4A}/Q_{4B}. The resulting voltage is applied to Q_{5A}/Q_{5B}, which apportions I_{EE} to output currents I_{early} and I_{late}. These are used as the tail currents for Q_{1A}/Q_{1B} and Q_{2A}/Q_{2B} in the interpolator of Fig. 2. Frequency as a function of x is still governed by eqns. 2–4. Compensation for the nonlinearity of eqn. 2 is achieved with the unbalance λ in the emitter areas of Q_{5A} and Q_{5B}, which causes an opposite curvature in the v-to-x characteristic of the translinear cell. Gilbert shows that the output fraction x is determined by the input fraction v and the imbalance ratio λ:

$$x = \frac{\lambda v}{1 + (\lambda - 1)v} \quad (8)$$

Substituting eqn. 8 into eqn. 2 gives frequency f as a function of v:

$$f = \frac{1 + (\lambda - 1)v}{2(t_{min} + [(\lambda - 1)t_{min} + \lambda t_{int}]v)} \quad (9)$$

To make f linear in v, choose λ so that the bracketed coefficient of v in the denominator is zero:

$$[(\lambda - 1)t_{min} + \lambda t_{int}] = 0 \quad (10)$$

which is satisfied by

$$\lambda = \frac{t_{min}}{t_{min} + t_{int}} \quad (11)$$

Then substituting into eqn. 9 gives the V-to-f characteristic

$$f = \frac{1}{2t_{min}}\left[1 - \left(\frac{t_{int}}{t_{min} + t_{int}}\right)v\right] \quad (12)$$

which is linear in V_{CTL}, because v is linear in V_{CTL}.

Experimental results: The circuit of Fig. 3 was used in an interpolating ring VCO with a centre frequency of 155MHz. The circuit was designed for $t_{min} = 2t_{int}$, which gives a value of $\lambda = 0.67$ from eqn. 11. Simulation showed that an imbalance of $\lambda = 0.63$ gave slightly better linearity compensation. This is because of a small nonlinearity in the V_{CTL}-to-delay characteristic not accounted for in eqn. 2.

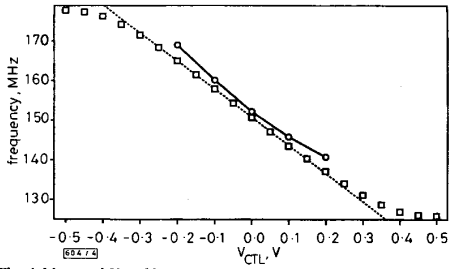

Fig. 4 *Measured V-to-f linearity*

□ measured frequency with linearity compensation
– – – – ideal linear V-to-f
—O— simulated frequency for uncompensated VCO

Fig. 4 shows the measured V-to-f characteristic of the with linearity compensation. Also shown is the simulated V-to-f of the uncompensated VCO; its nonlinearity is obvious by comparison. Fig. 5 shows the measured nonlinearity, which is less than 0.2% of the centre frequency over a ±10% tuning range. The compensation is stable over temperature, because t_{min} t_{int} tend to track, and the v-to-x characteristic of the translinear cell is temperature independent [6].

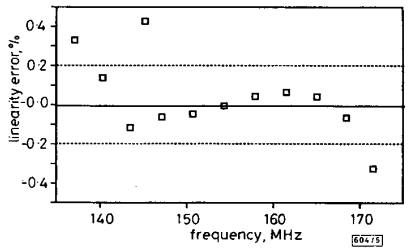

Fig. 5 *Linearity error against frequency*

Conclusion: The inherent nonlinearity of the interpolating ring oscillator can be compensated out in a stable, predictable manner. Experimental results show a control characteristic linear to within 0.2% over a ±10% frequency range.

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Resistance of an *n*-cube

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Indexing terms: Circuit theory, Graph theory

The resistance into any pair of vertices in an n-cube composed of 1Ω resistors is one of n distinct numbers between zero and unity. Exact explicit expressions are given for the extrernal vertex pair resistance values. As n becomes large all vertex pair resistances approach the same functional value.

The n-dimensional binary hypercube, or n-cube, occupies a prominent place in large scale computational applications both as a multiprocessor architecture and as a model structure in physical problems [1]. Multiprocessor systems are expected to appear containing over one million processors. If these were arranged in an n-cube positioned at the vertices in the cube, then this would indicate a dimension number $n = 20$ at least. Apart from computational hardware considerations, the n-cube appears with arbitrarily large dimension in topics in coding theory and in a variety of theoretical investigations. In particular, certain edge occurrence probabilities in random trees or paths may be expressed in terms of electrical resistances across single edges in a network of 1Ω resistors **N** having the same graph G as the system under consideration [2]. An application of this which is of considerable present concern is that of fault diagnosis in large systems [3]. The specific topic of interest here is the resistance between any pair of vertices in such a network **N** with graph G an n-cube.

The distance, or separation, between two vertices i, j in a graph G is the length in edges of a path of minimum length between the vertices i and j, and the diameter of a graph is the largest such distance over all the vertex pairs in G. Paths up to one diameter in length have application in minimum path length data routing in communication systems, including multiprocessor systems. The graph G used below will be that of an n-cube and use is made of an associated electrical network **N** having the same graph G and being constructed using a 1Ω resistor at the position of each edge in G.

P1: An n-cube has diameter n. For any vertex i being given, there is exactly one other vertex at a distance of one diameter from i. Between two vertices in G separated by one diameter, there are exactly $n!$ distinct paths each of length n edges. The maximum number of these paths which can be edge-disjoint is n and there is at least one subset containing exactly n paths which are edge-disjoint.

P2: Choose any minimum length path across one diameter in G which has one extremal vertex i and number the other n vertices in this path $i+1, i+2, \ldots, i+n$. If the resistance seen into the port in the network **N** formed by vertices i and j is written $R_{ij}(n)$ then the R_{ij} are such that $R_{ij} < R_{i,\,j+1}$ for $i+1 \le j \le i+n-1$. This sequence of n resistance values R_{ij} is numerically the same whichever minimum length path is chosen between any vertex pair separated by one diameter. For $n > 2$, all the R_{ij} are $R_{ij} < 1$.