EN390W
Practical Aspects of Grounding, Power, and EMI
Module 1: Grounding and Power

Lecture Notes

ANNOTATED PDFS WILL BE AVAILABLE

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Introduction: Noise and Interference

Noise is any electrical signal present in a circuit other than the desired signal.
Types of noise sources:
(1) intrinsic noise sources that arise from random fluctuations within physical systems, such as thermal and shot noise;
(2) man-made noise sources, such as motors, switches, computers, digital electronics, and radio transmitters; and
(3) noise caused by natural disturbances, such as lightning and sunspots.

Interference is the undesirable effect of noise.
If a noise voltage causes improper operation of a circuit, it is interference.
Noise cannot be eliminated, but can be reduced in magnitude, until it no longer causes interference.

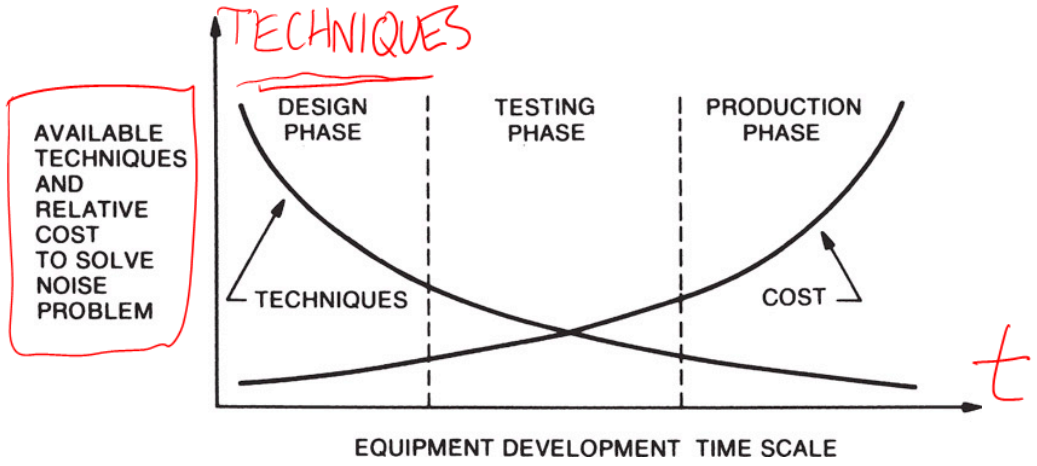


Figure 1-1: As equipment development proceeds, the number of available noise-reduction techniques goes down. At the same time, the cost of noise reduction goes up

Models for Noise Coupling

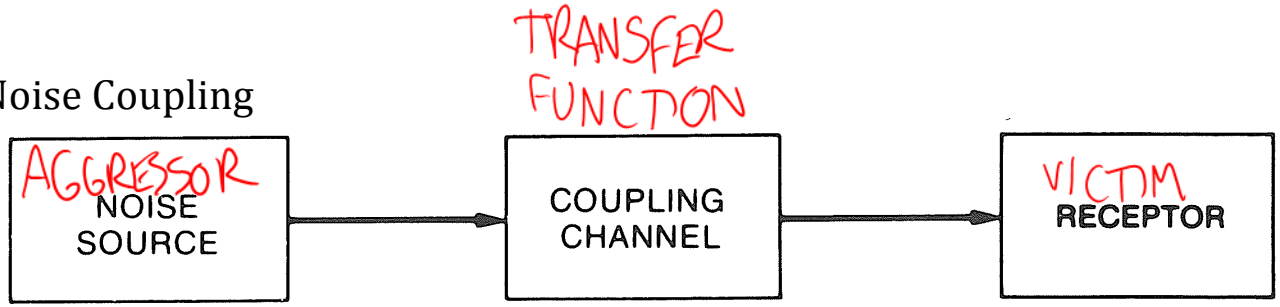


Figure 1-7: Before noise can be a problem, there must be a noise source, a receptor, and a coupling channel

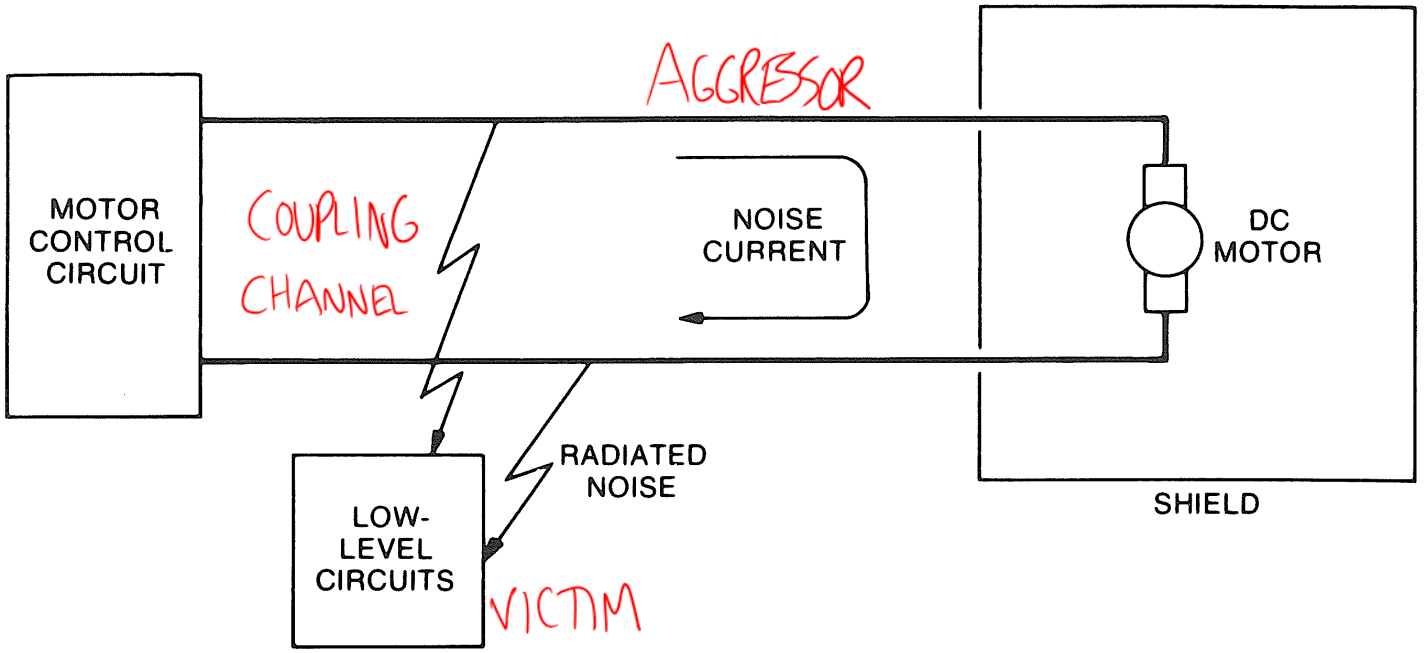


Figure 1-8: In this example, the noise source is the motor, and the receptor is the low-level circuit. The coupling channel consists of conduction on the motor leads and radiation from the leads

Coupling through EM fields

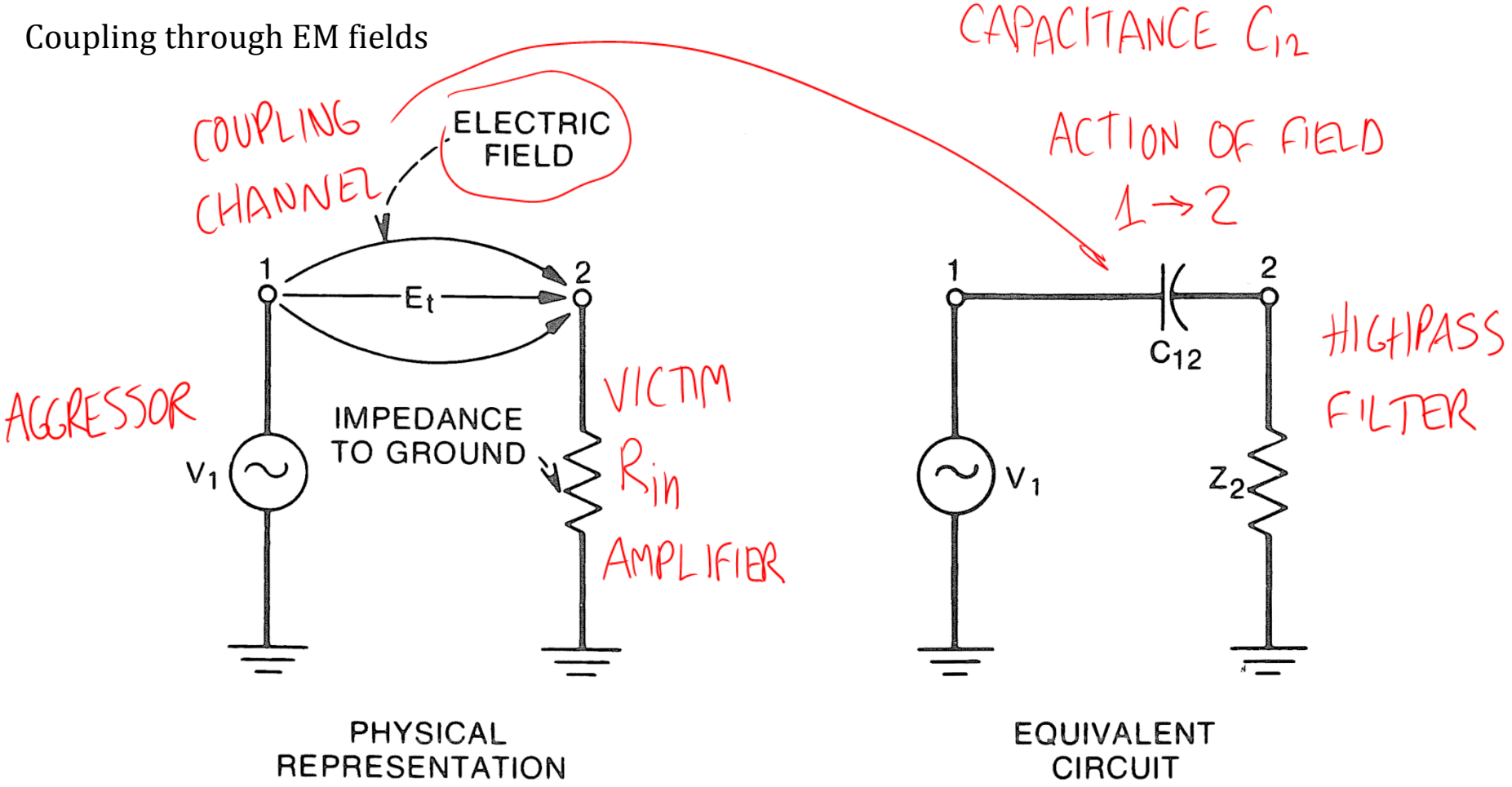
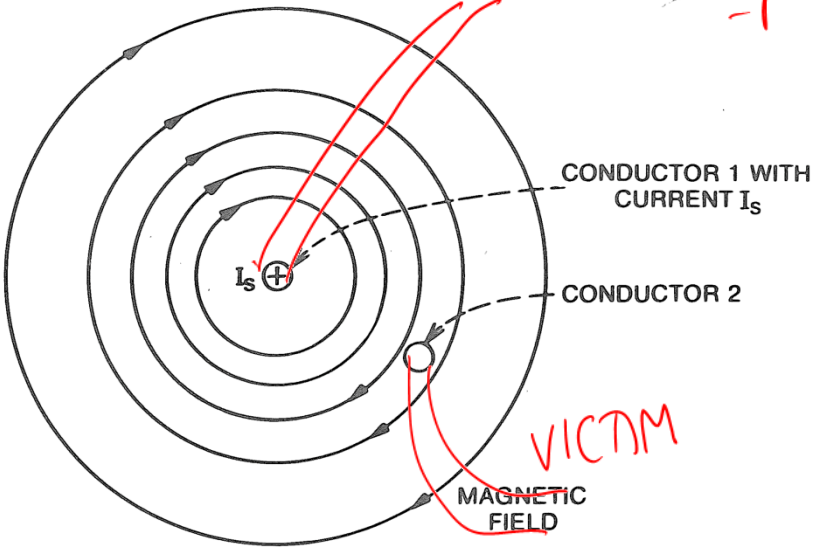
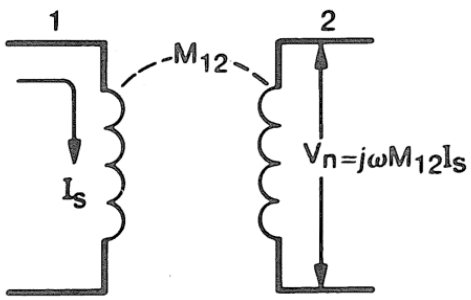


Figure 1-12: When two circuits are coupled by an electric field, the coupling can be represented by a capacitor



PHYSICAL REPRESENTATION



EQUIVALENT CIRCUIT

Figure 1-13: When two circuits are coupled by a magnetic field, the coupling can be represented as a mutual inductance

Coupling through common impedance

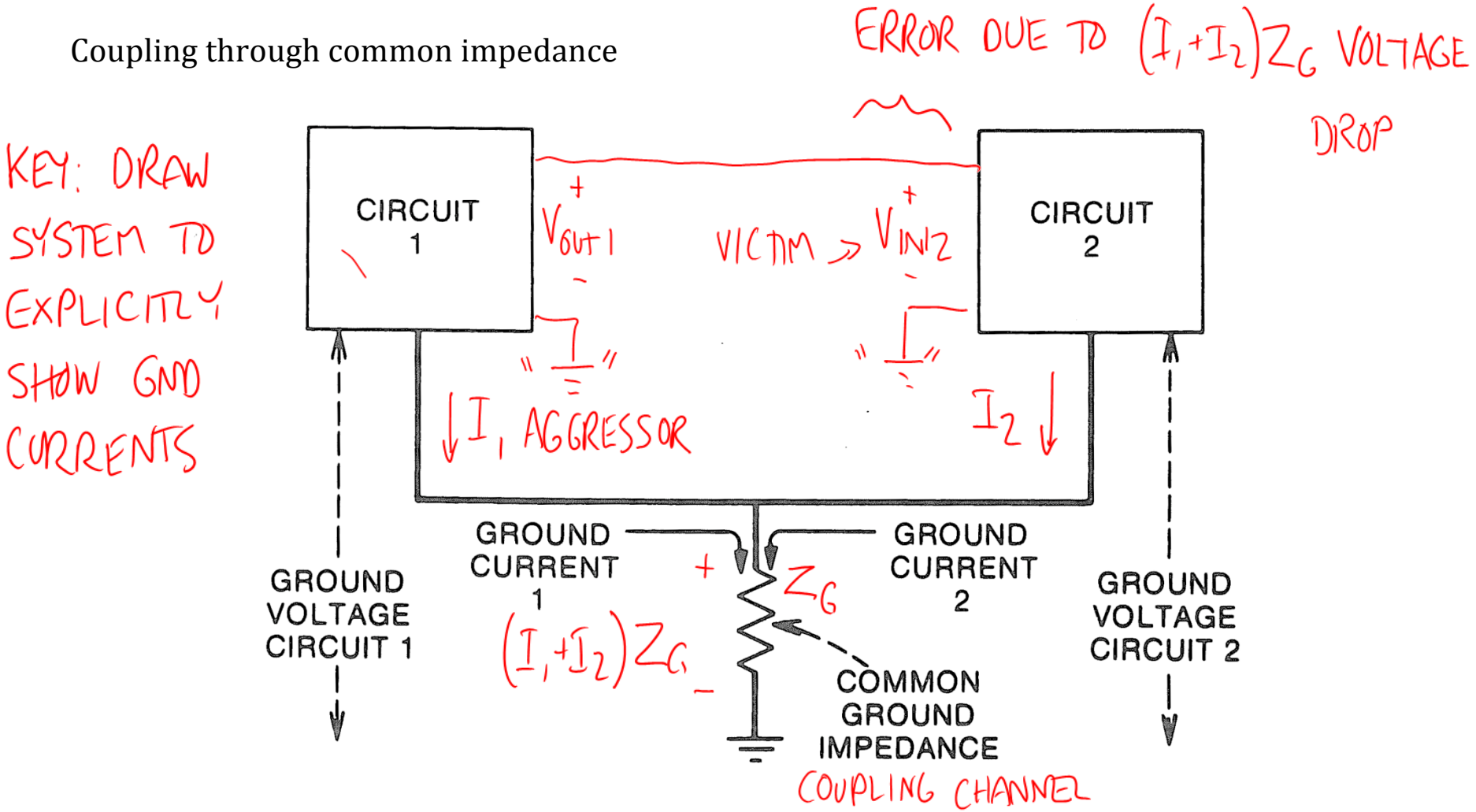


Figure 1-9: When two circuits share a common ground, the ground voltage of each one is affected by the ground current of the other circuit

2 FUNCTIONS OF "GROUND"
① VOLTAGE REFERENCE
② CURRENT RETURN PATH
$Z_G \neq 0$ CONFLICT!

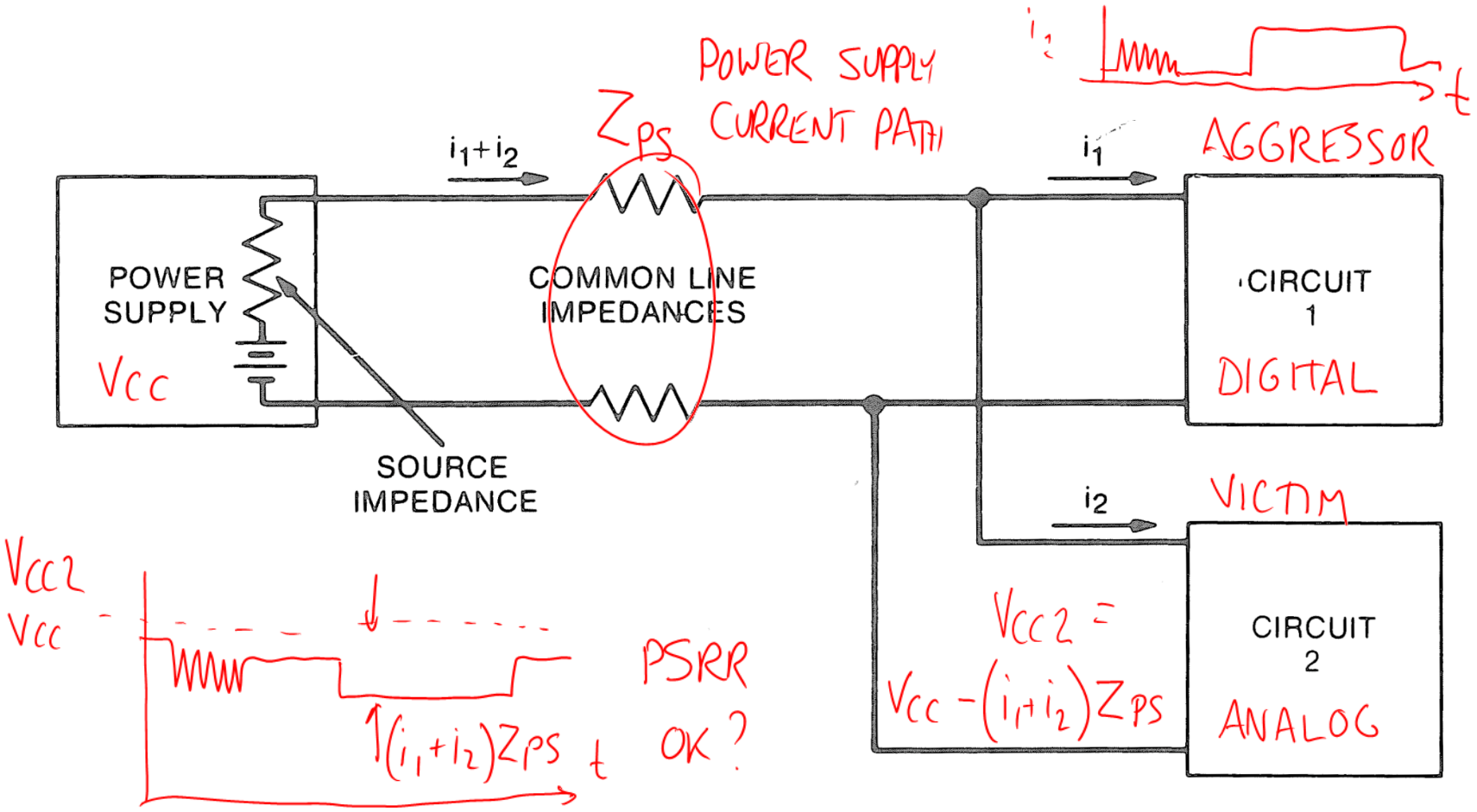


Figure 1-10: When two circuits share a common power supply, current drawn by one circuit affects the voltage at the other circuit

KEY: SHOW CURRENT PATHS!

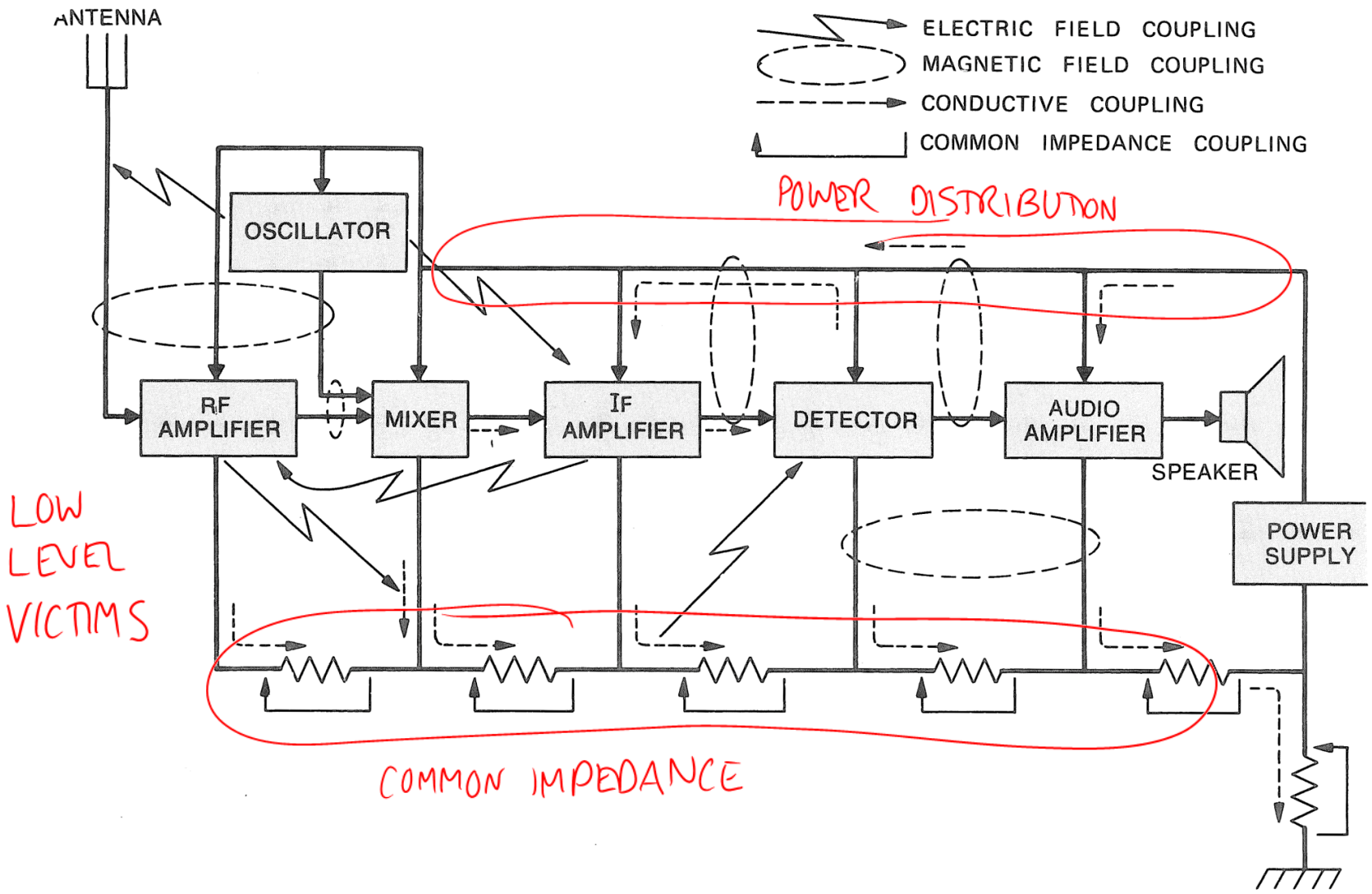


Figure 1-1. *Within equipment, such as this radio receiver, individual circuit elements can interfere with one another in several ways.*

Other Methods of noise coupling

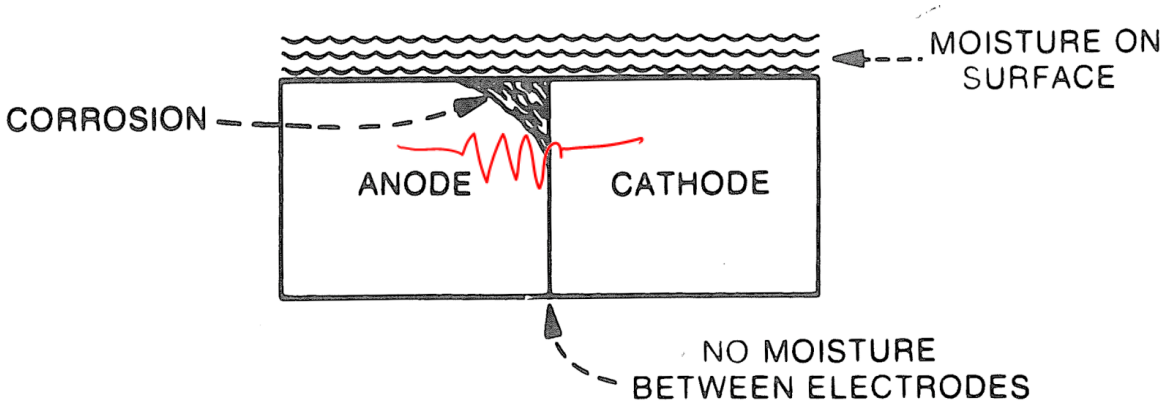


Figure 1-11: Galvanic action can occur if two dissimilar metals are joined and moisture is present on the surface

CONNECTORS

SMALL ΔV CONTACT POTENTIAL

INCREASES IMPEDANCE

One Minute Quiz:

Think of a noise / interference problem you have encountered in your engineering experience.

If possible, describe it in terms of the source – channel – receptor model.

METHODS OF ELIMINATING INTERFERENCE

The following chapters present techniques by which interference between electronic circuits can be eliminated, or at least reduced. The primary methods available for combatting interference are listed as follows:

1. Shielding BREAK FIELDS COUPLING: $M, C \rightarrow 0$
2. Grounding AVOID COMMON IMPEDANCE
3. Balancing VICTIM DIFFERENTIAL, GND NOT A REFERENCE
4. Filtering V A f SHAPE TRANSFER FUNCTION OF COUPLING CHANNEL
5. Isolation SEPARATE VICTIM, AGGRESSOR CURRENTS
6. Separation and orientation BREAKING (OR REDUCING) FIELDS COUPLING
7. Circuit impedance level control $Z_G \rightarrow 0$ $Z_{PS} \rightarrow 0$
8. Cable design SHIELDING, GROUNDING, TWISTED PAIR
9. Cancellation techniques (frequency or time domain).
   DIFFERENTIAL VS COMMON MODE
   INTERFERENCE $\leftrightarrow$ TIME SLOTTING

*

Summary: Introduction

- Designing equipment that does not generate noise is as important as designing equipment that is not susceptible to noise.
- Noise sources can be grouped into the following three categories: (1) intrinsic noise sources, (2) man-made noise sources, and (3) noise caused by natural disturbances.
- To be cost effective, noise suppression must be considered early in the design.
- Electromagnetic compatibility is the ability of an electronic system to function properly in its intended electromagnetic environment.
- Electromagnetic compatibility should be a major design objective: designed into a product not added on at the end of the design.
- The following three items are necessary to produce an interference problem:
  - A noise source
  - A coupling channel
  - A susceptible receptor
- Three important aspects of noise / interference problems:
  - Frequency
  - Amplitude
  - Time (when does it occur)
- Metals in contact with each other must be galvanically compatible.
- Noise can be reduced in an electronic system using many techniques; a single unique solution to most noise reduction problems does not exist.

Grounding

Safety:

ISSUE: FAULT CAUSES UNSAFE VOLTAGE ON CHASSIS

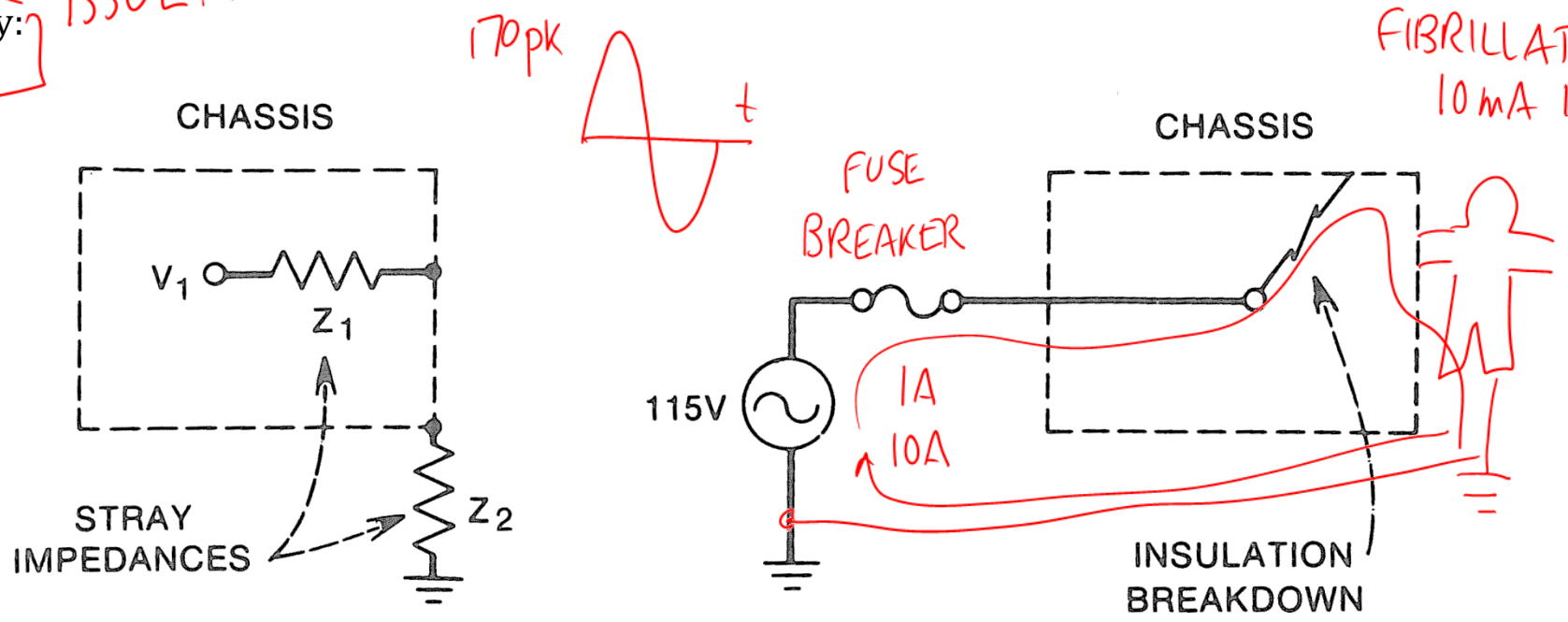


Figure 3-1. *Chassis should be grounded for safety. Otherwise, it may reach a dangerous voltage level through stray impedances (left) or insulation breakdown (right).*

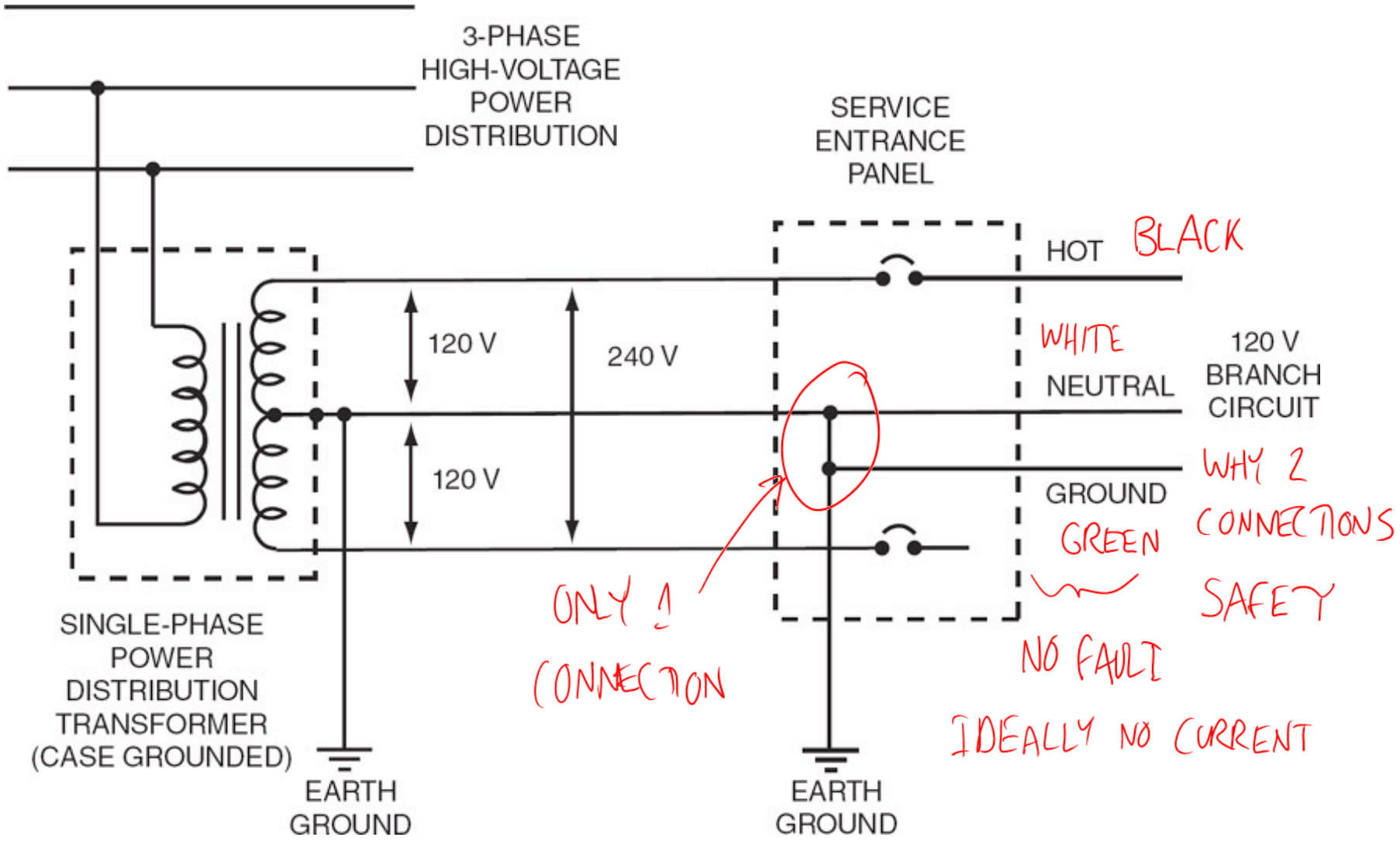


Figure 3-1: A single-phase residential service providing 120/240 V single-phase power

Safety: NEC specifies that the neutral and ground wires shall be connected together at *one and only one point*

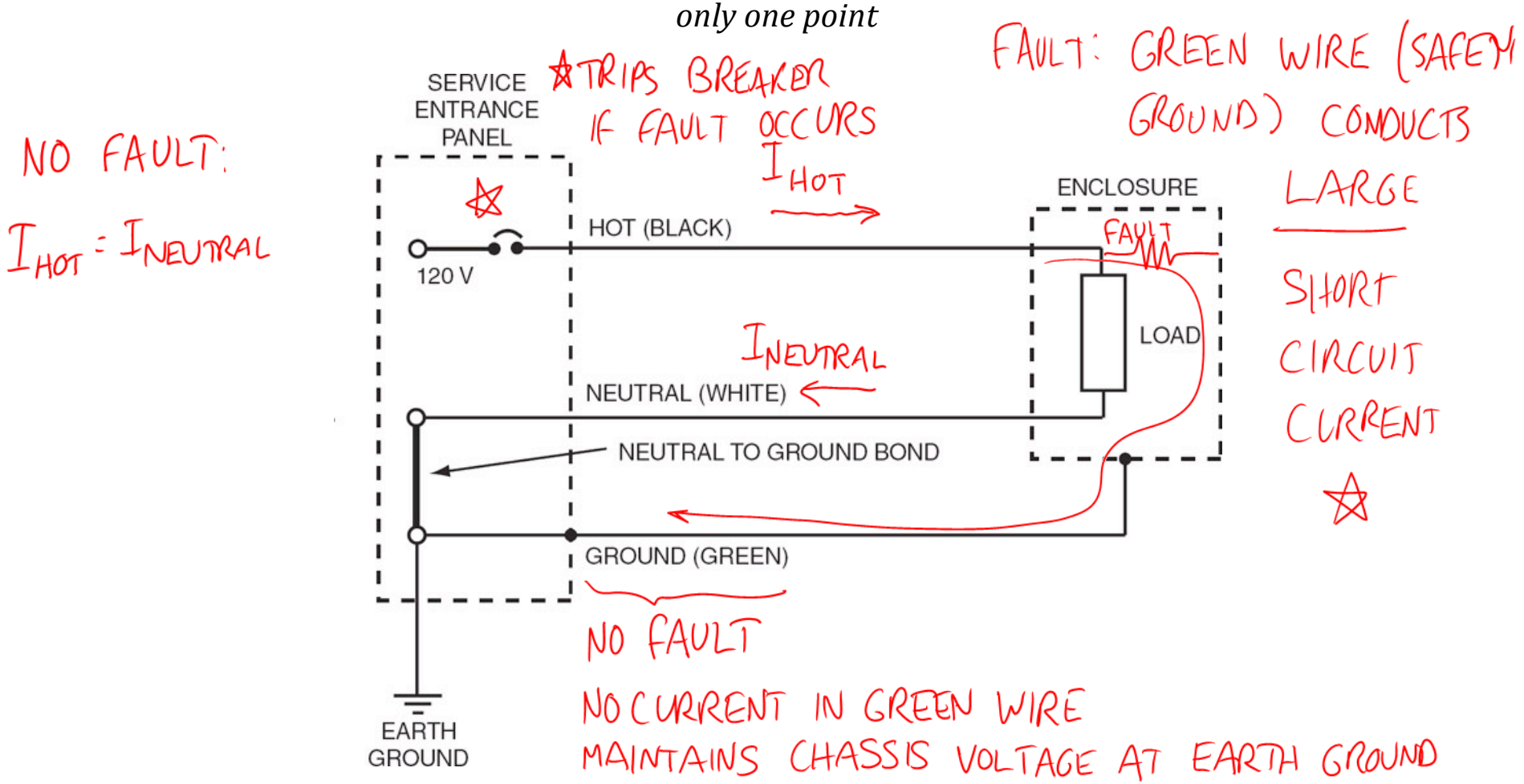


Figure 3-2: Standard 120-V ac power distribution branch circuit has three conductors

Note: GFCI looks for $I_{HOT} \neq I_{NEUTRAL}$

PARTIAL FAULT: Z_{FAULT} NOT ENOUGH TO TRIP

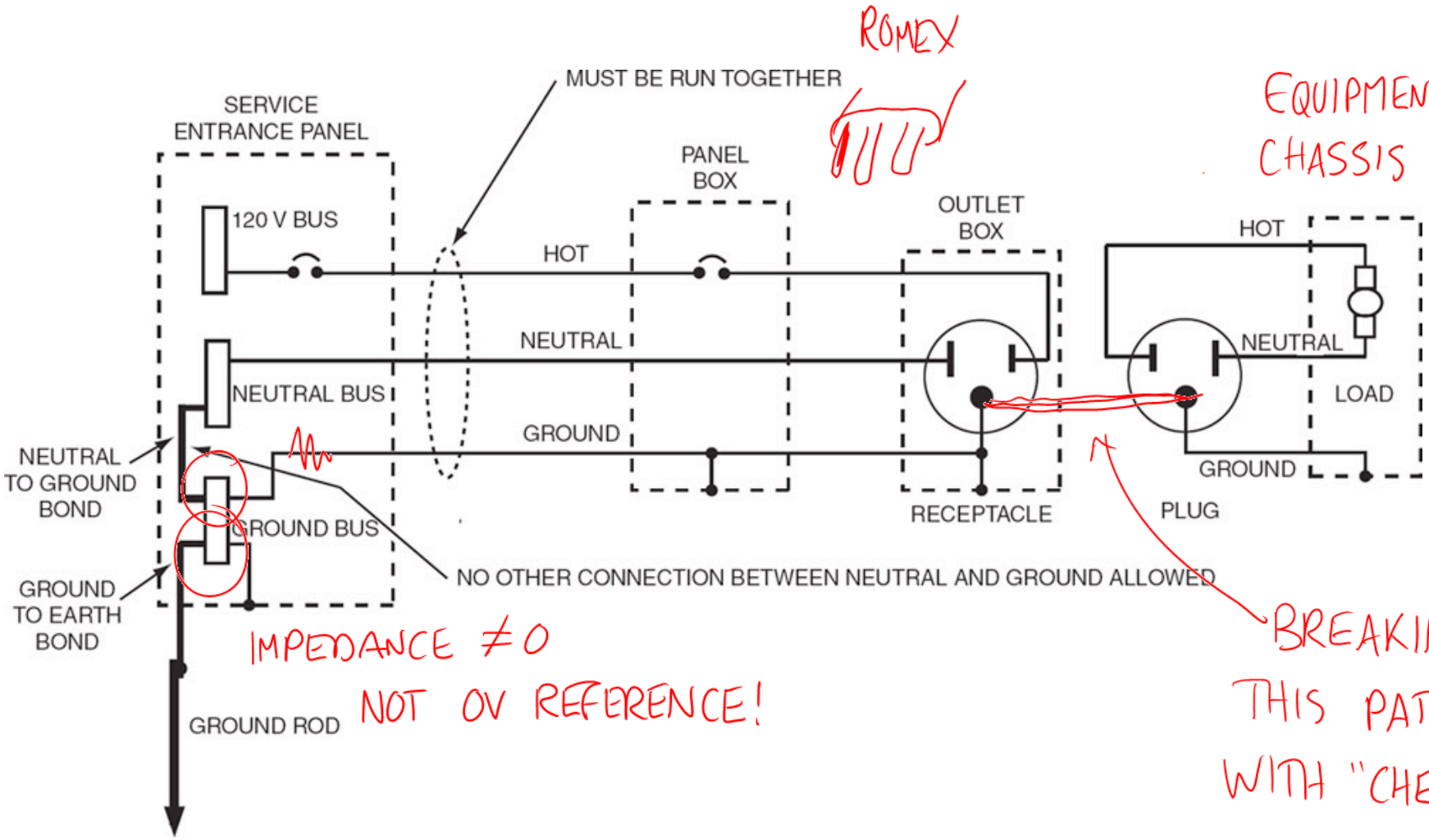


Figure 3-3: A properly wired and grounded ac branch circuit

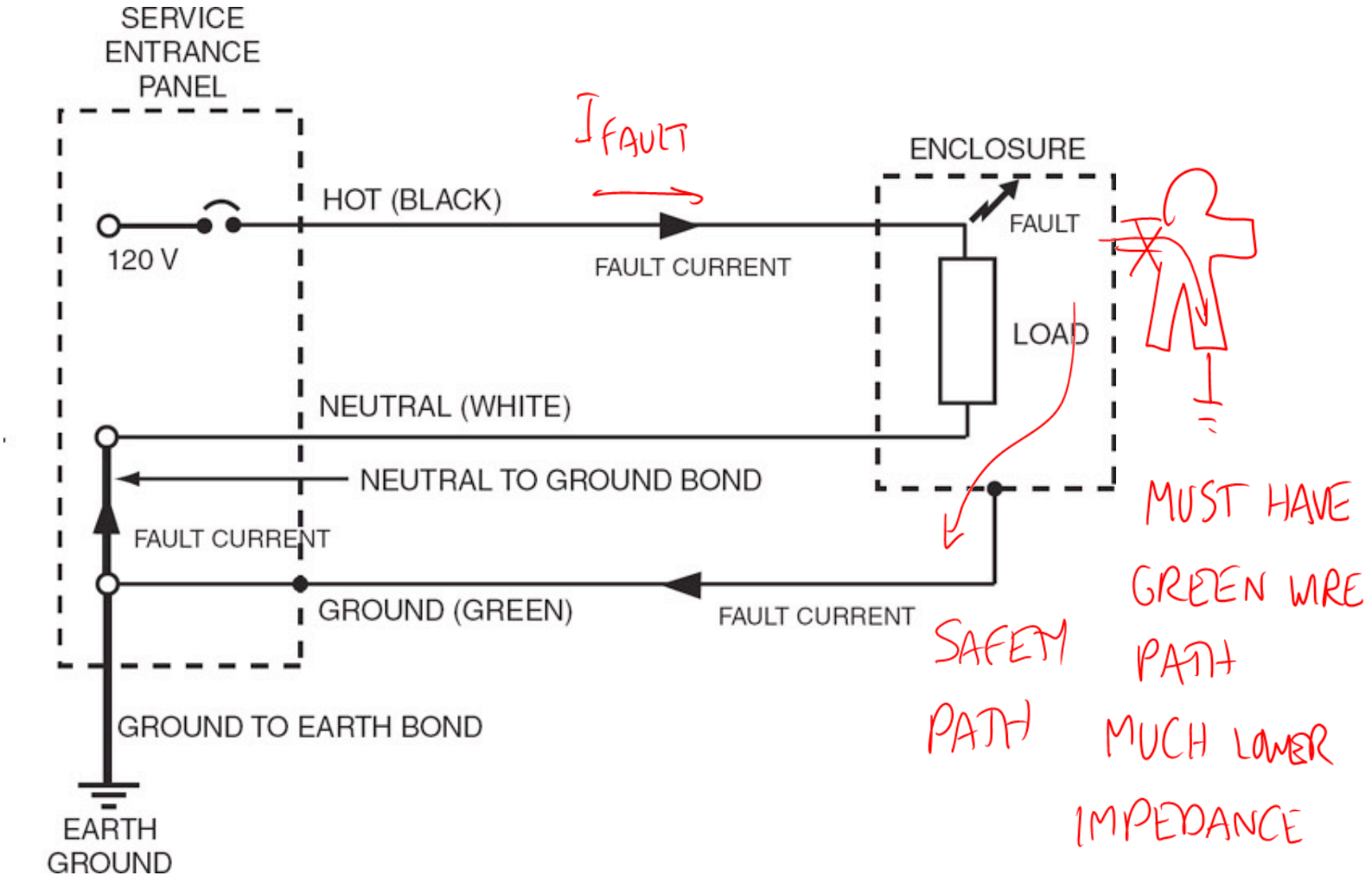


Figure 3-5: Fault current path in a standard 120-V ac power distribution branch circuit

NEC says very little about the issue of noise and interference control
Mostly concerned with electrical safety and fire protection.
System designer must find a way to satisfy the code and still produce a low-noise system.
NEC is only concerned with a frequency of 50/60 Hz and its harmonics.
An acceptable 60-Hz ground will not be an acceptable 1-MHz ground.
IEEE Std. 1100-2005, *IEEE Recommended Practice for Powering and Grounding Electronic Equipment*
Noise can be differential mode (hot to neutral) or common mode (neutral to ground)
Grounding, however, will only have an effect on the common-mode noise.

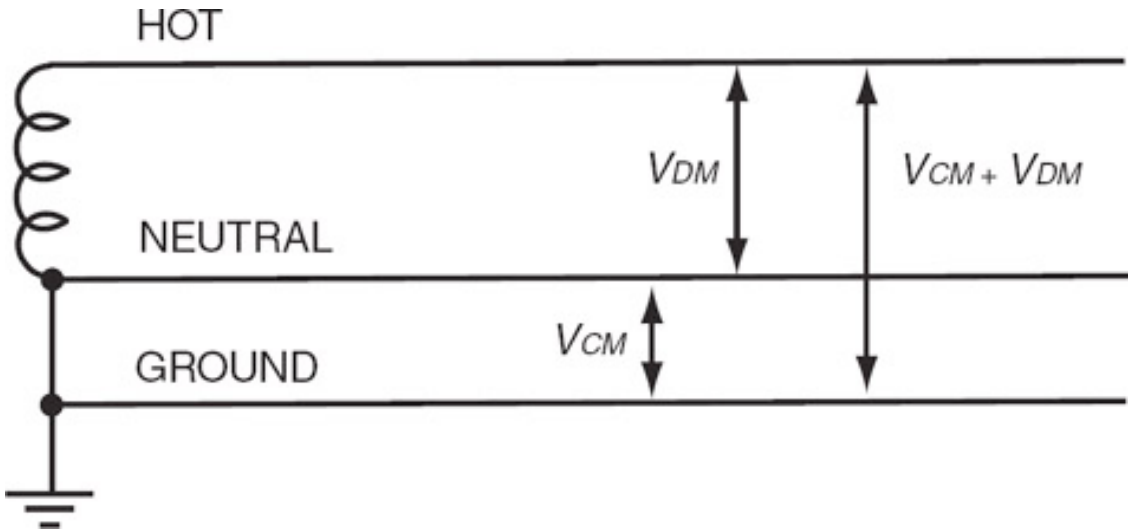


Figure 3-6: Differential-mode and common-mode noise

To control noise and interference, must create a low-impedance ground system that is effective not only at 50/60 Hz but also at much higher frequencies (10s – 100s MHz).
Supplemental ground conductors such as ground straps, ground planes, ground grids, and so on may be required.
NEC allows such supplemental ground conductors provided they meet the following two conditions:

1. They must be in addition to the ground conductors required by NEC, not in place of them.
2. They must be bonded to the NEC required ground conductors.

FREQUENCY RANGE

SIGNAL f RANGE

INTERFERING SIGNAL f

CAUTION: “Earth” ground INEFFECTIVE

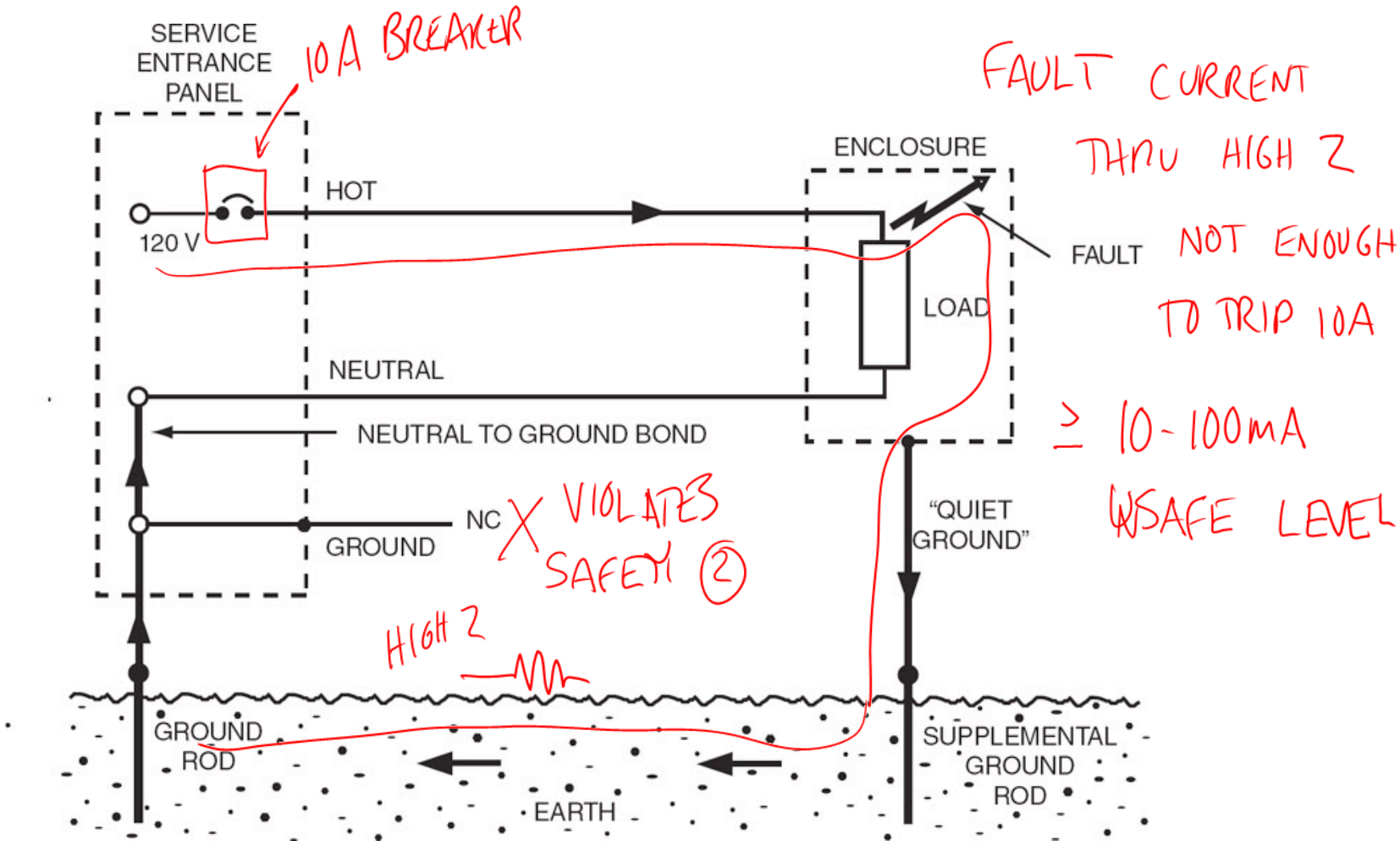


Figure 3-7: Fault current path when the load is connected to an isolated or separate "quiet" ground. This configuration is dangerous and violates the NEC

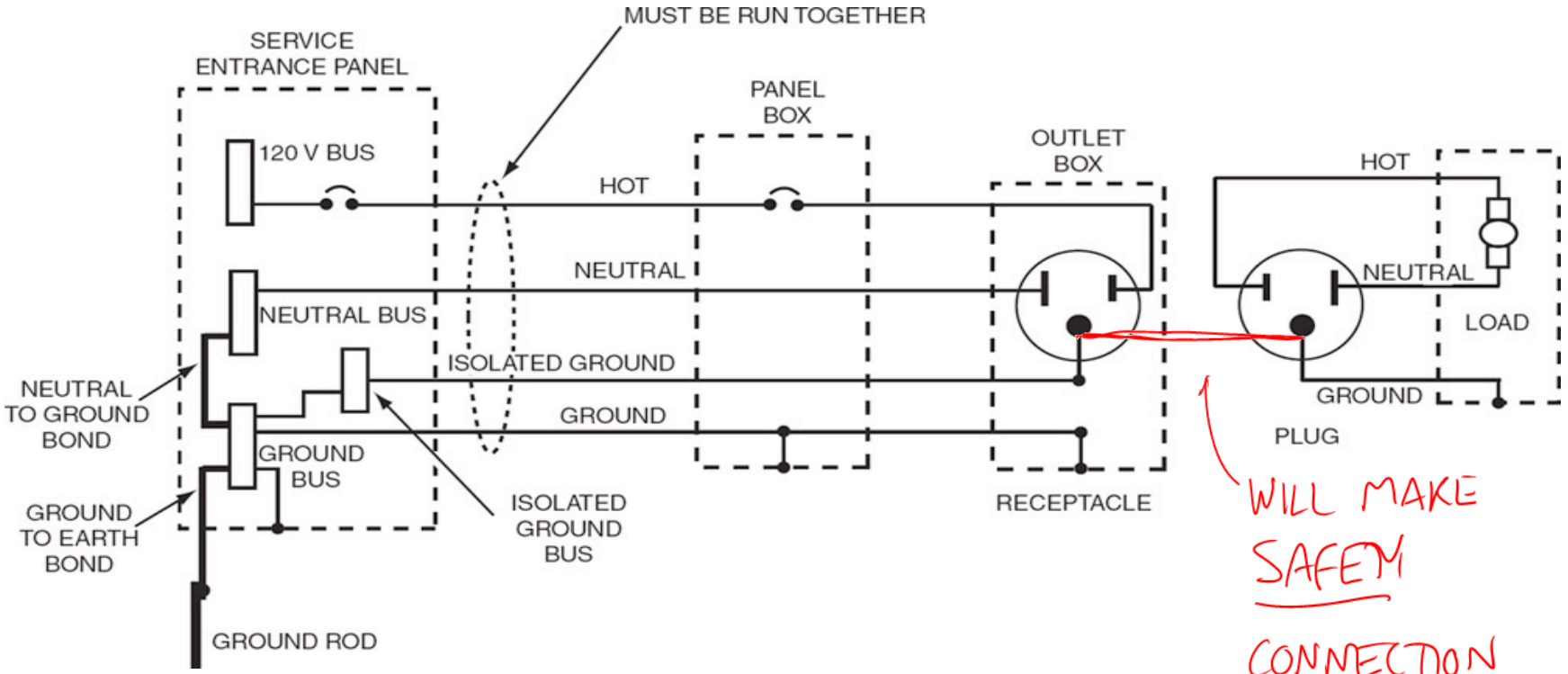


Figure 3-8: A properly wired IG receptacle

In practice, there will be small (safe) voltage difference between the grounds of outlets.
Leakage currents, magnetic field induction, and currents that flow through EMI filter capacitors connected to the equipment ground cause these voltages.
Typically less than 100 mV, but in some cases, it is as high as a few volts.
These noise voltages, although safe, are excessive if coupled into most low-level signal circuits.
Therefore, *the ac power ground is of little practical value as a signal reference.*
Connection should be made to the ac power, or earth, ground only when required for safety.

Isolated Grounds

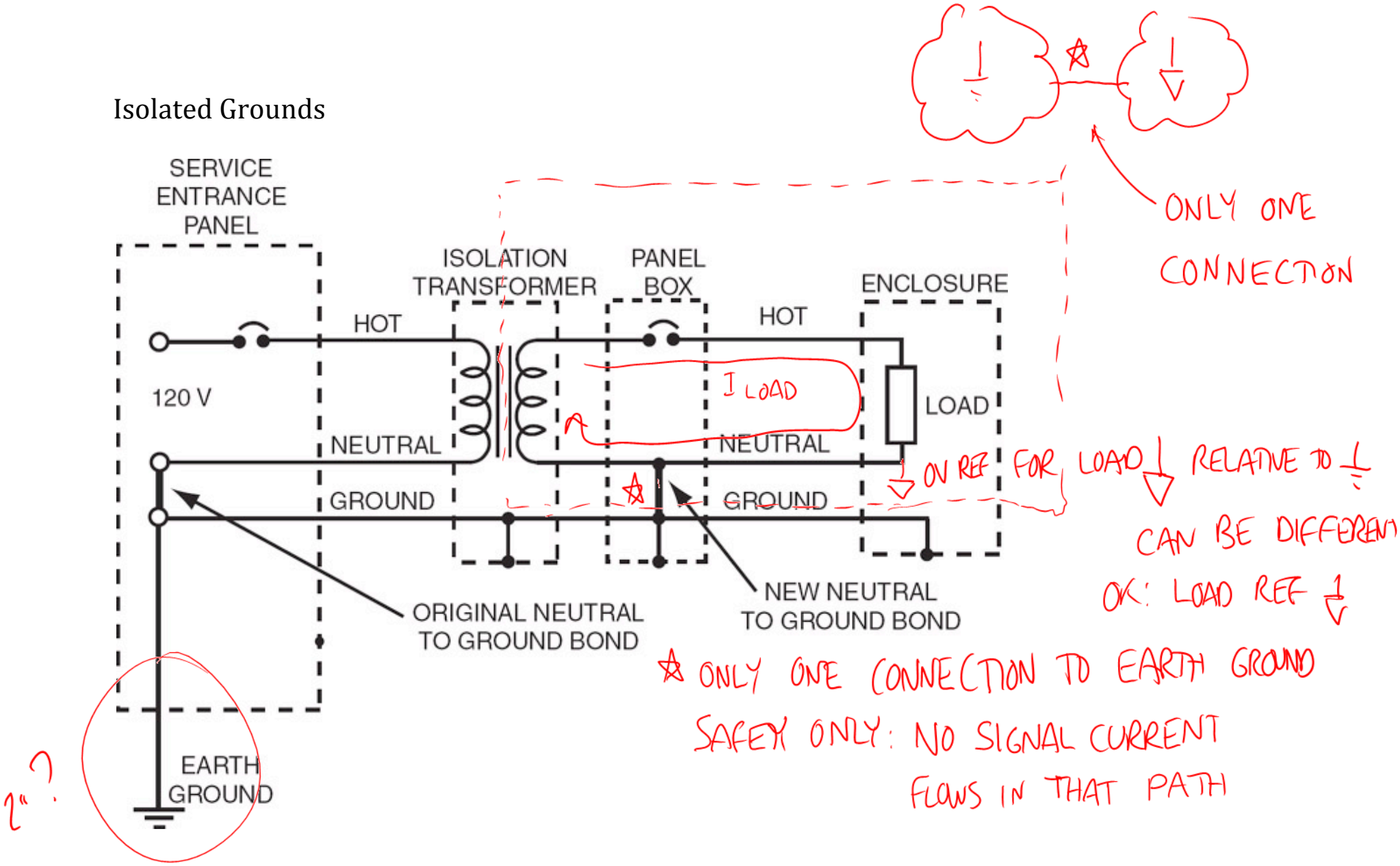


Figure 3-9: An isolation transformer used to create a separately derived system. A new neutral-to-ground bond point is established at the transformer or first panel box after the transformer

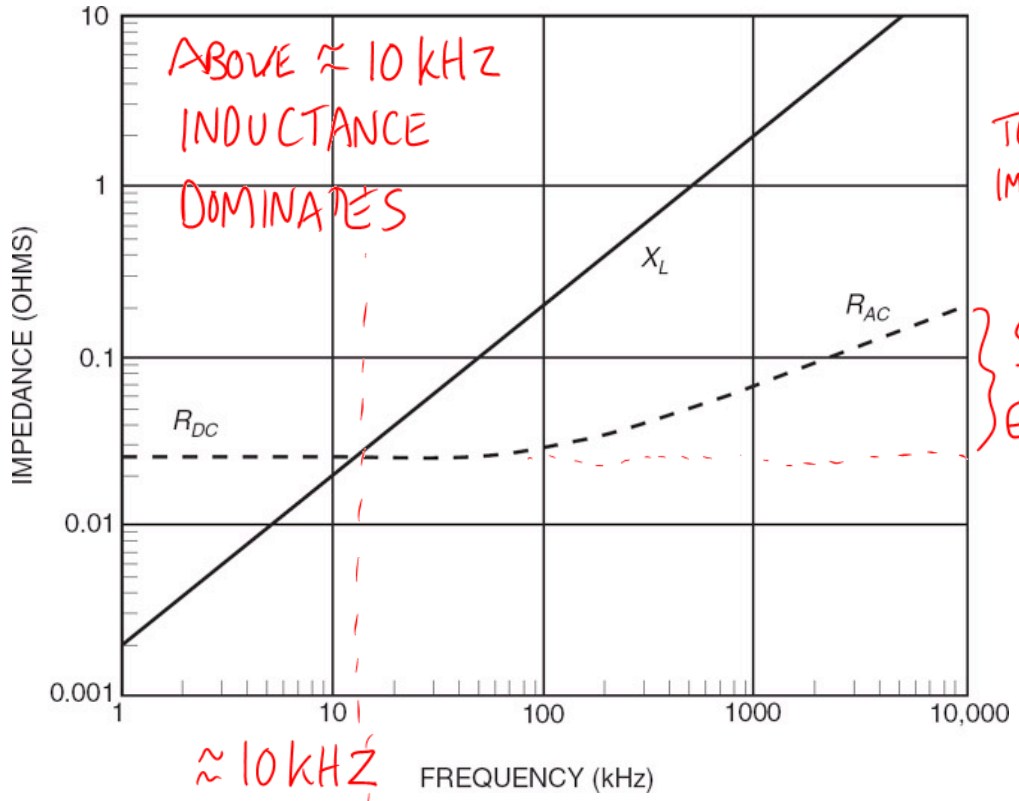
Grounding Myths

1. The earth is a low-impedance path for ground current. False, the impedance of the earth is orders of magnitude greater than the impedance of a copper conductor.
2. The earth is an equipotential. False, this is clearly not true as a result of (1).
3. The impedance of a conductor is determined by its resistance. False, what happened to the concept of inductive reactance?
4. To operate with low noise, a circuit or system must be connected to an earth ground. False, because airplanes, satellites, cars, and battery-powered laptop computers all operate fine without a ground connection. As a matter of fact, an earth ground is more likely to be the cause of a noise problem. More electronic system noise problems are resolved by removing (or isolating) a circuit from earth ground than by connecting it to earth ground.
5. To reduce noise, an electronic system should be connected to a separate "quiet ground" by use of a separate, isolated ground rod. False, in addition to being untrue, this approach is dangerous and violates the requirements of the NEC.
6. An earth ground is unidirectional, with current only flowing into the ground. False, because current must flow in loops, any current that flows into the ground must also flow out of the ground somewhere else.
7. An isolated receptacle is not grounded. False, the term "isolated" refers only to the method by which a receptacle is grounded, not if it is grounded.
8. A system designer can name ground conductors by the type of the current that they should carry (i.e., signal, power, lightning, digital, analog, quiet, noisy, etc.), and the electrons will comply and only flow in the appropriately designated conductors. Obviously false.

CURRENT HAS TO FLOW IN A LOOP: FOLLOW COMPLETE PATH

Signal Grounds: Three basic objectives of signal grounding are as follows:

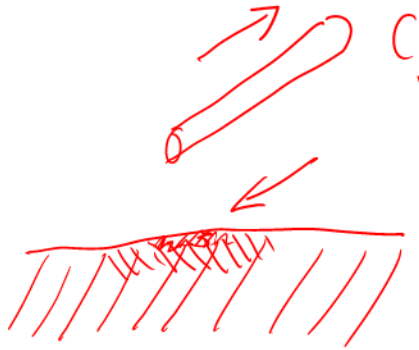
1. Not to interrupt the ground return path $Z_G \to 0$
2. Return the current through the smallest loop possible AVOIDS RADIATION, LOWER IMPEDANCE
3. Be aware of possible common impedance coupling in the ground UNWANTED SHARED CURRENT PATHS



TOTAL IMPEDANCE RES INDUCTIVE

$$Z_g = R_g + j\omega L_g \quad (3\text{-}1)$$

SKIN EFFECT



CURRENT "WANTS" TO FLOW IN SMALLEST POSSIBLE LOOP AT HIGH FREQUENCIES

RETURN CURRENT "PULLED" CLOSE TO SURFACE

RESISTANCE INCREASES

Figure 3-10: Resistance and inductive reactance versus frequency for a straight, 1-ft length of 24-gauge wire, located 1-in. above a ground plane

"HIGH FREQUENCIES"
$|Z_L| > |Z_R|$

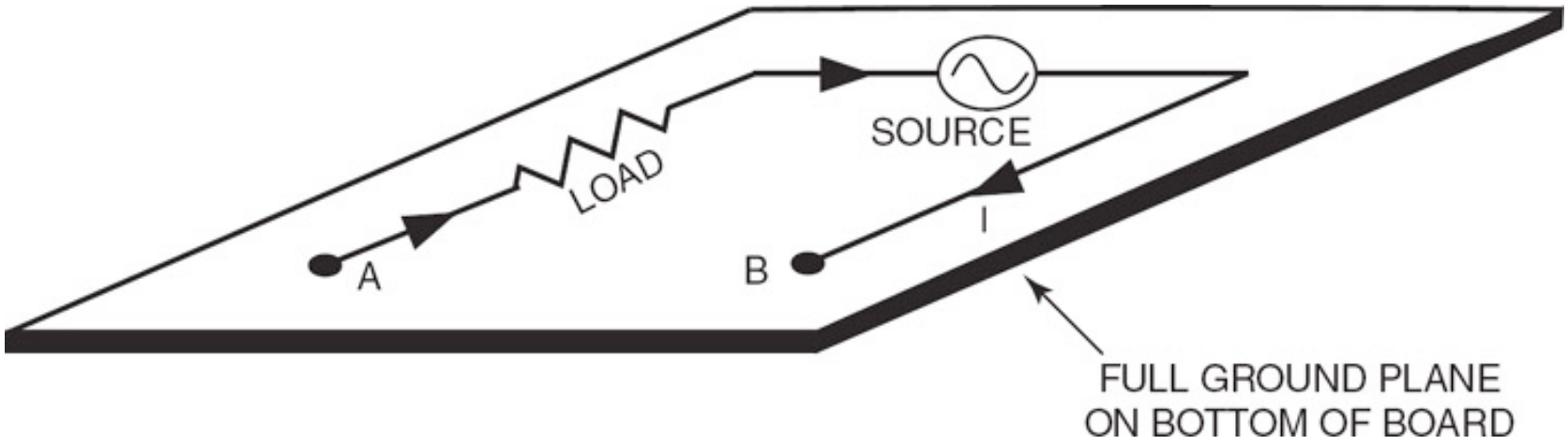


Figure 3-11: A double-sided PCB with a single trace on the topside and a full ground plane on the bottom side. How does the ground plane current flow between points A and B?

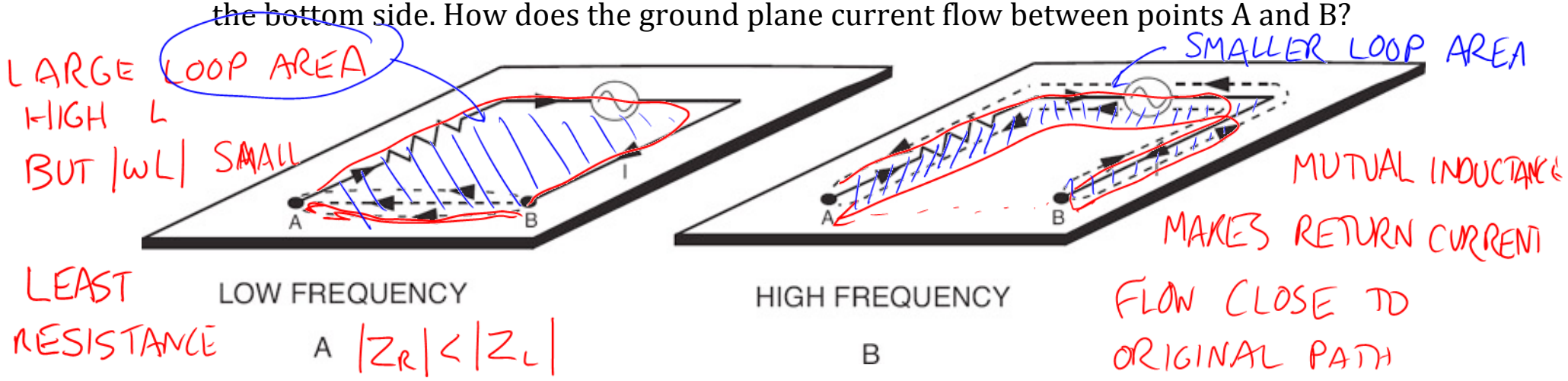


Figure 3-12: Ground plane current path, (A) at low frequency the return current takes the path of least resistance and (B), at high frequency the return current takes the path of least inductance

ALWAYS WANT TO MINIMIZE LOOP AREA LOWER L, LOWER Z_L LOWER EMISSION
LOWER SUSCEPTIBILITY

VISUALIZE WHERE CURRENT "WANTS" TO FLOW: CONTINUOUS PATH

Signal grounds can be divided into the following three categories:

1. Single-point grounds
2. Multipoint grounds
3. Hybrid grounds

In general, it is desirable that the topology of the power distribution system follows that of the ground.

Usually, the ground structure is designed first, and then the power is distributed in a similar manner.

Voltage drop along current path in "ground"

$$V_g = I_g Z_g \qquad (3\text{-}2)$$

"GROUND" IMPLIES $V_g = 0$

MINIMIZE IMPEDANCE

MINIMIZE SHARED COMMON IMPEDANCE

(IF POSSIBLE, DON'T SHARE CURRENT PATHS)

Single Point Grounds

Single-point grounds are most effectively used at low frequency, from dc up to about 20 kHz. They should usually not be used above 100 kHz, although sometimes this limit can be pushed as high as 1 MHz. With single-point grounding, we control the ground topology to direct the ground current to flow where we want it to flow, which decreases I_g in the sensitive portions of the ground.

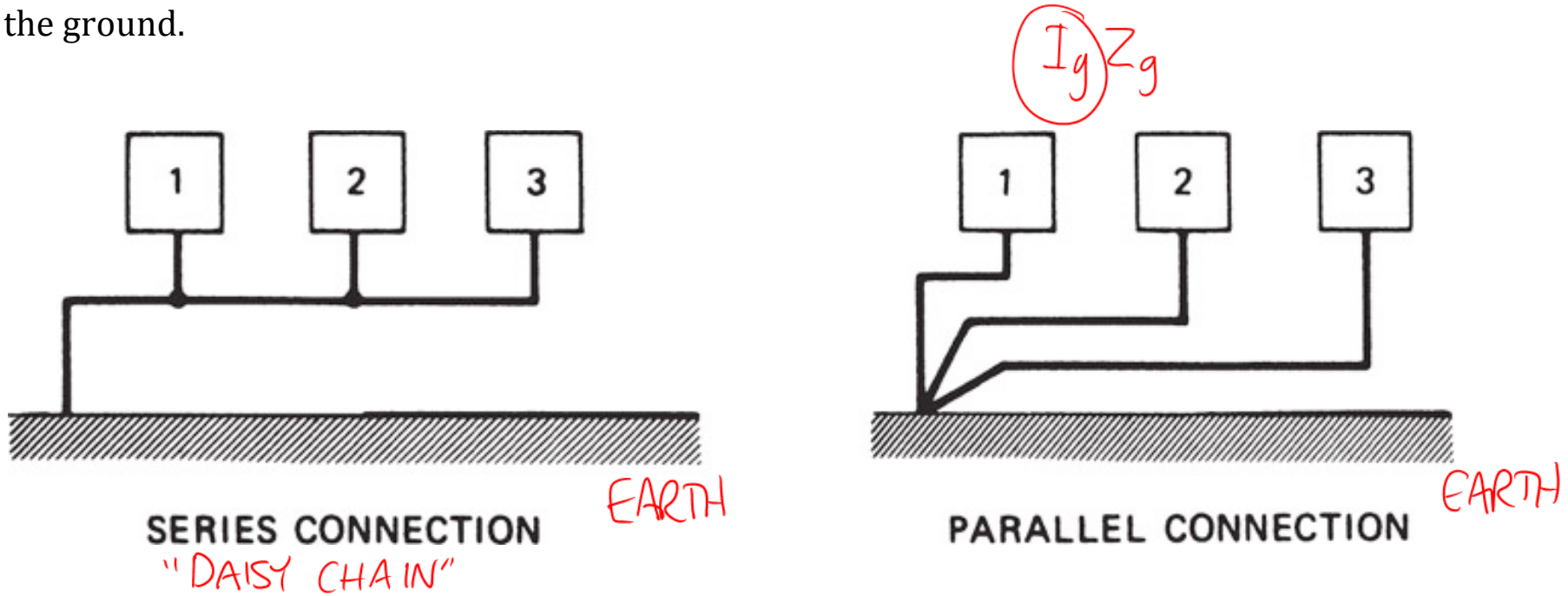


Figure 3-13: Two types of single-point grounding connections

"Daisy Chain" ground

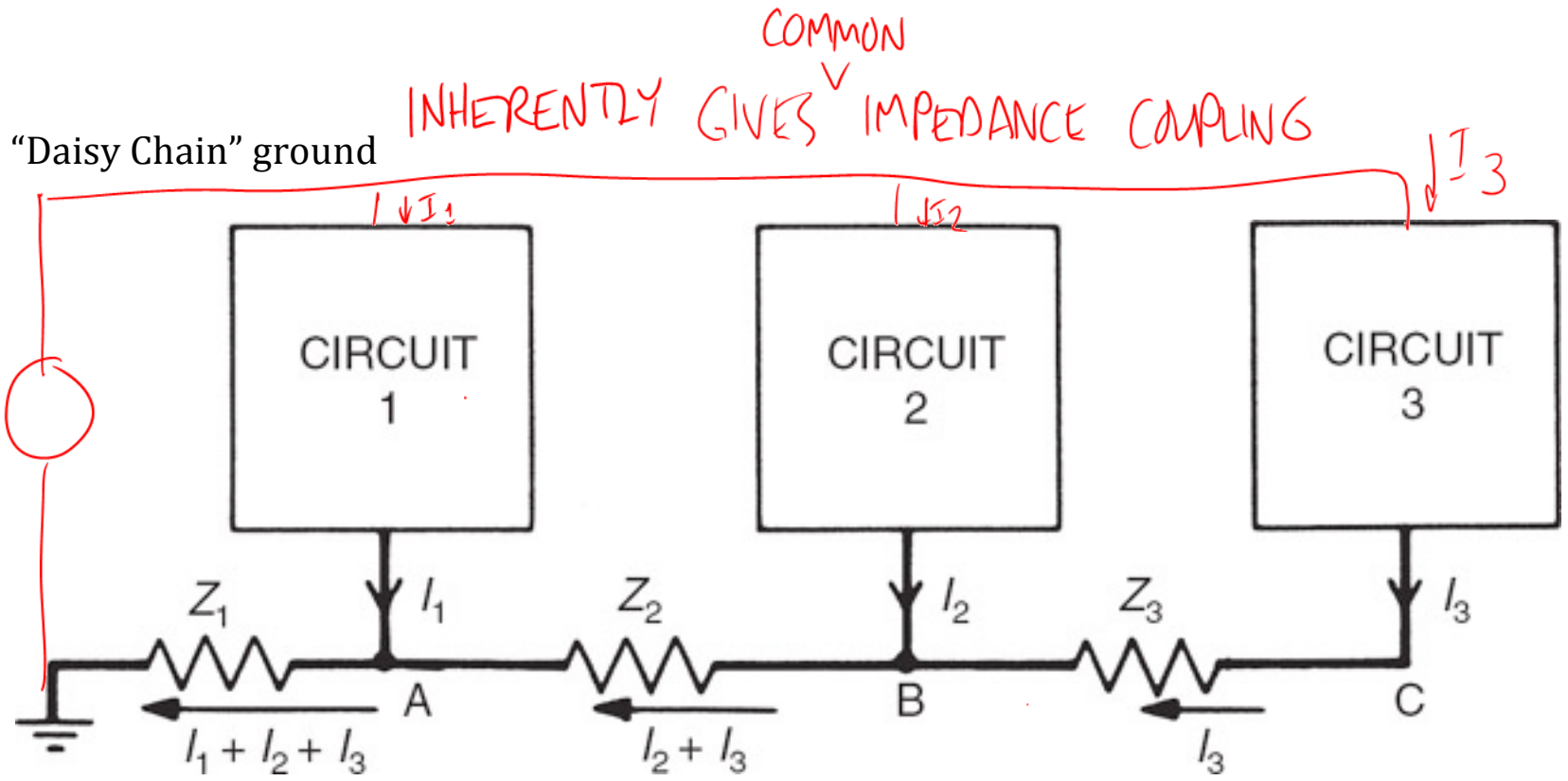


Figure 3-15: Common, or daisy chain, single-point ground system is a series ground connection and is undesirable from a noise standpoint, but it has the advantage of simple wiring

MAY BE OK IF I_1, I_2, I_3 SMALL } $I_g Z_g$ SMALL
Z_1, Z_2, Z_3 REL TO SIGNAL

BLOCK TO BLOCK COMMUNICATION?

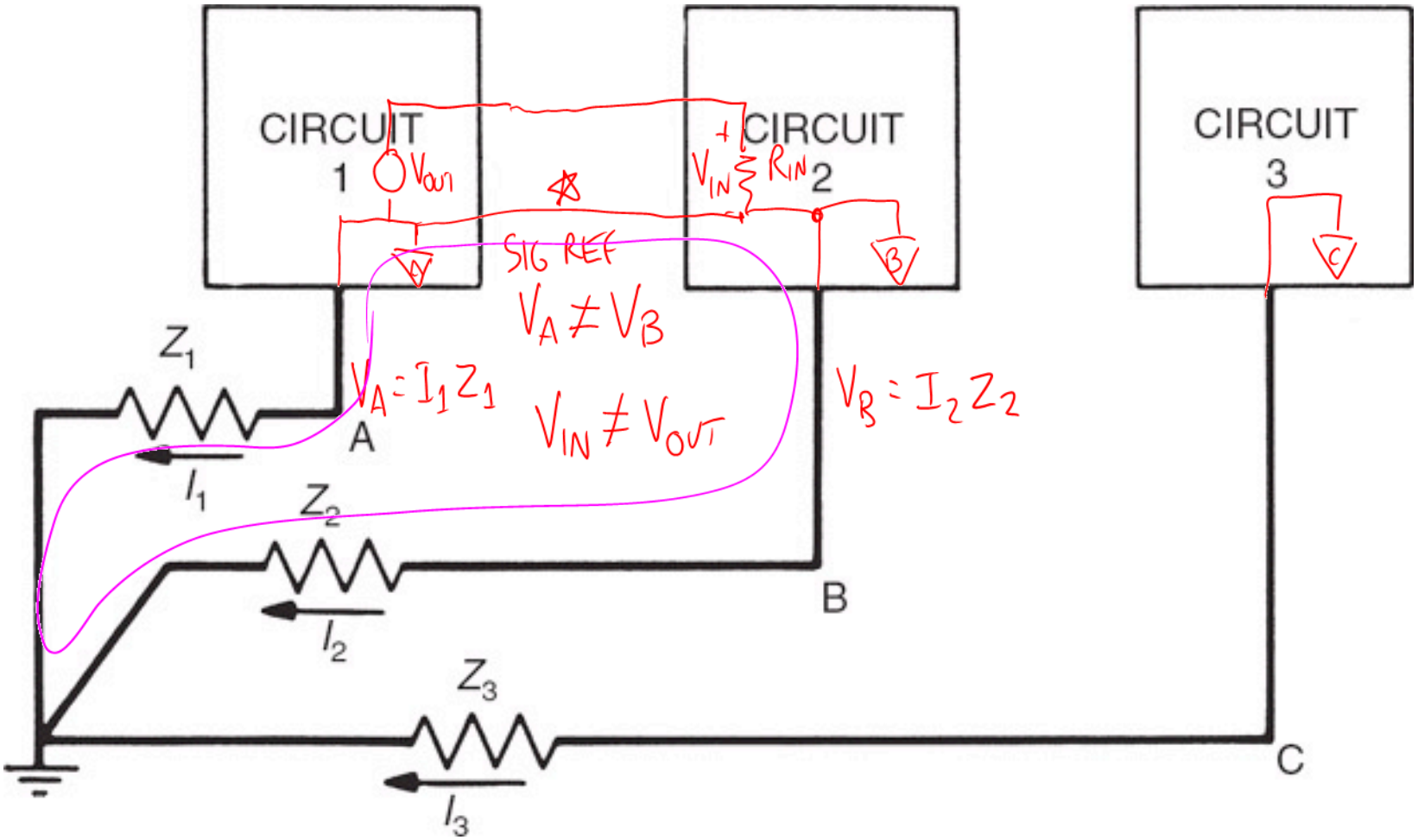
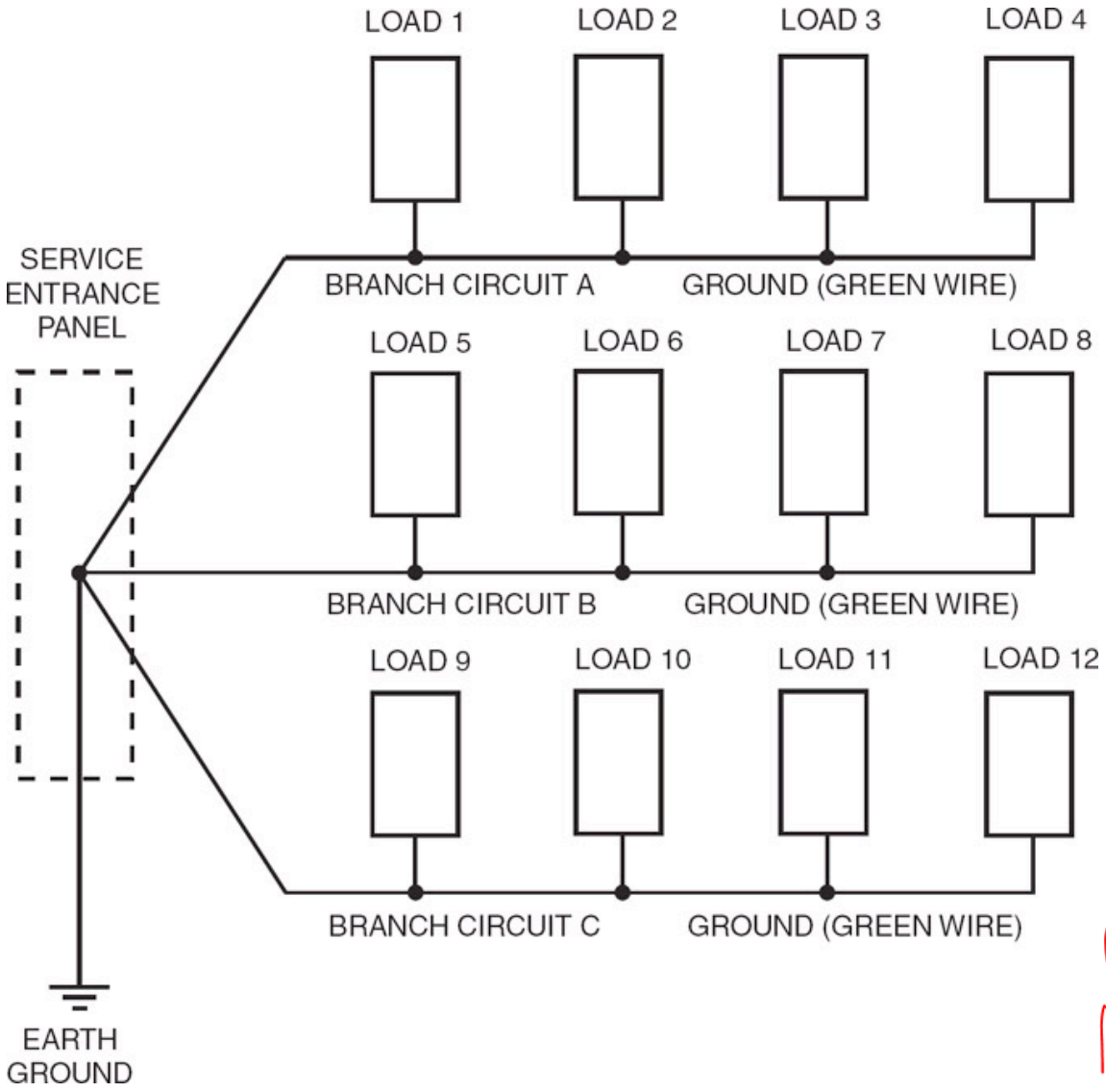


Figure 3-16: Separate, or parallel, single-point ground system is a parallel ground connection and provides good low-frequency grounding, but it may be mechanically cumbersome in large systems

TRY TO AVOID COMMON IMPEDANCE COUPLING BY FORCING I_1, I_2 DIFFERENT PATH

★ IF TIE $\frac{1}{C}$ TO $\frac{1}{B}$ VIOLATES "SEPARATE PATH" "GROUND LOOP"



STAR, DAISY CHAIN OK FOR SAFETY

60 Hz LIMIT V DIFFERENCE!

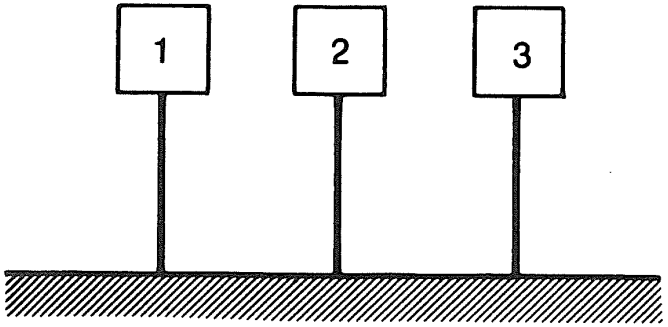
$|Z_L + Z_R| \ll 1\Omega$

FOR $f > 10\text{KHz}$ $|Z_L|$ TOO BIG

Figure 3-17: A single-point ac power ground, as per the NEC

NO GOOD FOR SIGNAL GROUND!

Multipoint Grounds



LOW IMPEDANCE PLANE

$Z_g \rightarrow 0$

Figure 3-14: Multipoint grounding connections

STILL HAVE COMMUNICATION ISSUE (MAYBE)

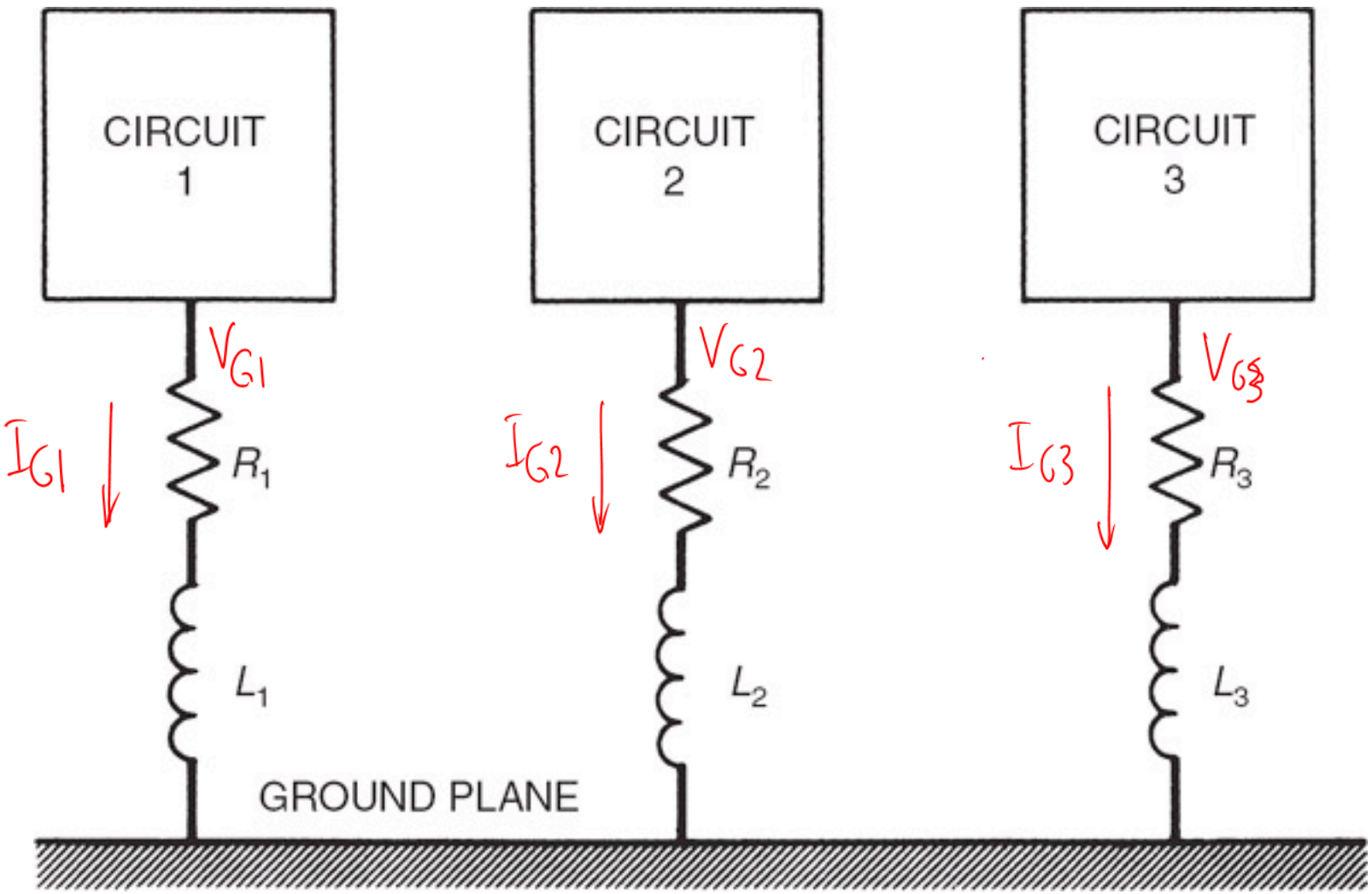


Figure 3-19: Multipoint ground system is a good choice at frequencies above about 100 kHz. Impedances $R_1 - R_3$ and $L_1 - L_3$ must be minimized at the frequency of interest

$V_{G1} \neq V_{G2} \neq V_{G3}$ Z_{G1}, Z_{G2}, Z_3 SMALL ENOUGH

OR: USE BLOCK-TO-BLOCK COMMUNICATION THAT CAN TOLERATE $V_{G1} = V_{G2}$

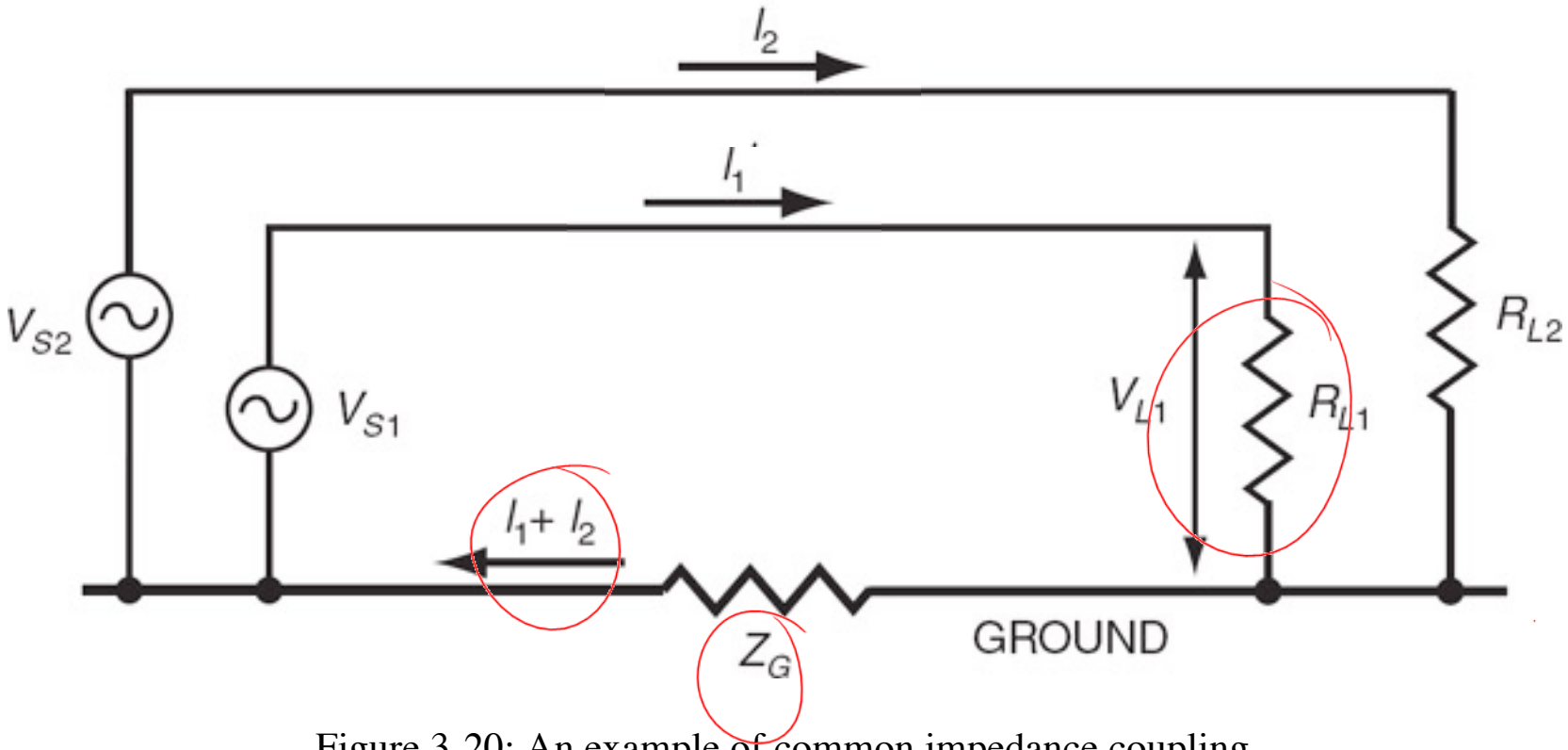
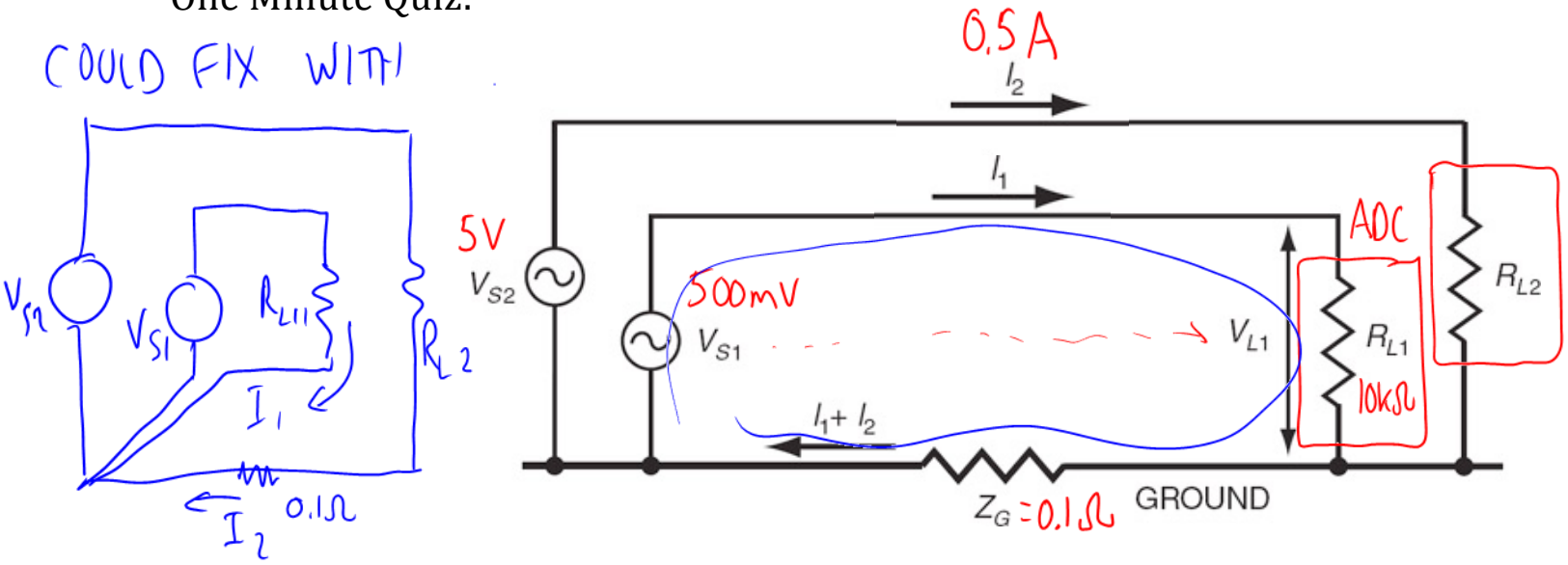


Figure 3-20: An example of common impedance coupling

Common impedance coupling becomes a problem when two or more circuits share a common ground and one or more of the following conditions exist:

1. A high-impedance ground (at high frequency, this is caused by too much inductance; at low-frequency this is caused by too much resistance).
2. A large ground current.
3. A very sensitive, low-noise margin circuit, connected to the ground.

One Minute Quiz:



V_{S1} is a 500mV signal source driving R_{L1} = 10 kΩ which is the input of an ADC with a 1mV LSB.
For accurate measurement we would like to have $V_{L1} = V_{S1}$.
V_{S2} is a 5V power supply providing 0.5A of current to circuitry represented by R_{L2}
Z_G = 0.1 Ω is the (DC) resistance of 100 feet of 10 AWG copper wire.

What is the error in V_{L1}? Express both in LSBs and as a fraction of the 500mV value of V_{S1}.

KVL: $V_{S1} - V_{L1} - (I_1 + I_2)Z_G = 0 \Rightarrow V_{L1} = V_{S1} - (I_1 + I_2)Z_G$

V_{L1}: OUT; V_{S1}: SIGNAL (WANT); $(I_1 + I_2)Z_G$: ERROR

$0.5\,A\,(0.1\,\Omega) = 50\,mV$ 50 LSB

500mV

10% ERROR!

Single-point grounds overcome these problems by separating ground currents that are likely to interfere with each other and by forcing them to flow on different conductors.
However, the signal current paths and long lead lengths associated with single-point grounds increase the inductance, which is detrimental at high frequencies.
In addition, at high frequencies, single-point grounds are almost impossible to achieve because parasitic capacitance closes the ground loop.
Multipoint grounds overcome these problems by producing a very low ground impedance, effectively controlling the L_g term in Eq. 3-1.
Normally, at frequencies below 100 kHz, a single-point ground system may be preferable; above 100 kHz, a multipoint ground system is best.

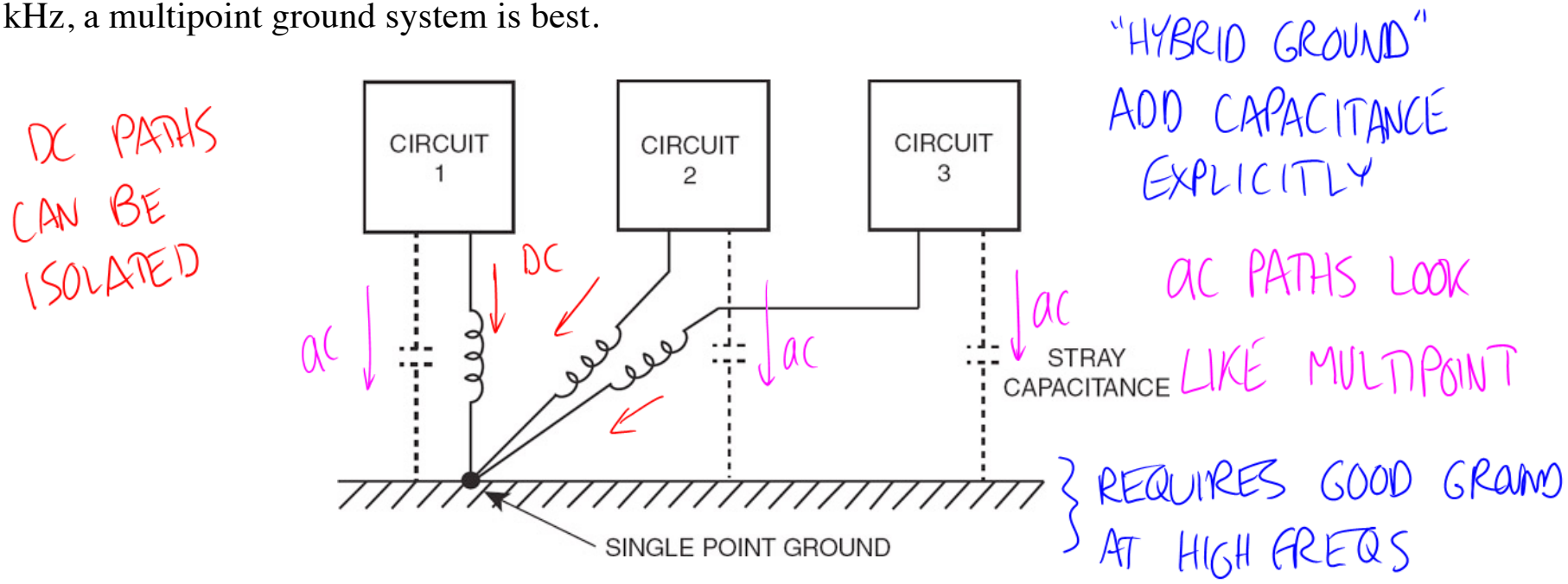


Figure 3-18: At high frequency, single-point grounds become multipoint grounds because of stray capacitance

Chassis Grounds

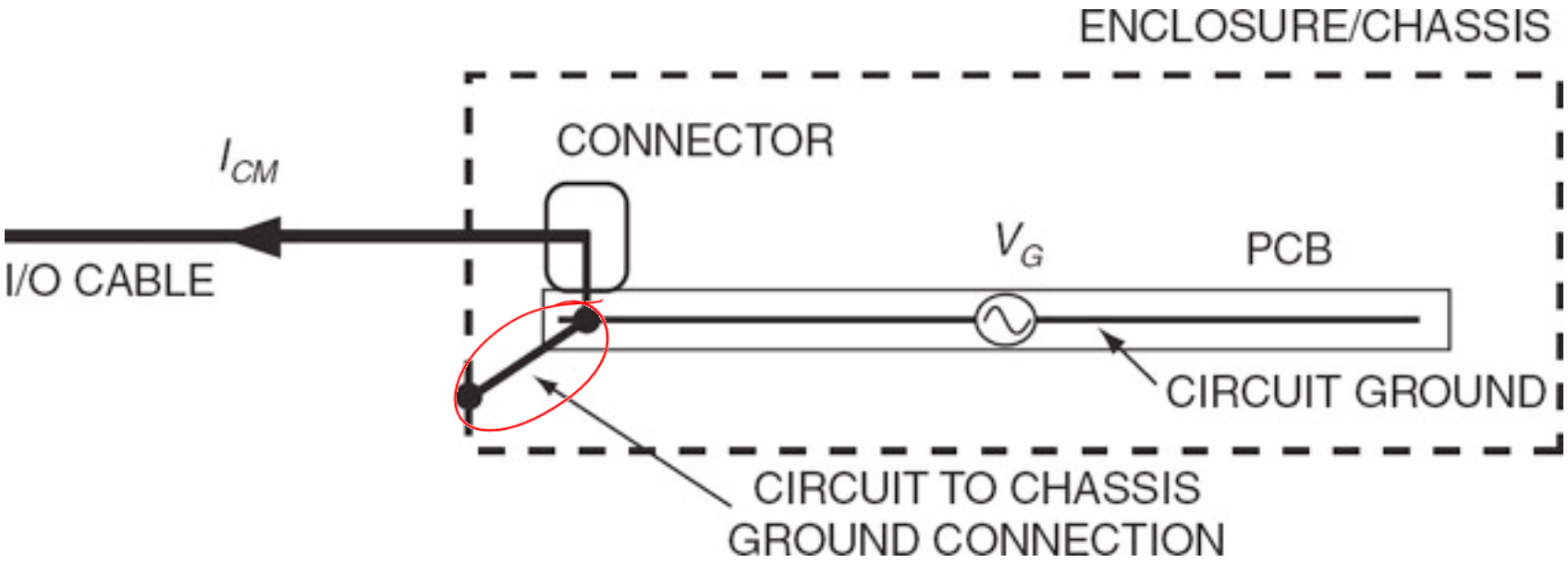
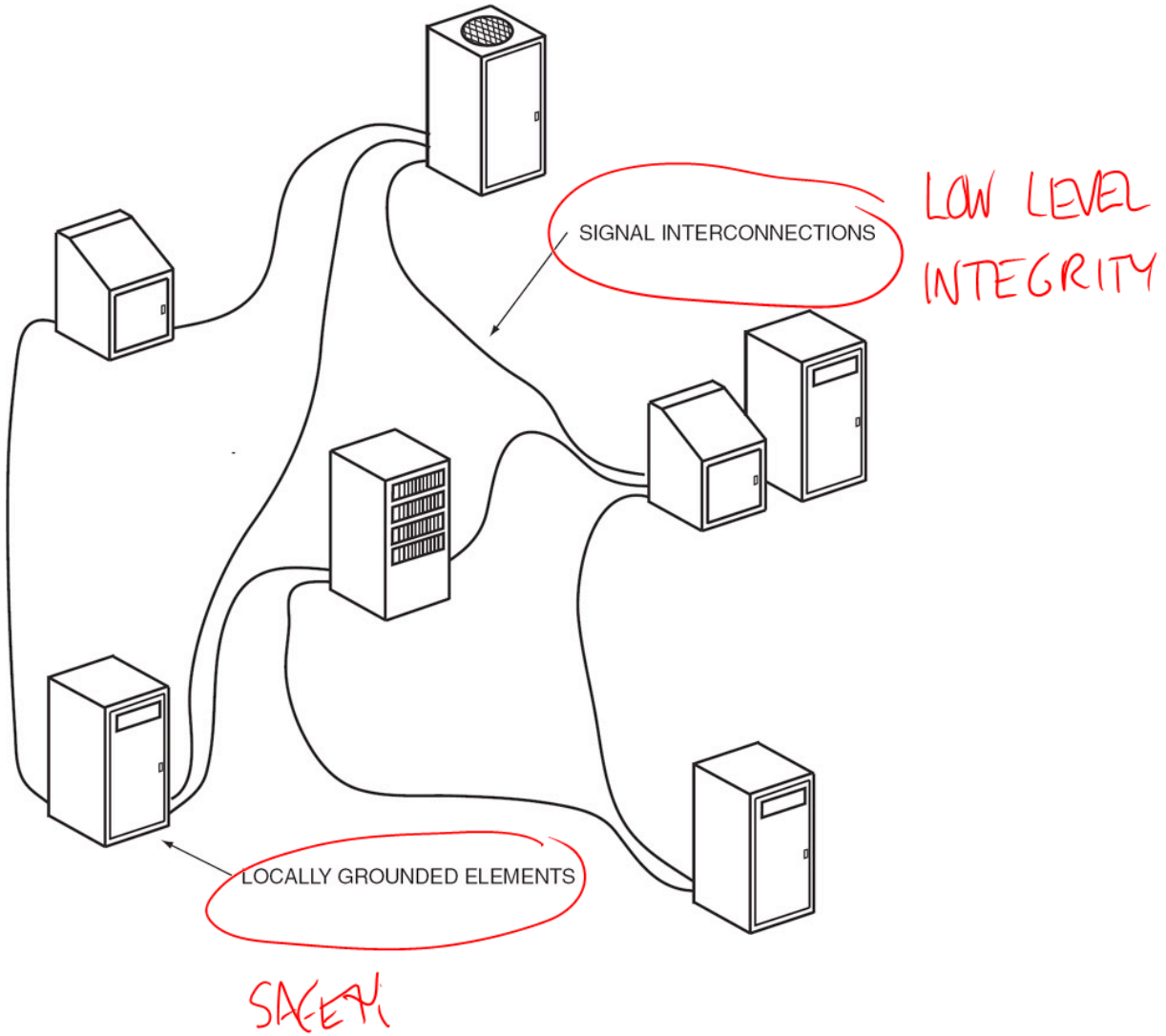


Figure 3-24:
Circuit ground should be connected to the enclosure (chassis) in the I/O area of the PCB

REASON: COMMON MODE EMI (MODULE 2)

SAFETY: COULD BE ANYWHERE

Figure 3-31: A distributed system that consists of a multiplicity of widely separated elements



Considerations in distributed systems:

- What are the characteristics of the signal? AMPLITUDE, f
- What type of cabling and/or filtering will be used?
- Is the signal analog or digital?
- What is its frequency and amplitude?
- Is the signal balanced or unbalanced? (Balanced signals are more immune to noise than unbalanced signals.)
- Will the cabling be individual wires, twisted pairs (shielded or unshielded), ribbon cable, or coax?
- If shields are used, should they be grounded at one end, both ends, or hybrid grounded?
- Another important consideration is can or will some form of isolation or filtering be used?
- For example, can the signal be transformer or optically coupled to the cable?
- Filters and common-mode chokes can also be used to treat the I/O signals and to minimize the noise coupling.

Grounding Strategies

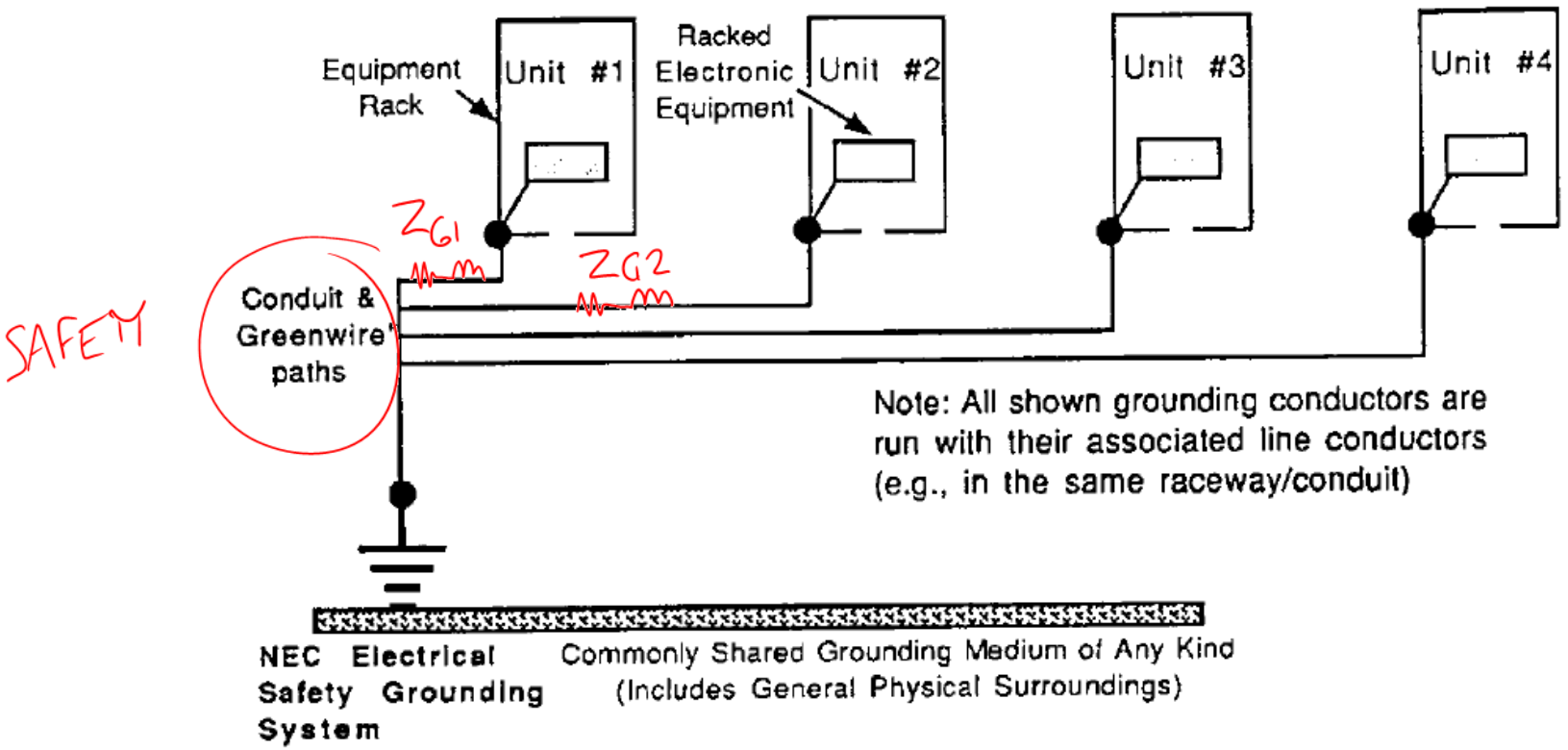
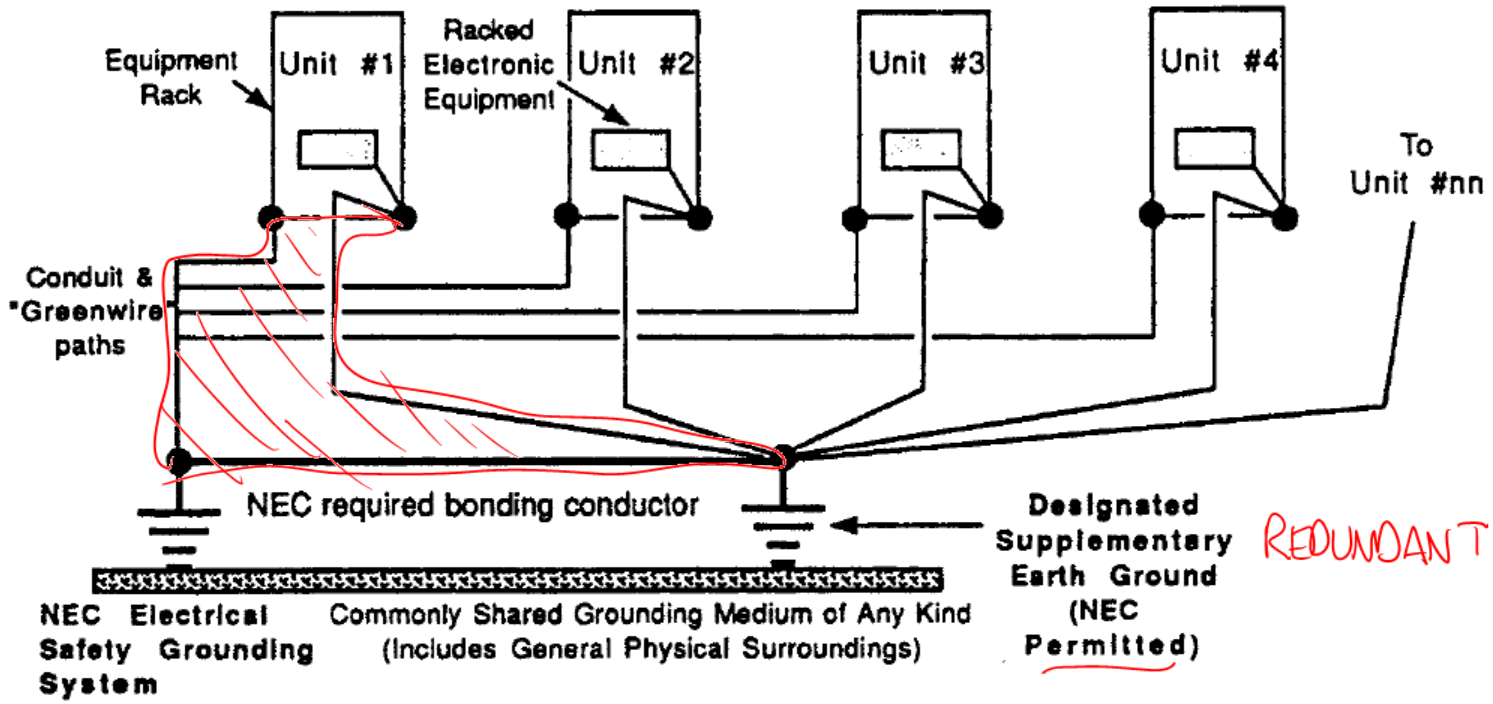


Figure 4-56—NEC-compliant equipment grounding for basic fault/personnel protection subsystem

Meets safety requirement but impedance may be too high for acceptable unti-to-unit "ground" potential variation

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

Grounding Strategies



LARGE LOOP AREA MAGNETIC FIELD COUPLING

REDUNDANT

Figure 4-57—NEC-compliant equipment and system grounding employing a supplementary grounding system consisting of an interconnected second electrode at its associated grounding conductors

Figure 4-57 shows an electronic system to which a supplementary grounding system has been attached.
Developed from Figure 4-56 by adding supplementary grounding conductors and related earth ground.
NEC-compliant, but is likely to also be electrically "noisy."
Also poor EMC practice because of the cabinet penetration by the supplementary grounding conductors.

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

Grounding Strategies

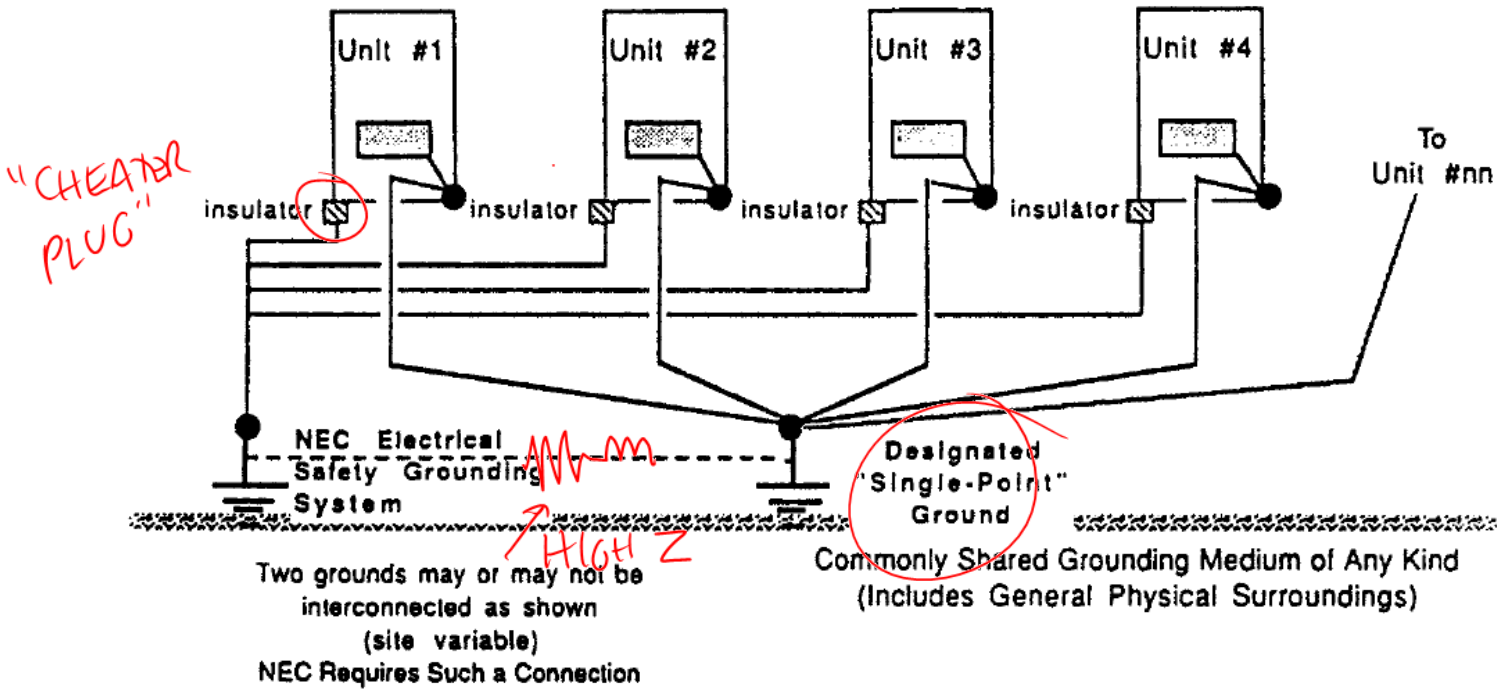


Figure 4-58—Non-NEC-compliant general configuration of an SPG design used with equipment being powered from building ac supply

X DON'T DO THIS

Figure 4-58 shows unsafe modification using "cheater plugs" to obtain a single point ground configuration. Does not meet NEC requirements due to broken equipment grounding paths in branch circuits at the point of connection to the load equipment.
Vulnerable to lightning and ground-fault current damage and is generally "noisy" as well.

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

"Zero Signal Reference Plane" (ZSRP)

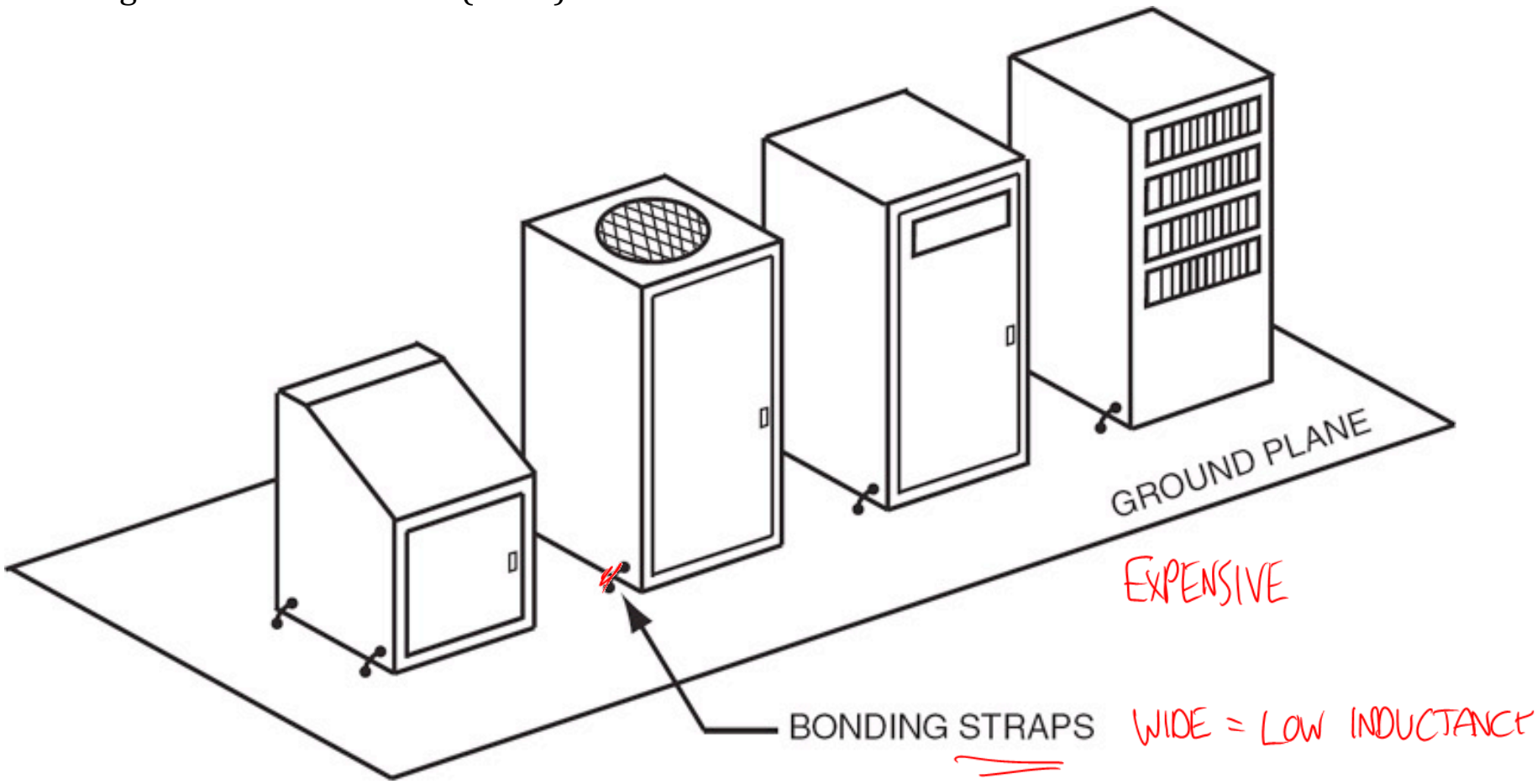


Figure 3-26: A ZSRP is the optimum way to provide a low-impedance ground connection between individual equipment enclosures that is effective over the widest frequency range

Much more in text section 3.3

Grounding Strategies

DON'T ALWAYS NEED EXPENSE OF SRS/ZSRP
SOLVE WITH BLOCK-BLOCK SIGNALING TECHNIQUES

The need for a signal reference structure (SRS) is minimal when **all of the inter-unit signal-level and telecommunication circuits are interfaced to the associated electronic equipment via optically or isolation transformer coupled means**, and where these interfaces have good common-mode voltage breakdown characteristics.

However, the need for an SRS may easily rise to that of a requirement in the event any of the following three conditions are established:

1) When the logic ac-dc power supplies used in the associated electronic equipment are installed with one of the terminals (e.g., the "common") connected to the equipment's metal frame/enclosure. This is typical and recommended practice in the commercial ITE and electrical business equipment industries, and others as well.

2) When the signal-level circuits and logic ac-dc power supply common terminals are OEM dielectrically insulated or galvanically isolated from equipment ground against recommended practice, and are instead connected to an insulated "ground" terminal that is intended for connection to an externally installed signal ground reference circuit.

3) There are actual performance problems occurring with the equipment, which can be assigned to common-mode electrical noise or similar common-mode interference related to the equipment's existing grounding system, whatever its design, or to the signal-level inter-unit cabling system.

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

"Single Point Ground" Impedance Issue

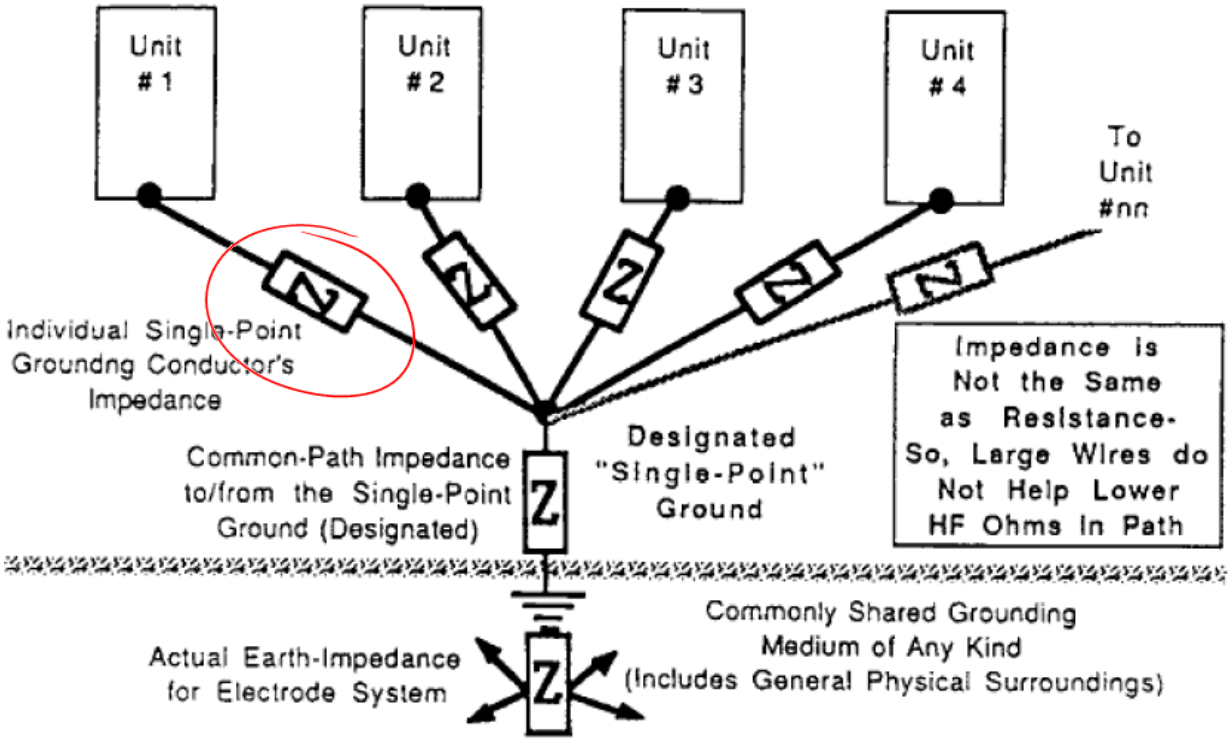


Figure 4-63—Typical Z = R ± jX impedance values

Meets safety requirement but impedance may be too high for acceptable unit-to-unit "ground" potential variation

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

Grounding Strategies

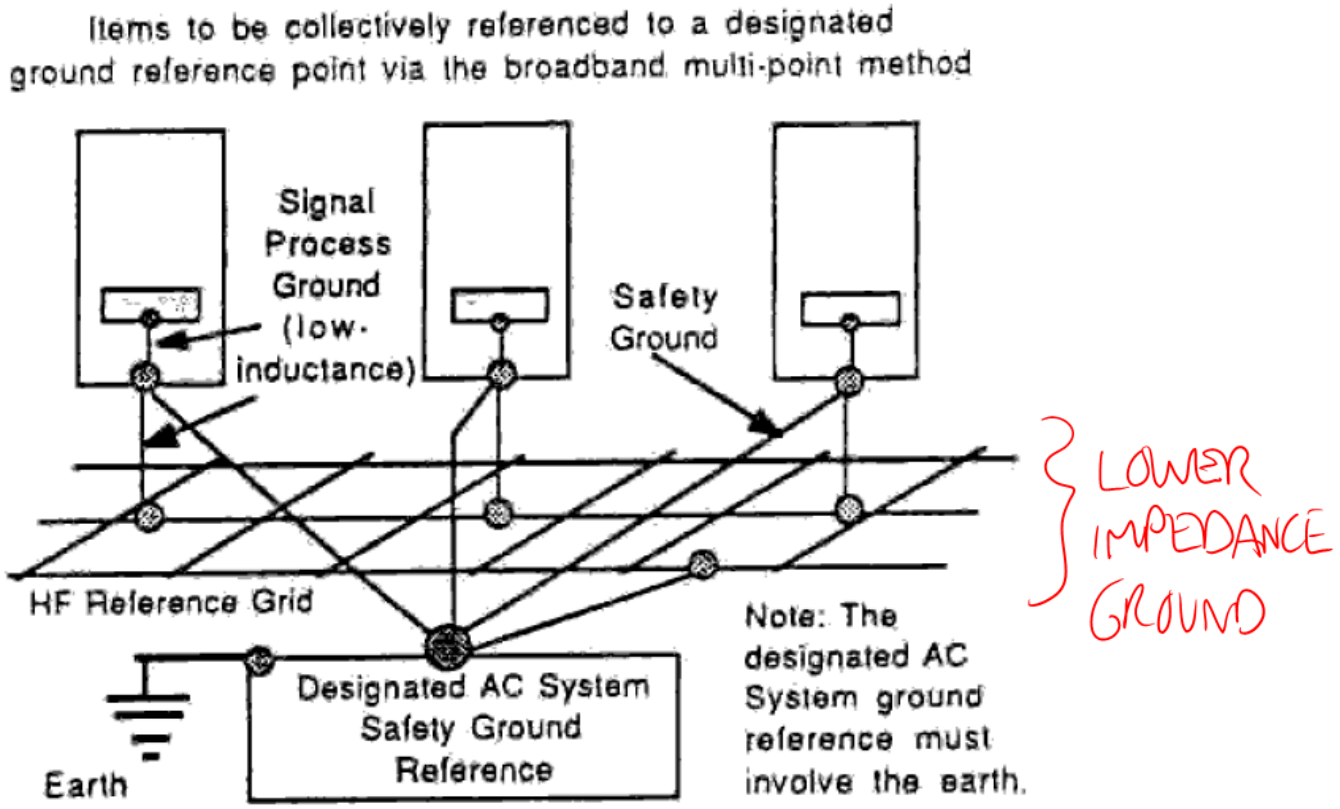


Figure 4-64—Recommended practice (simplified diagram) for dc—high-frequency grounding of electronic systems powered from building ac power system

Low impedance paths for current at both low and high frequencies

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

Much better impedance over frequency performance:

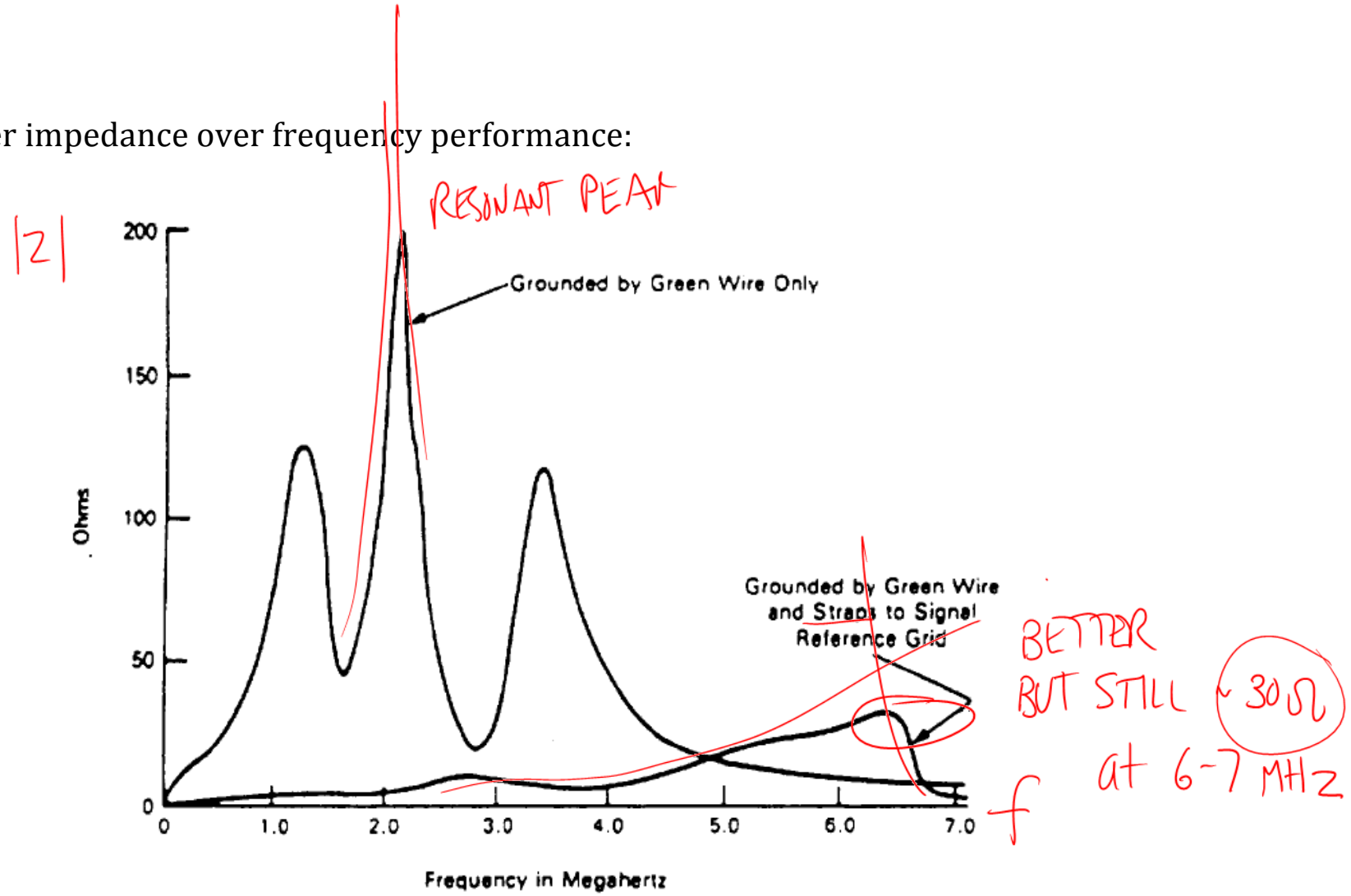


Figure 4-66—Impedance of grounding conductors for a computer system

Decision: Isolate critical signal & return paths to avoid need for ZSRP?

Source: IEEE Std. 1100-2005, available at ieeexplore.ieee.org

Ground Loops

Figure 3-33 shows a system grounded at two different points. Two different ground symbols are shown in the figure to emphasize the fact that the two physically separated ground points are likely to be at different potentials. This configuration has three potential problems, as follows:

1. A difference in ground potential V_G between the two grounds may couple a noise voltage V_N into the circuit as shown in Fig. 3-33. The ground potential is usually the result of other currents flowing through the ground impedance.
2. Any strong magnetic fields can induce a noise voltage into the loop formed by the signal conductors and the ground, which is designated as "ground loop" in Fig. 3-33.
3. The signal current has multiple return paths and may, especially at low-frequency, flow through the ground connection and not return on the signal return conductor.

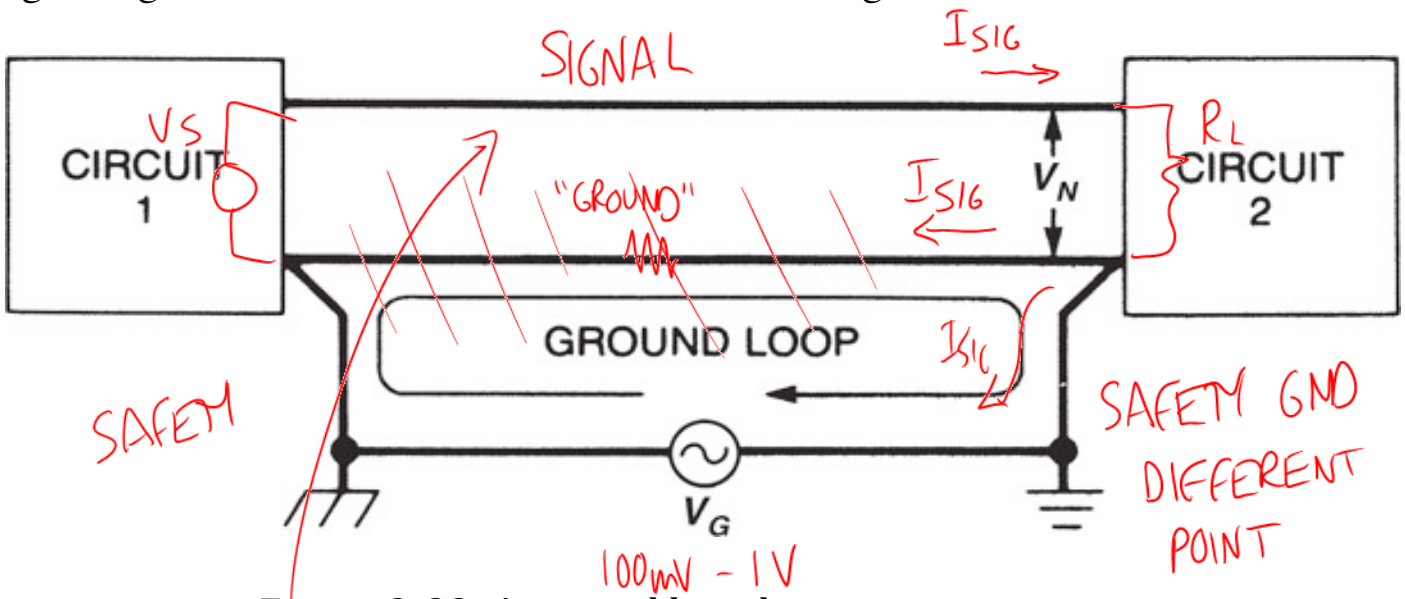


Figure 3-33: A ground loop between two circuits

- All ground loops are not bad, and some ground loops are benign.
- Most actual ground-loop problems occur at low frequency, under 100 kHz, and they are usually associated with sensitive analog circuits, such as audio or instrumentation systems. Classic example: 50/60-Hz hum coupling into an audio system.
- Ground loops are seldom a problem at high frequency, above 100 kHz, or in digital systems.
- Some ground loops are actually helpful, for example, in the case of a cable shield being grounded at both ends in order to provide magnetic field shielding (see text section 2.5)

If ground loops are a problem, then they can be dealt with in one of three ways as follows:

1. Avoid them by using single-point or hybrid grounds. This technique is usually only effective at low frequencies, and often it makes the situation worse when attempted at high frequency.
2. Tolerate them by minimizing ground impedance (e.g., by using a ZSRP) and/or by increasing the circuit noise margin (e.g, by increasing the signal voltage level or by using a balanced circuit).
3. Break them by using one of the techniques discussed below.

The ground loop shown in Fig. 3-33 can be broken by one of the following:

1. Transformers
2. Common-mode chokes
3. Optical couplers

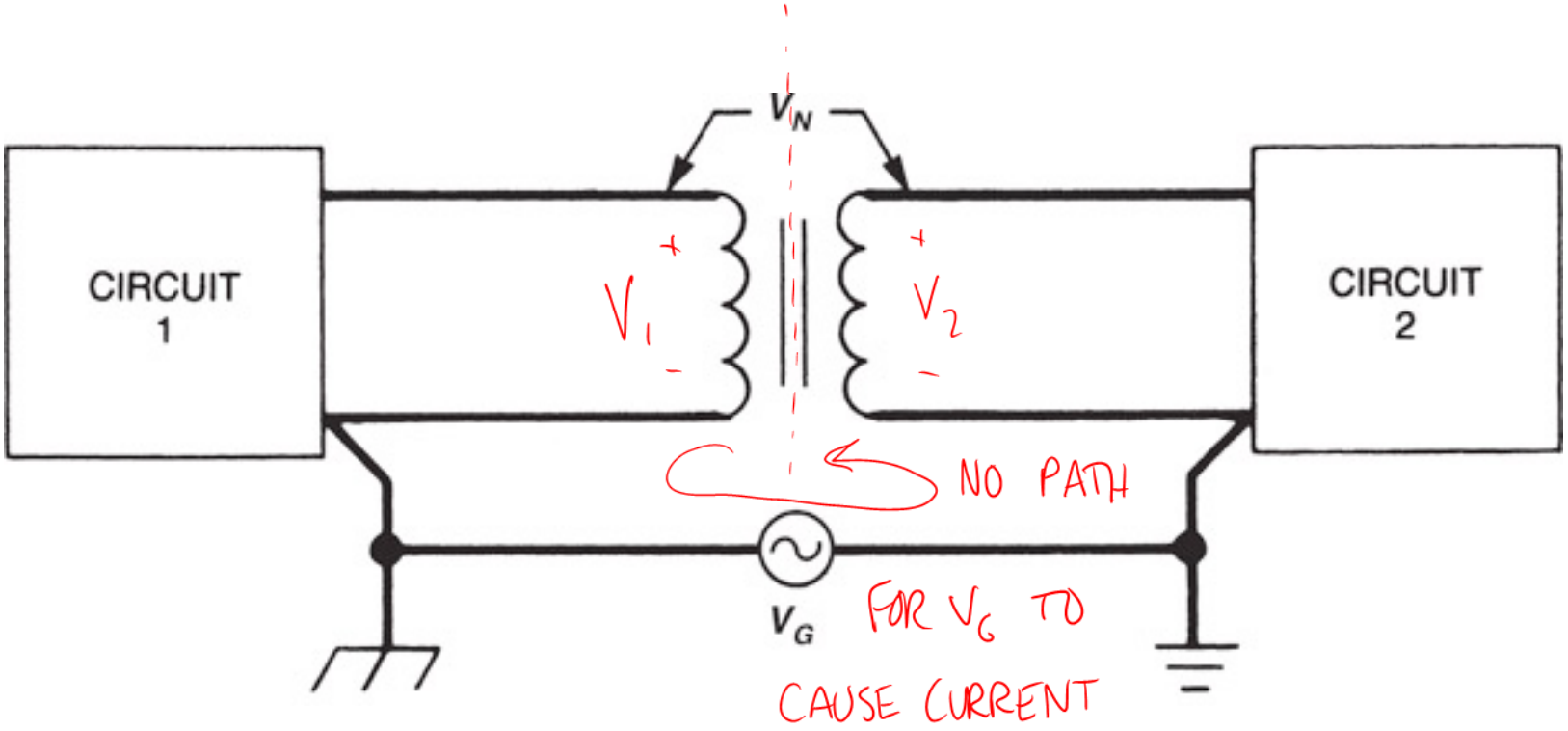


Figure 3-34: A transformer used to break a ground loop ground between two circuits

INHERENTLY DIFFERENTIAL

IF DC CONTINUITY NOT NEEDED

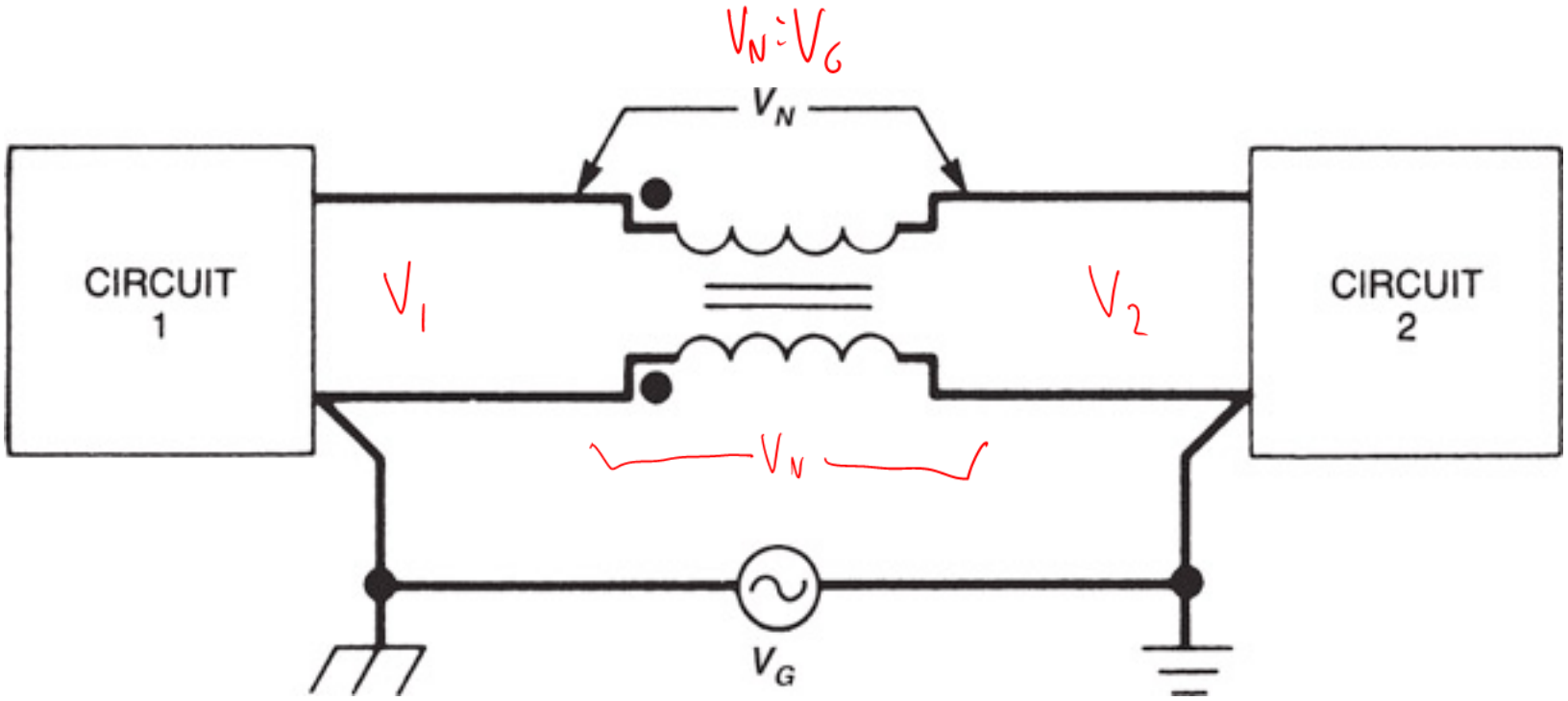


Figure 3-36: A common-mode choke used to break the ground loop between two circuits

PRESENTS HIGH IMPEDANCE TO COMMON MODE V_G

DIFFERENTIAL V_1, V_2 SAME

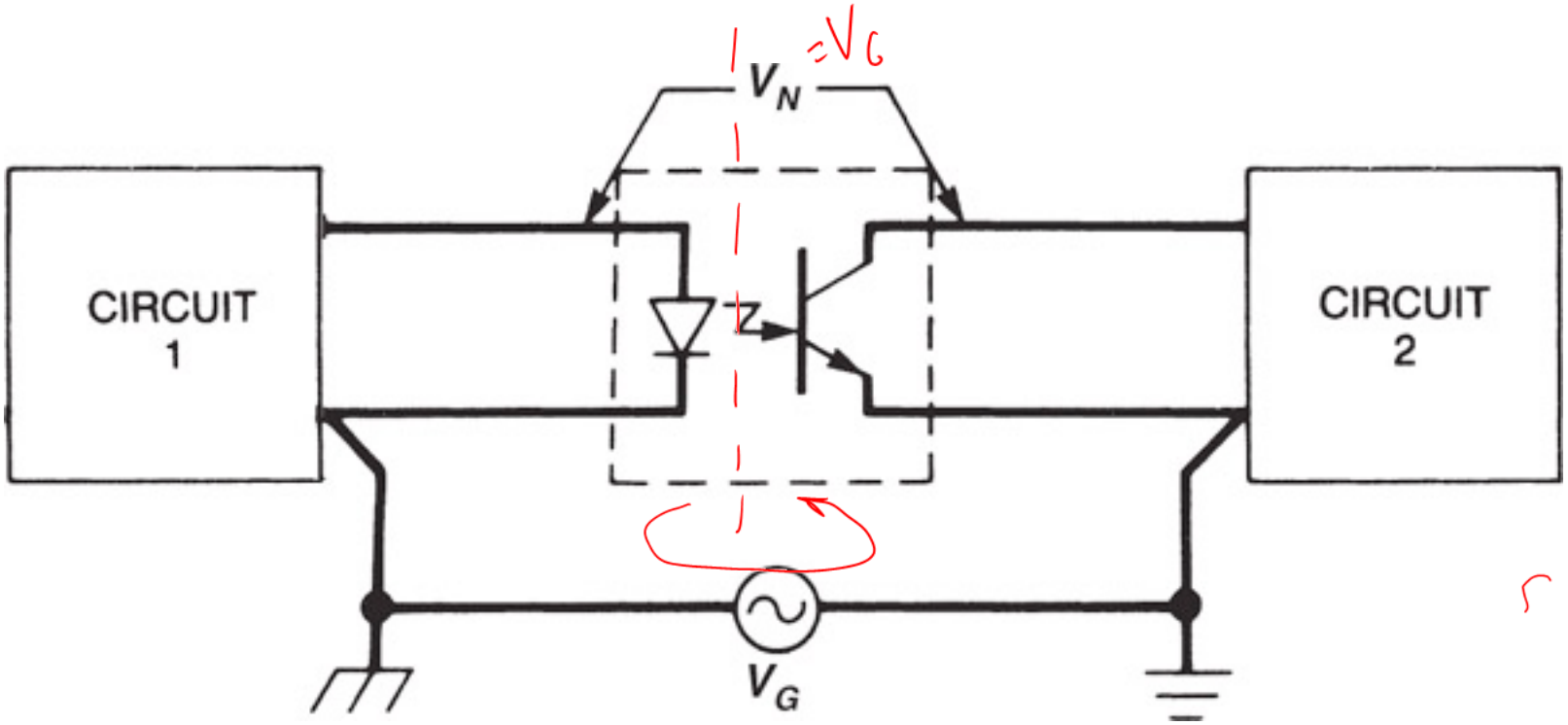


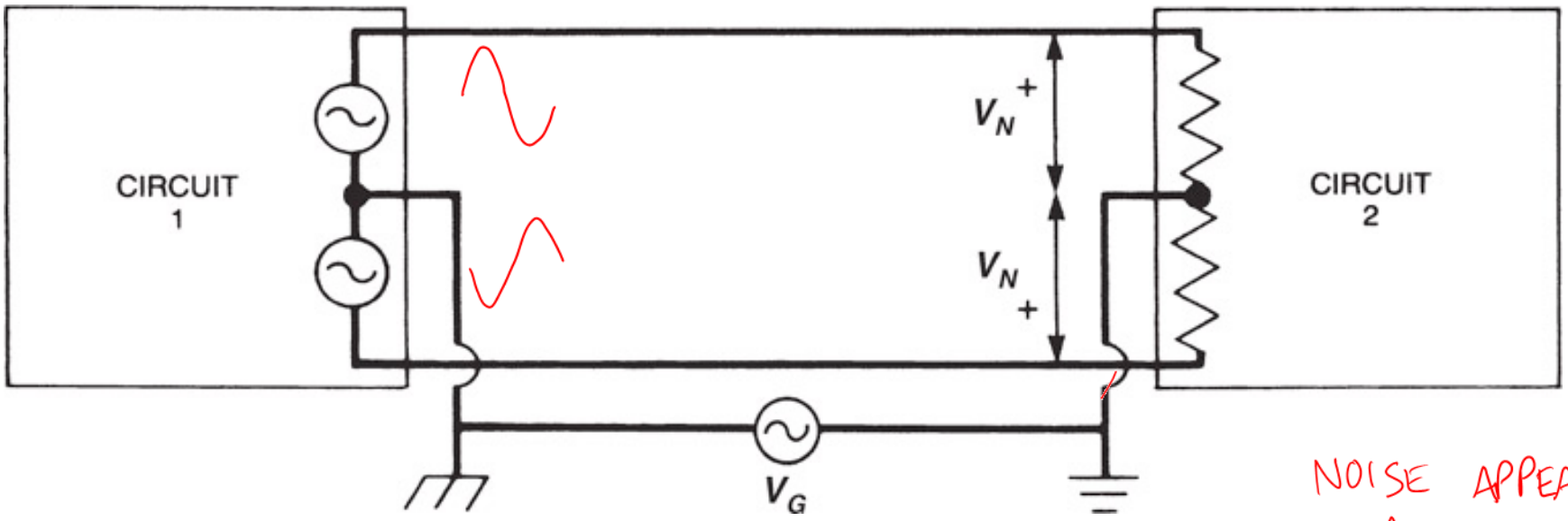
Figure 3-37: An optical coupler used to break the ground loop between two circuits

NO PATH FOR V_G TO CAUSE CURRENT

GREAT FOR DIGITAL

HARDER FOR ACCURATE ANALOG

SIGNAL



NOISE APPEARS AS COMMON MODE

Figure 3-38: A balanced circuit can be used to cancel out the effect of a ground loop

SUBTRACTED OUT

CANCELLATION NEVER PERFECT

MATCHING CAN USUALLY BE MADE GOOD ENOUGH

Common-Mode Choke (Low Frequency)

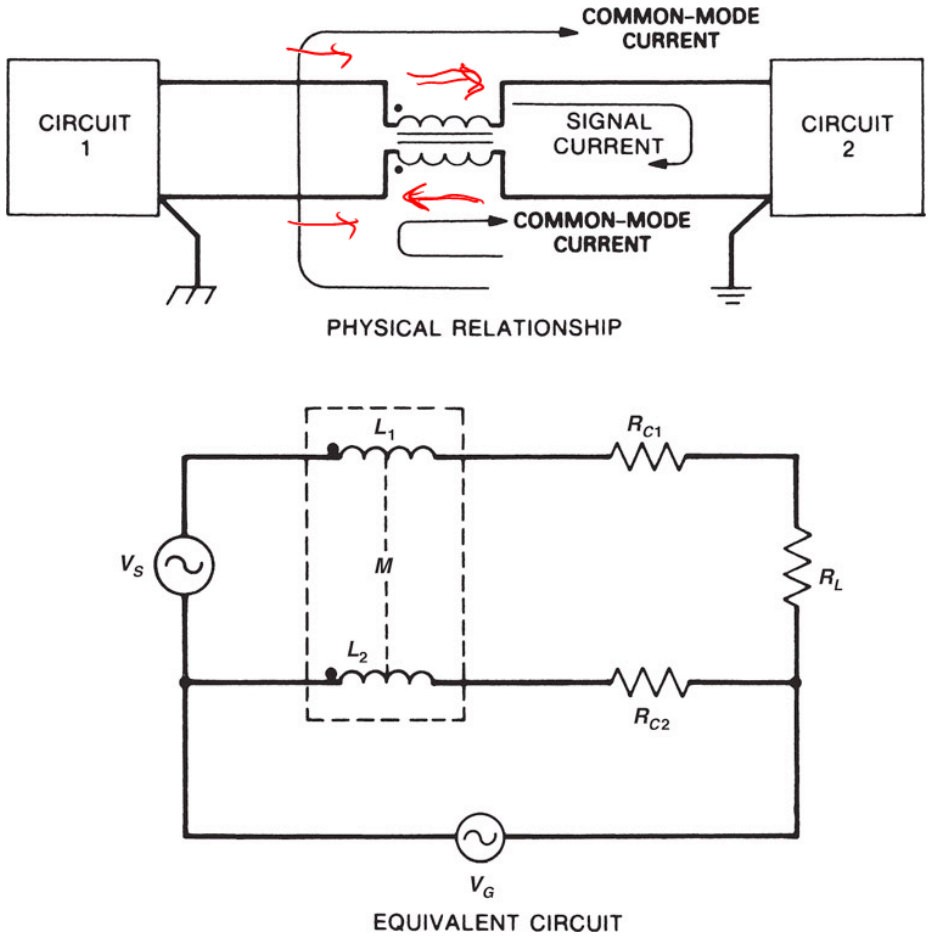


Figure 3-39: When dc or low-frequency continuity is required, a common-mode choke can be used to break a ground loop

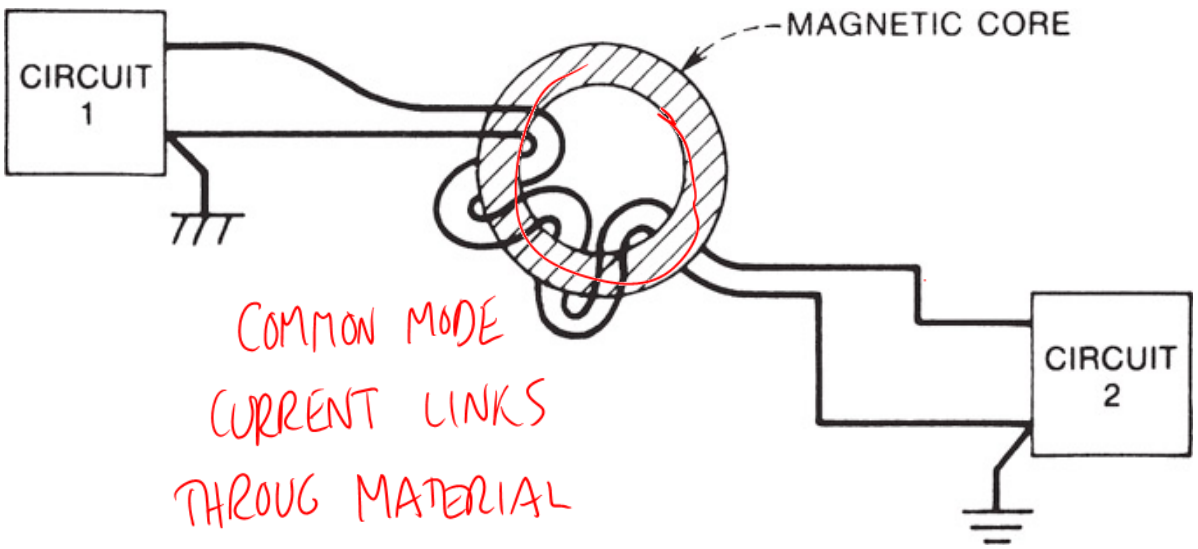


Figure 3-43: An easy way to place a common-mode choke in the circuit is to wind both conductors around a torodial magnetic core. A coaxial cable may also be used in place of the conductors shown

Common-Mode Choke (High Frequency)

PARASITIC CAPACITIVE COUPLING

LOW Z PATH FROM V_{CM} TO LOAD

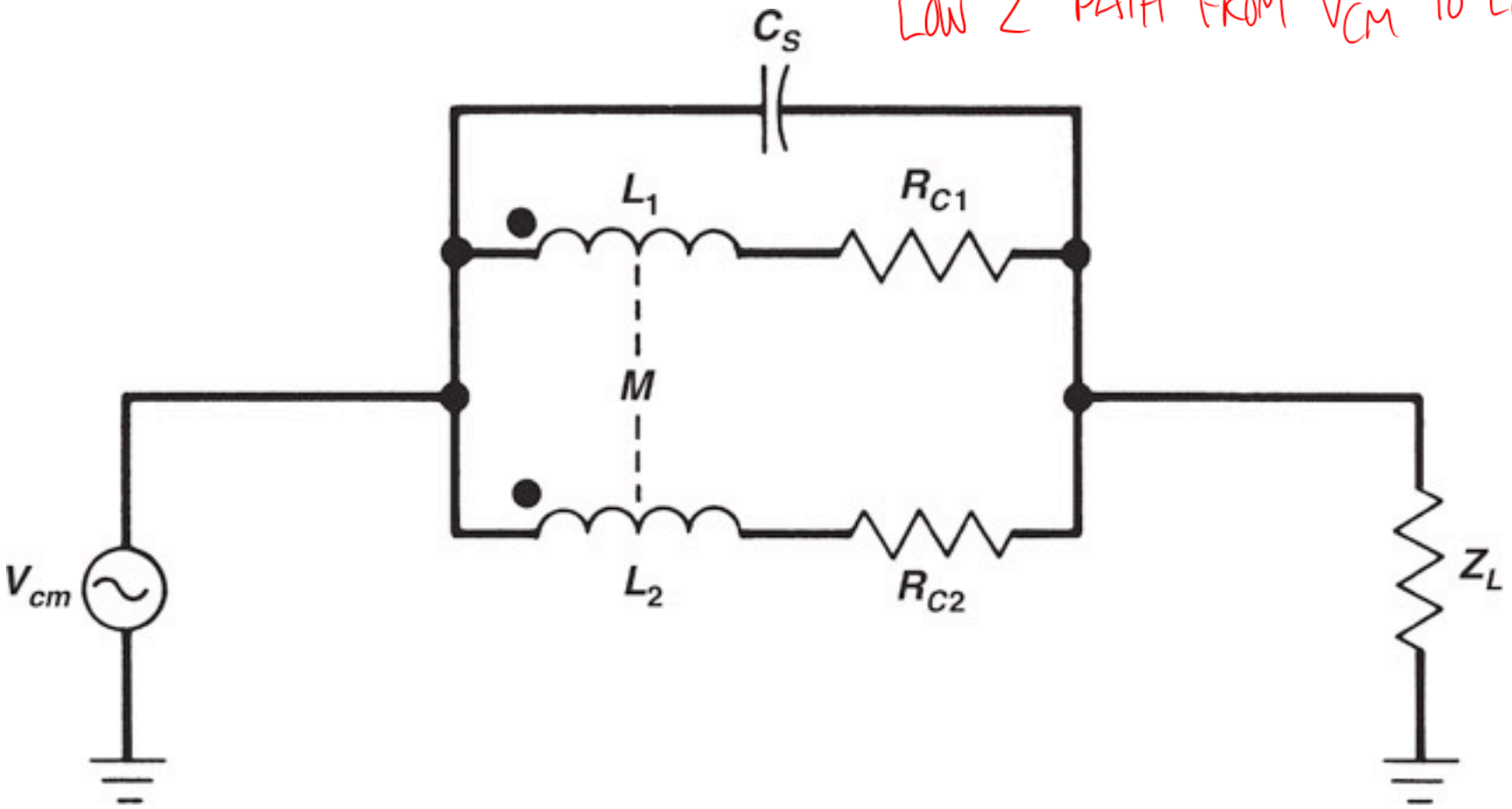


Figure 3-44: Equivalent circuit of a common-mode choke with parasitic shunt capacitance C_S

Insertion loss above 70 MHz does not vary much with the inductance of the choke; however, it varies considerably as a function of the shunt capacitance.
The most important parameter in determining the performance of the choke is the shunt capacitance and not the value of inductance.
The presence of the parasitic capacitance severely limits the maximum insertion loss possible at high frequencies.

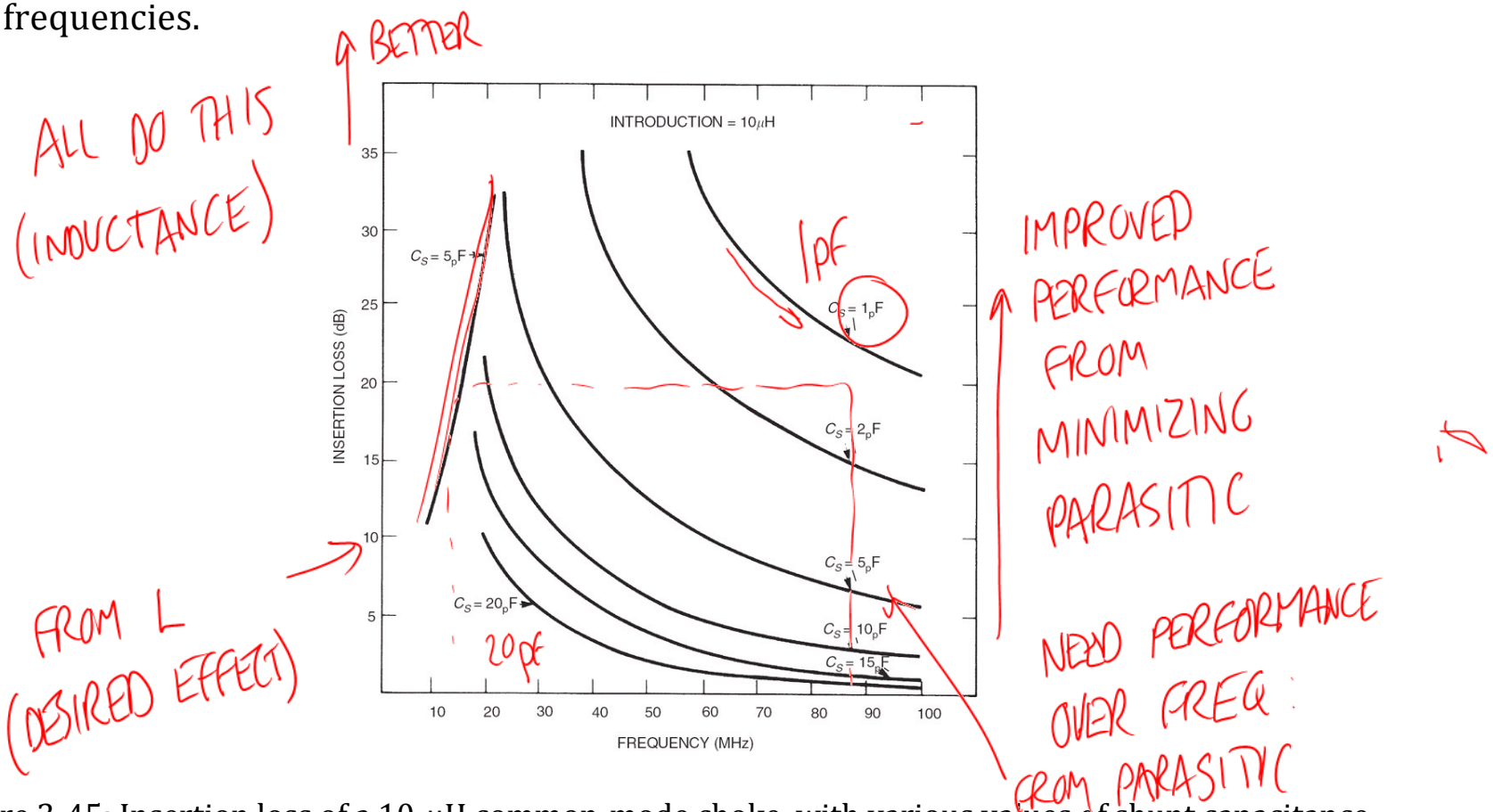


Figure 3-45: Insertion loss of a 10-μH common-mode choke, with various values of shunt capacitance

Summary: Grounding

- All conductors have finite impedance, which consists of both resistance and inductance.
- A ground conductor longer than 1/20 wavelength is not a low impedance.
- Grounds fall into two categories, safety grounds and signal grounds.
- The ac power ground is of little practical value as a signal ground.
- The earth is not a low impedance and is polluted with noisy power currents; not equipotential.
- Make connections to earth ground only when required for safety.
- Do not look to an earth ground as a solution to your EMC problems.
- Single-point grounds should only be used at low frequencies, typically below 100 kHz.
- Use multipoint grounds at high frequencies, typically above 100 kHz, and with digital circuits.
- One purpose of a good ground system is to minimize the noise voltage produced when two or more ground currents flow through a common ground impedance.
- The best way to make a low-impedance ground connection over the widest range of frequencies, between separate pieces of equipment, is by connecting them with a plane or grid.
- To minimize ground noise voltage,
- At low-frequency, control the ground topology (direct the current).
- At high-frequency, control the ground impedance.
- Ground loops can be controlled by:
- Avoiding them
- Tolerating them
- Breaking them
- Three common ways to break a ground loop are:
- Isolation transformers
- Common-mode chokes
- Optical couplers

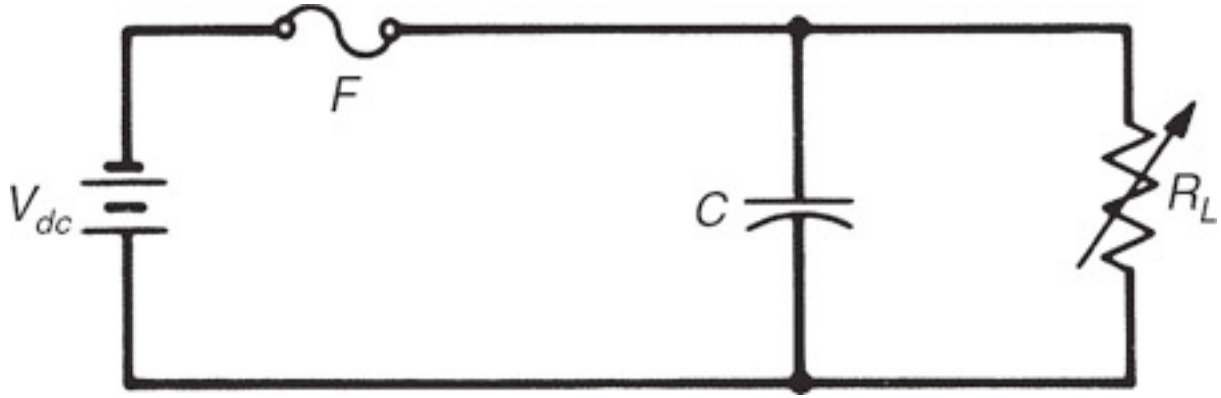


Figure 4-14: A dc power distribution system as it might appear on schematic

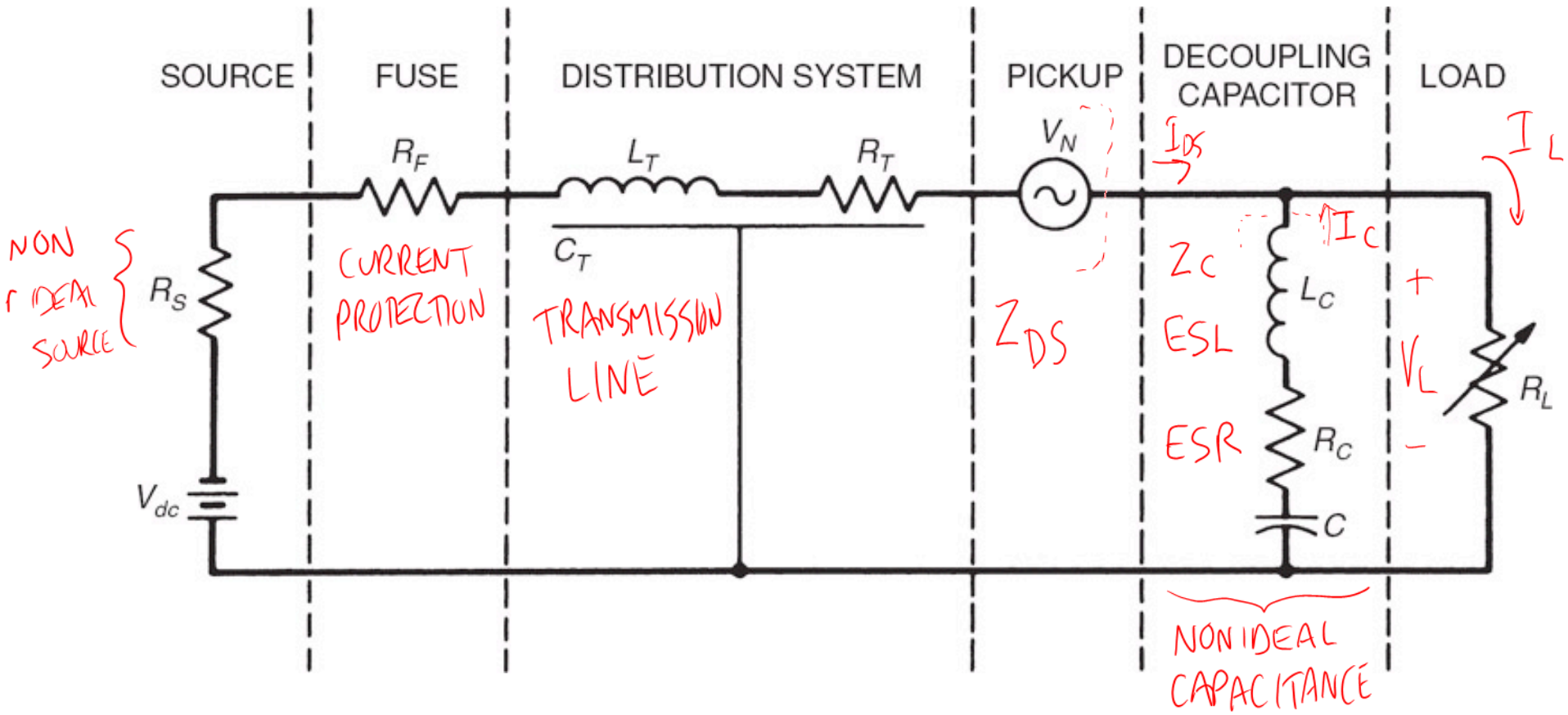


Figure 4-15: The actual circuit for a dc power distribution system, including parasitics

WHAT HAPPENS TO (IDEALLY CONSTANT) V_L AS A FUNCTION OF I_L

TRANSIENTS. WANT $|Z_C| \ll |Z_{DS}|$

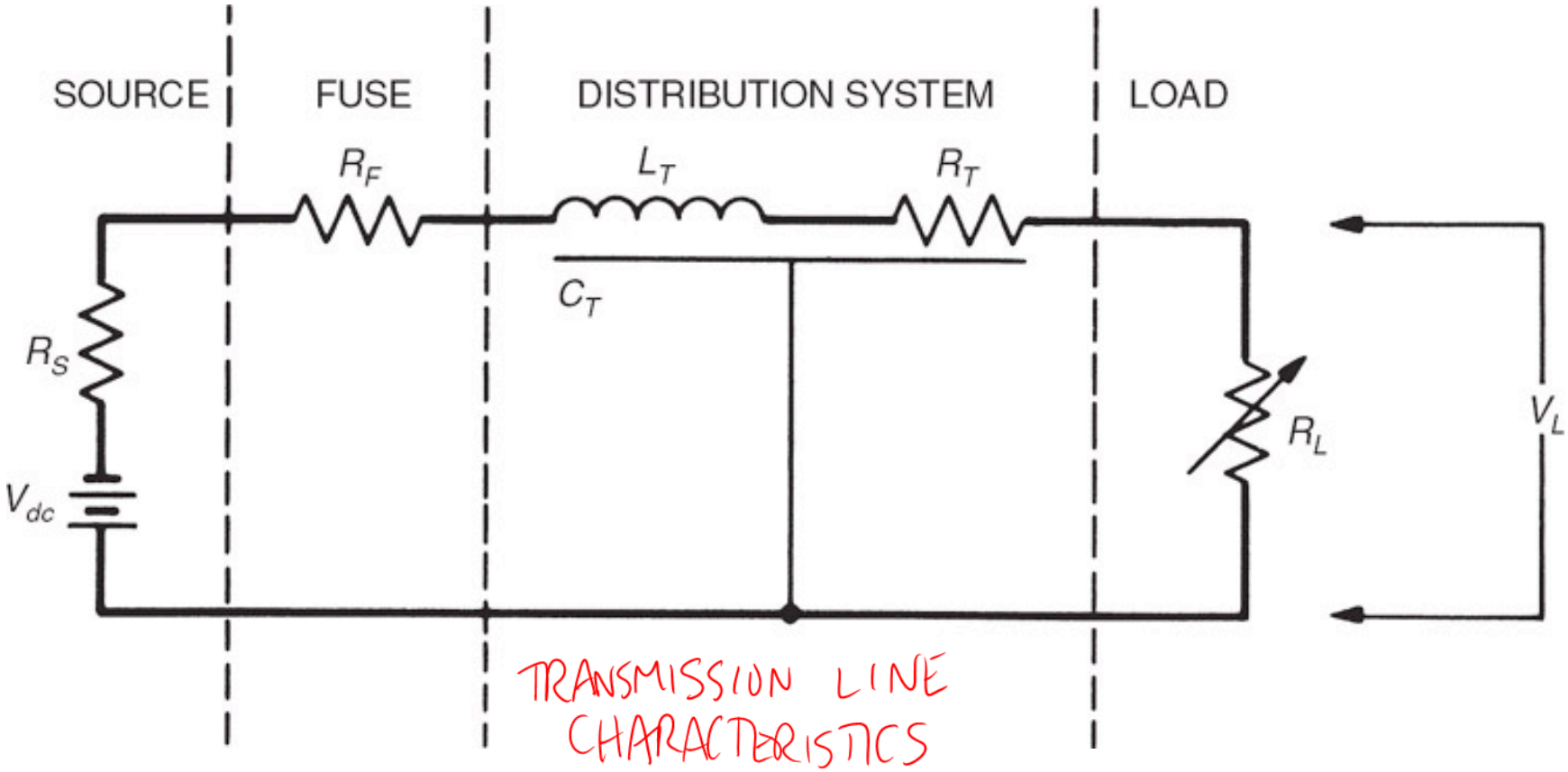


Figure 4-16: Circuit of Fig. 4-15, less the decoupling capacitor and noise pickup voltage

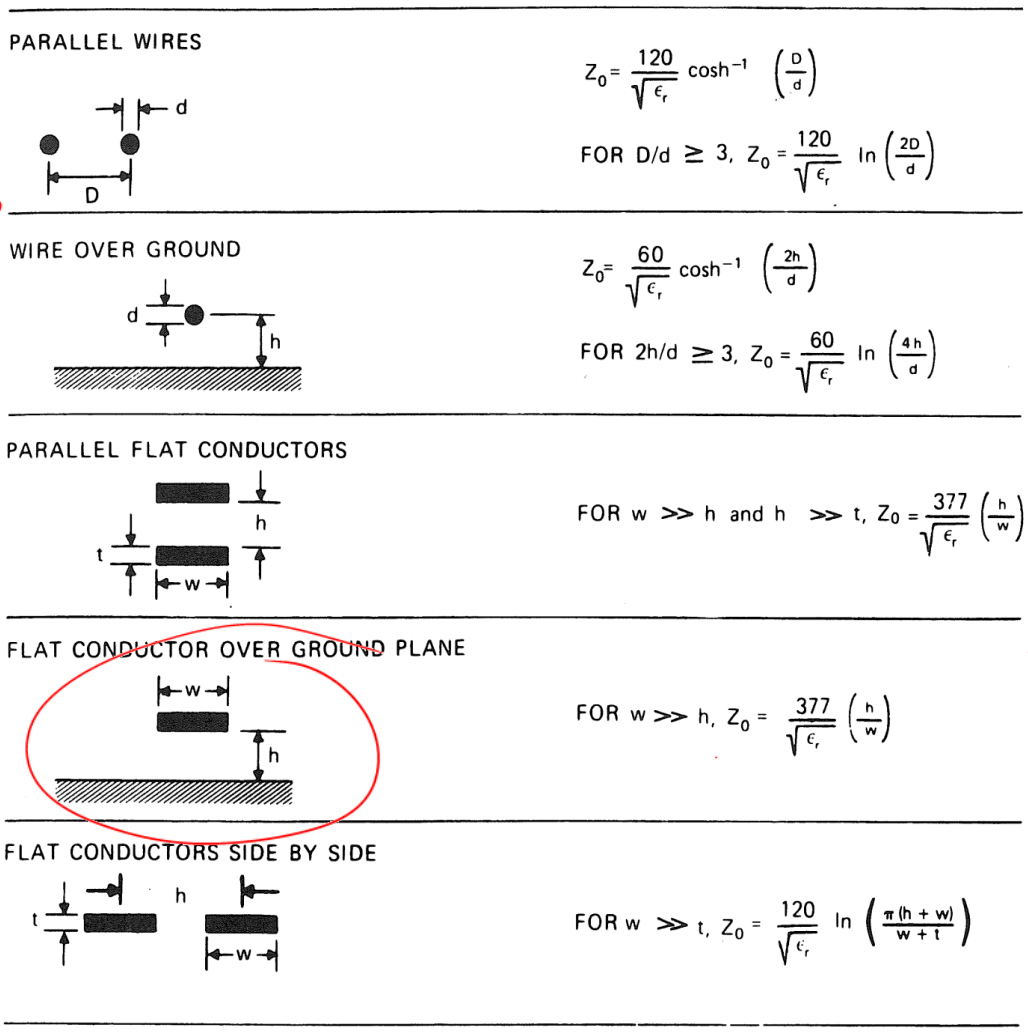


Table 4-3: Relative Dielectric Constants of Various Materials

Material	ε_r
Air	1
Styrofoam	1.03
Polyethylene foam	1.6
Cellular polyethylene	1.8
Teflon_[a]	2.1
Polyethylene	2.3
Polystyrene	2.5
Nylon	3
Silicone rubber	3.1
Polyester	3.2
Polyvinylchloride	3.5
Epoxy resin	3.6
Delrin™	3.7
Getek_[a]	3.9
Epoxy glass	4.5
Mylar_[b]	5
Polyurethane	7
Glass	7.5
Ceramic	9

Figure 4-17: Characteristic impedance for various conductor configurations

One Minute Quiz:

DC power is distributed on a 0.1" trace of 1oz. copper on an epoxy resin PCB, 0.032" above a solid ground plane.

What is the characteristic impedance?

How wide should the trace be for an impedance of 5Ω ?

$$Z = \frac{377\Omega}{\sqrt{3.6}} \frac{0.032}{0.1} = 63\Omega$$

FOR 5Ω : DESIGN

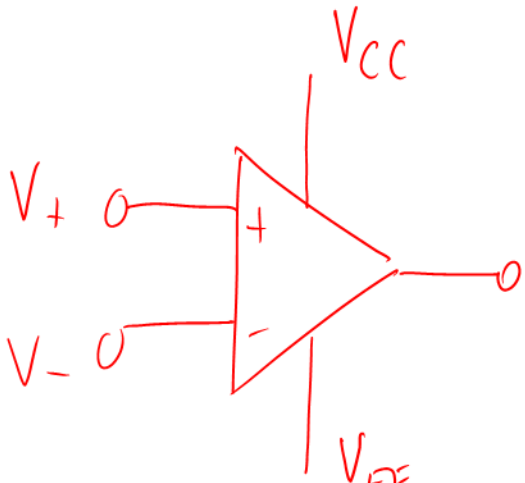
$$5\Omega = \frac{377\Omega}{\sqrt{3.6}} \frac{0.032}{W} \Rightarrow W = 1.2"$$

LOW Z WIDE TRACE W ↑

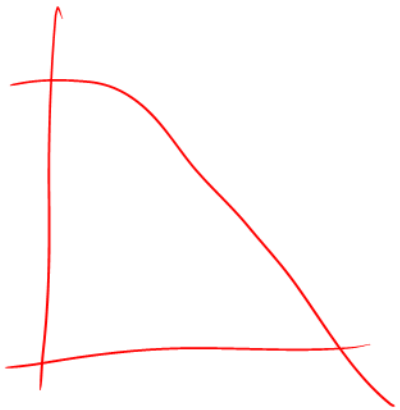
CLOSE TO GND RETURN h ↓

POWER SUPPLY REJECTION RATIO PSRR

OP-AMP (EXAMPLE)



$$V_{OUT} = \underbrace{A_{OL}}_{\text{OPEN LOOP GAIN}}\underbrace{(V_+ - V_-)}_{\text{SIGNAL}} + \underbrace{A_{PS}}_{\text{IDEALLY ZERO}}\underbrace{(V_{CC} - V_{EE})}_{\text{SUPPLY}}$$

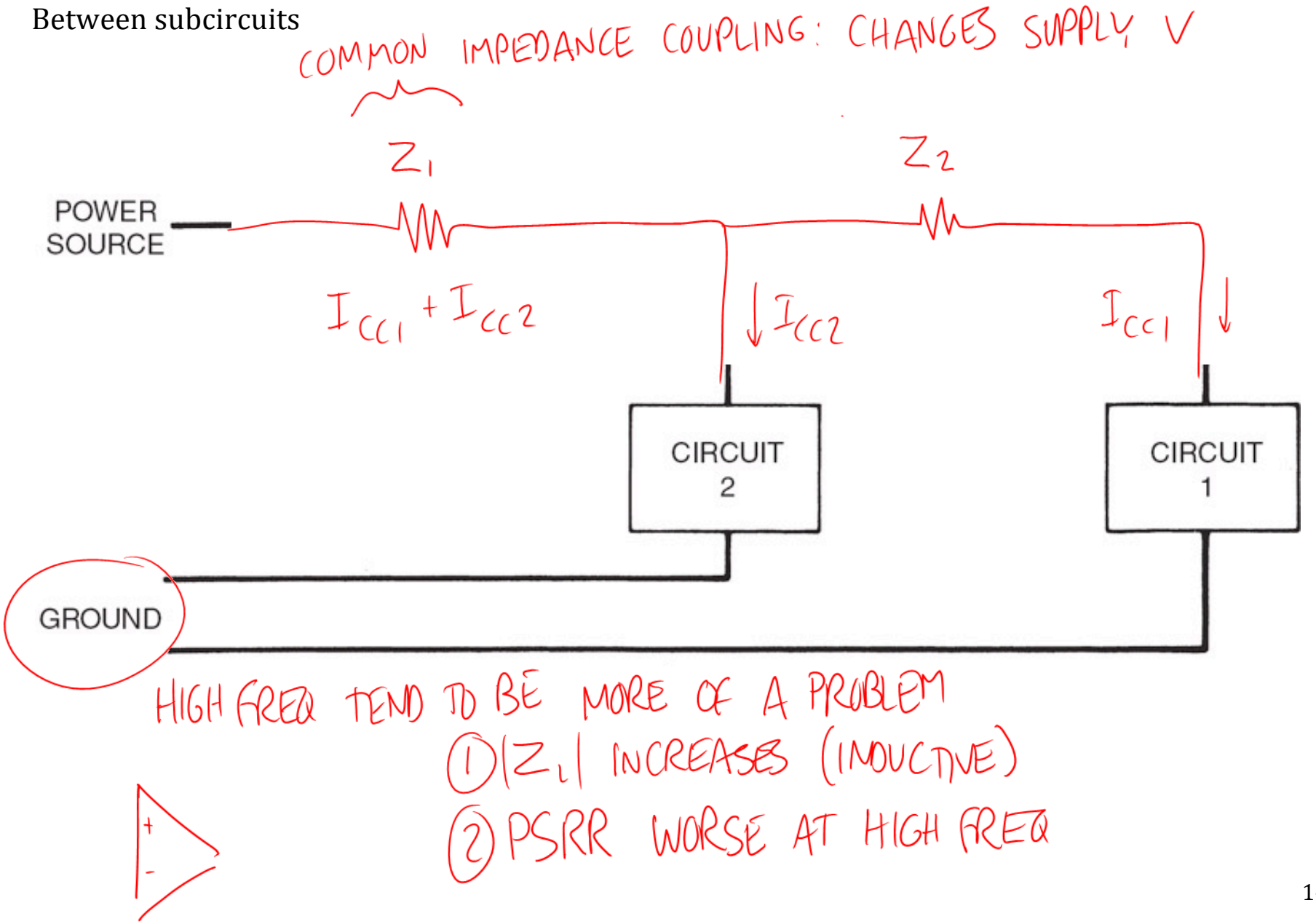


BAD AT HIGH FREQ

$$PSRR \quad \frac{A_{PS}}{A_{OL}} \rightarrow 0$$

Coupling through power supply distribution networks

Between subcircuits



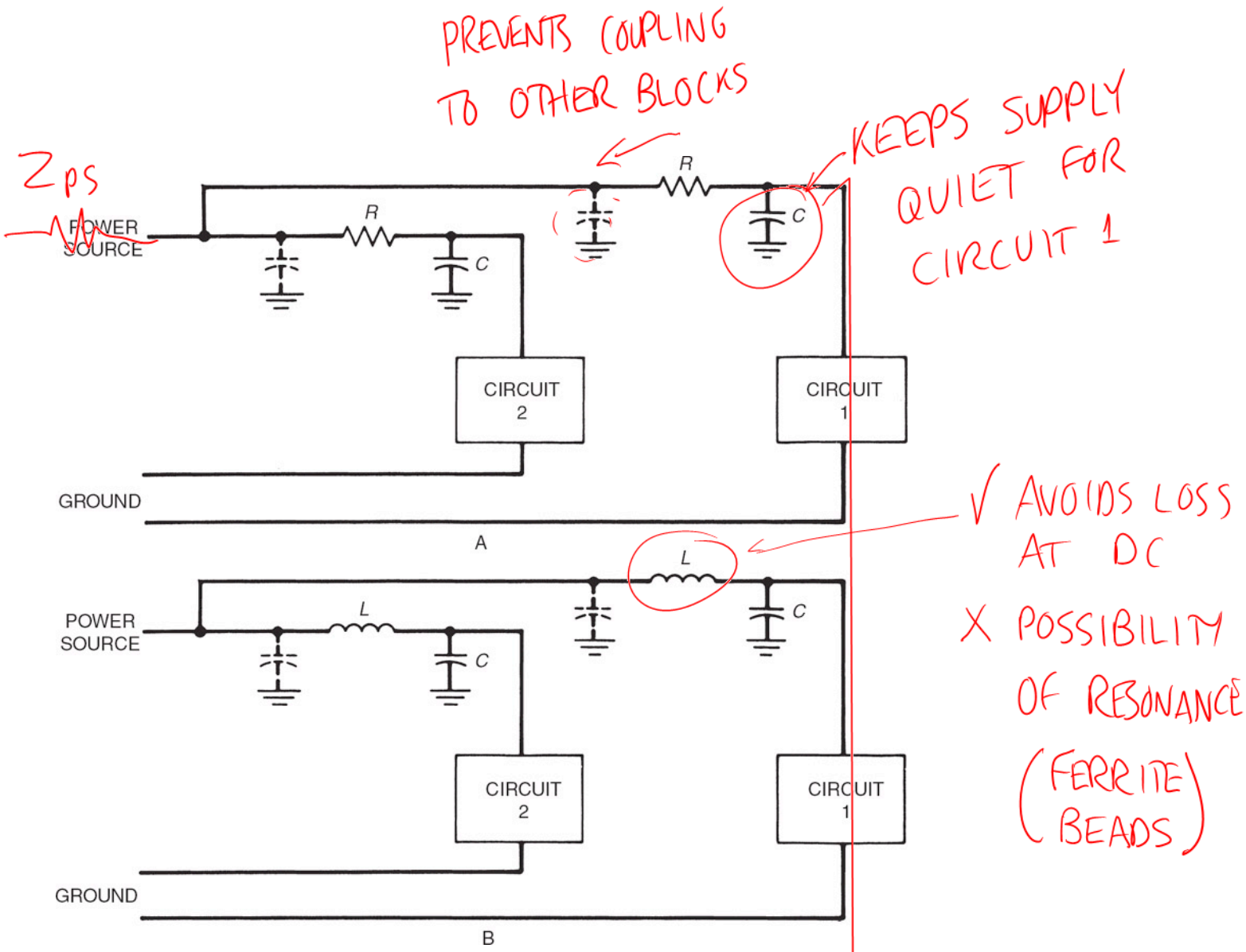


Figure 4-18: Circuit decoupling with *(A)* resistance-capacitance and *(B)* inductance-capacitance networks

Coupling through power supply distribution networks: Within subcircuits

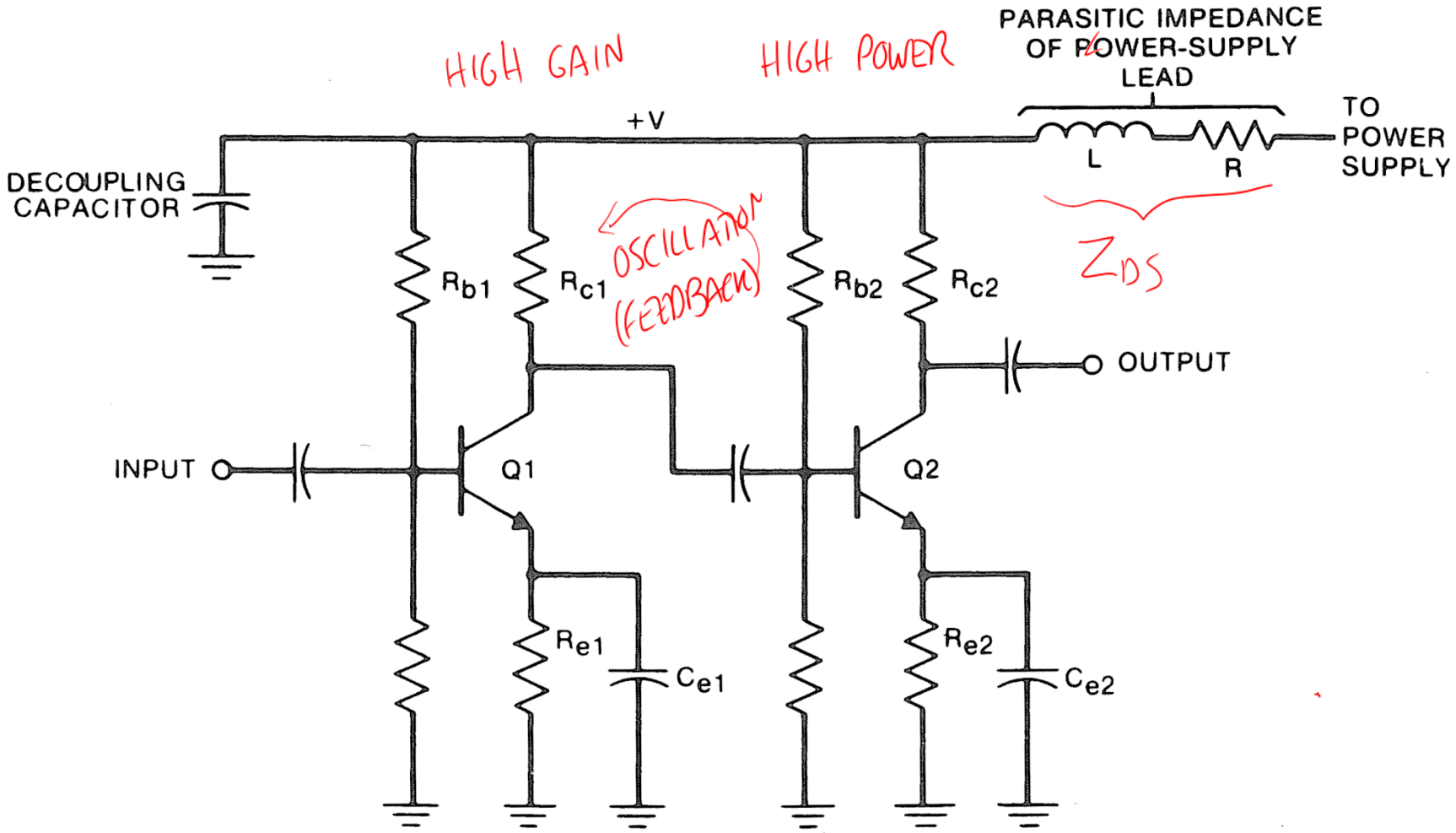


Figure 4-20: Power supply decoupling for a two-stage amplifier

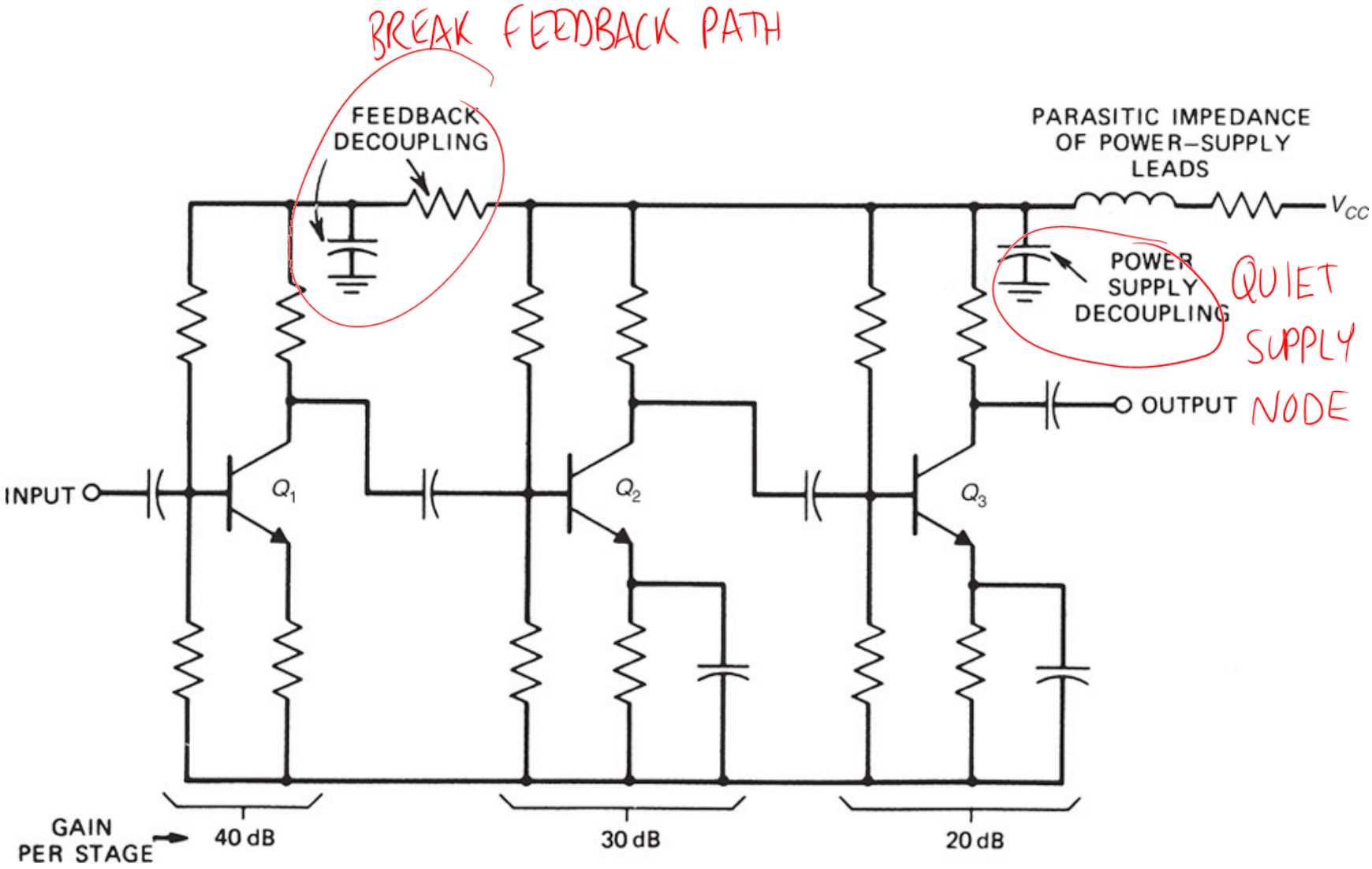


Figure 4-23: Power supply feedback decoupling between stages of an amplifier

Caution: Energy storage in inductance vs. loss in resistance

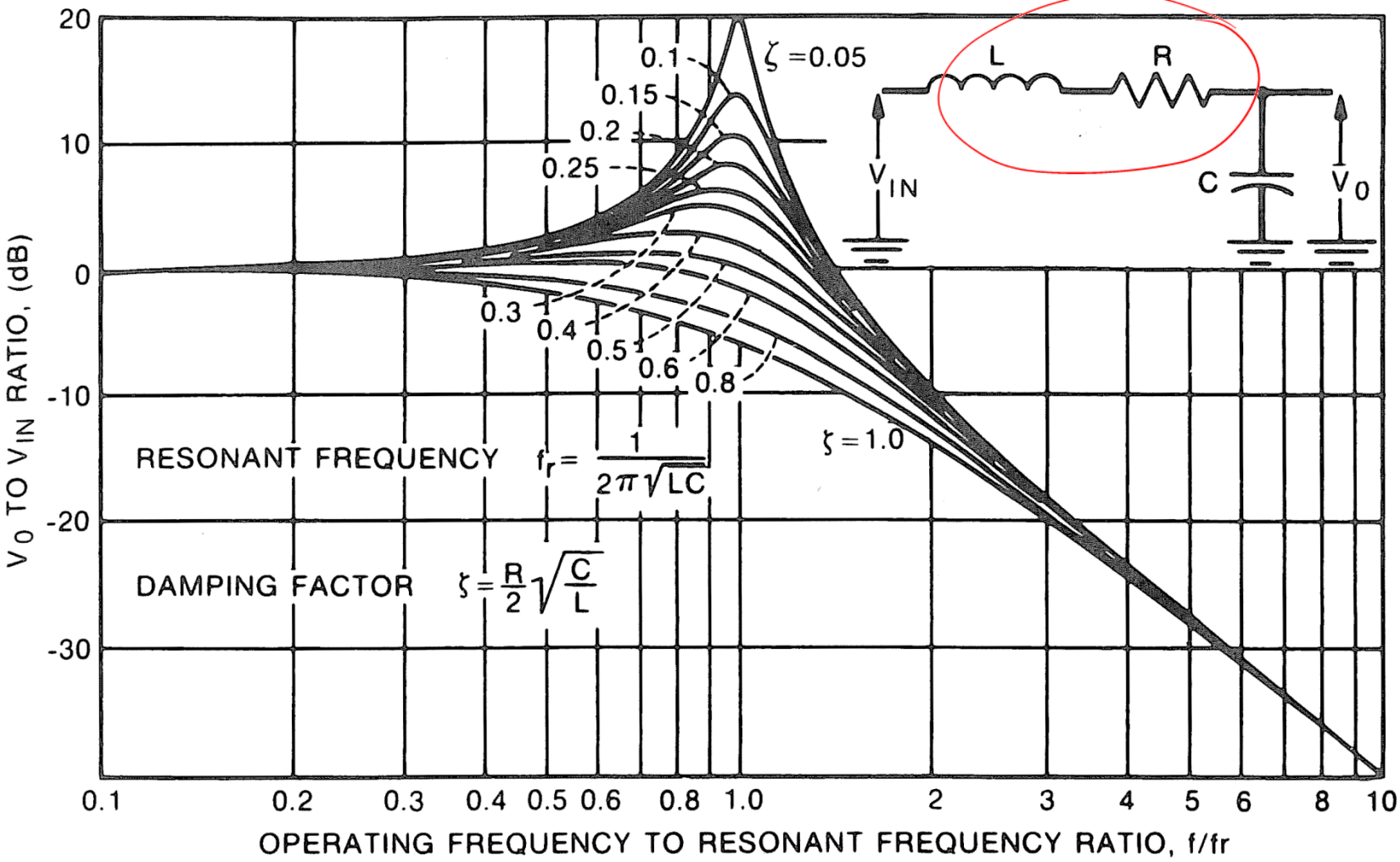


Figure 4-19: Effect of damping factor on filter response

FEEDTHROUGH CAPACITORS

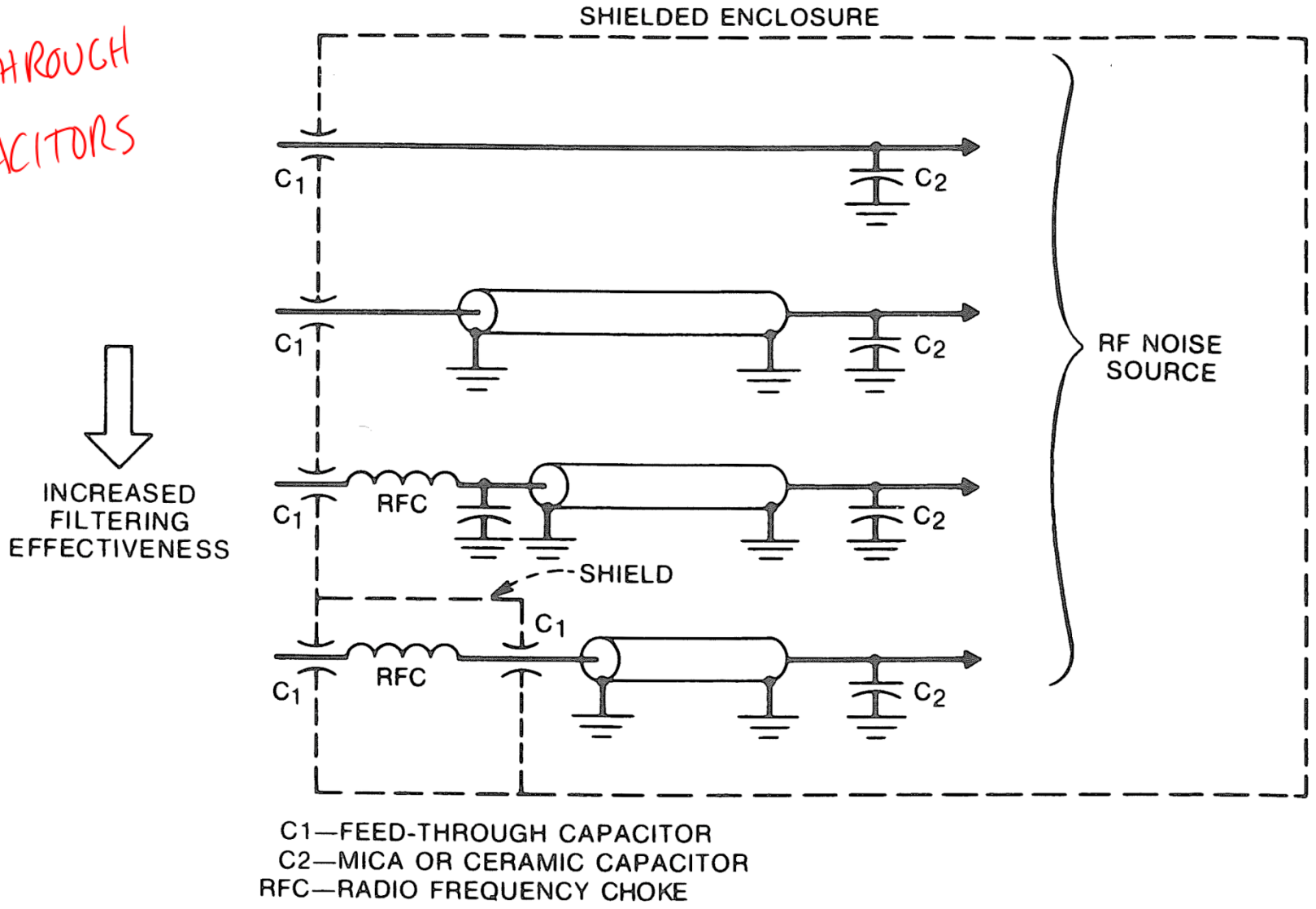


Figure 4-18. *Various high-frequency lead-filtering methods. Effectiveness increases from top toward bottom.*

Summary: Analog Power Supply Decoupling and Routing

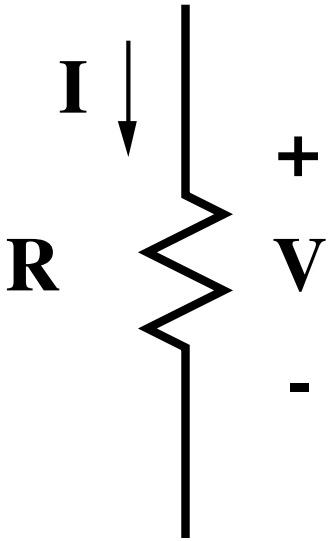
- The lower the characteristic impedance of a dc power distribution circuit, the less the noise coupling over it.
- Because many dc power distribution systems do not provide a low impedance, decoupling capacitors should be used at each load.
- From a noise point of view, a dissipative filter is preferred to a reactive filter.
- Some amplifier circuits will oscillate when driving a capacitive load, unless properly compensated and/or decoupled.
- To minimize noise, the bandwidth of a system should be no more than that necessary to transmit the desired signal.

Parallel Plate EM Fields

- Electric field demonstration relatively easy
  - –Rub a balloon on your sweater, stick it to a wall
  - –See lightning, spark after shuffling across carpet
  - –Opposite charges attract
  - –E field tells you which way charges move (force acting on charge)
- Magnetic field
  - –???
  - –Try a different way to look at things...

(Acknowledgment: Paul Brokaw, Analog Devices)

Cause and Effect: Ohm's Law



$$V = I\,R$$

- Which is cause, which is effect?
- V cause, I effect?
- I cause, V effect?

Chemistry vs. Electrical Engineering

$$2H_2 + O_2 \rightarrow 2H_2O$$

Cause Effect

$$V=IR$$

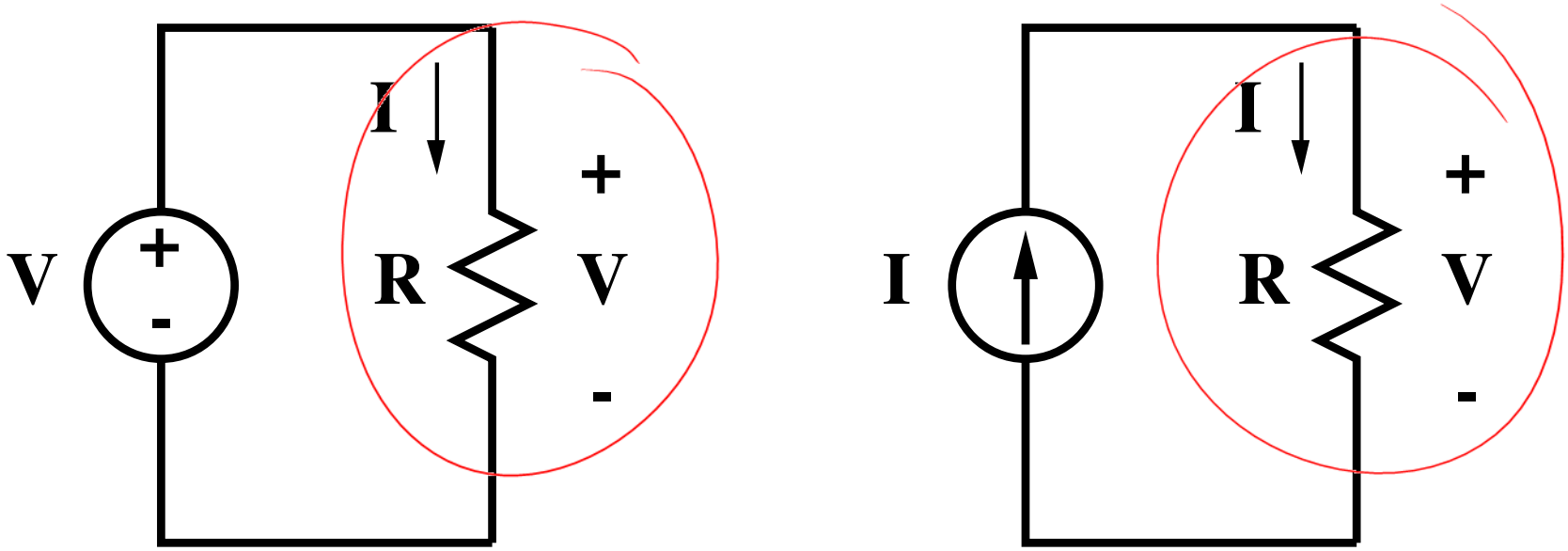
–No arrow!

–V, I just "go together"

–View either as cause, effect

–Whatever is best for your purpose

You're the cause



V, I go together - Resistor doesn't care

What causes magnetic field?

- Usual answer: current
  - –Usually introduced in terms of current in a wire creating an associated magnetic field
  - –Physics (force-based) approach
- Think about it another way ...
  - –Better way for circuit designers
  - –What effect is field describing?
- Look at capacitance, inductance

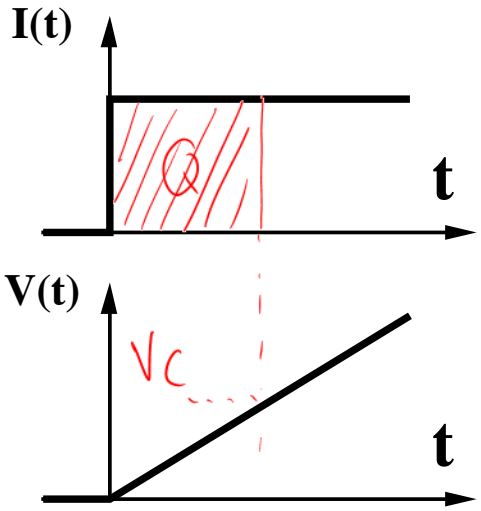
Capacitance

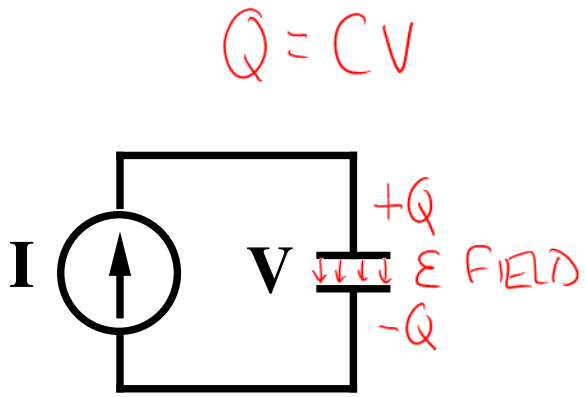
- Represents energy stored in electric field
- Capacitor voltage can't change instantaneously
- Time delay required to "build up" energy in field
- C tells you how much V results from applied A-sec

$$I_C = C\frac{dV_C}{dt}$$

$$\Rightarrow \quad V_C = \frac{1}{C}\int \underbrace{I_C dt}_{A\cdot\sec}$$

Q



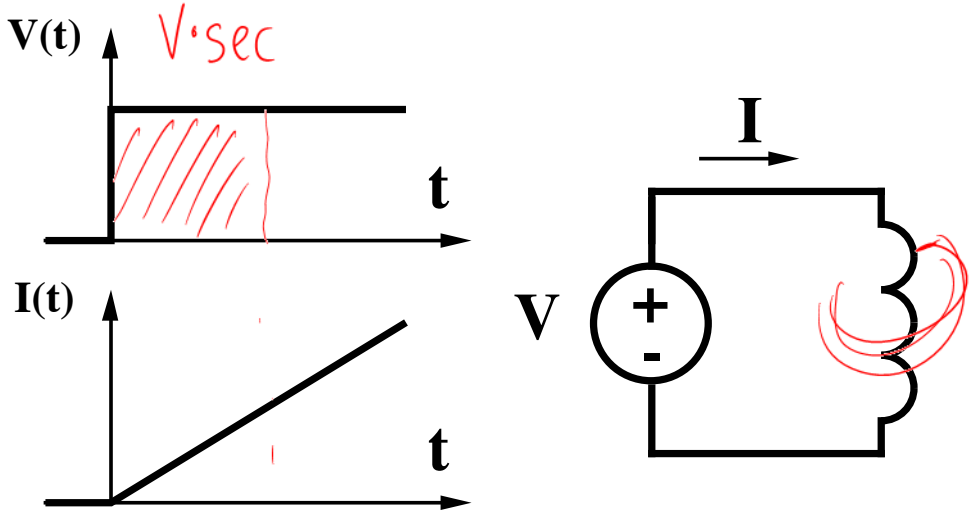


Inductance

- Represents energy stored in magnetic field
- Inductor current can't change instantaneously
- Time delay required to "build up" energy in field
- L tells you how much I results from applied V-sec

$$V_L = L\frac{dI_L}{dt}$$

$$\Rightarrow \quad I_L = \frac{1}{L}\underbrace{\int V_L dt}_{V\cdot\text{sec}}$$



Different Approach to Magnetic Field

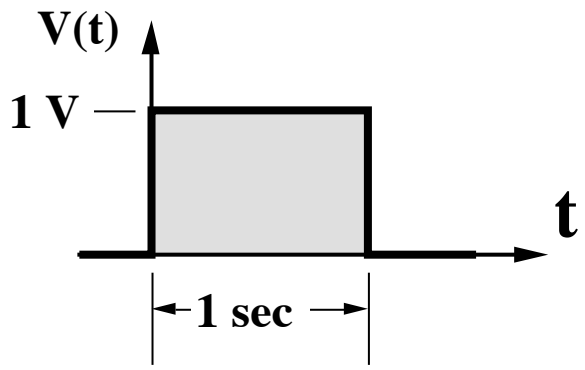
- Electric Field
  - –Represented by capacitance
  - –Voltage is result; cause is applied A-sec (charge)

- Magnetic Field
  - –Represented by inductance
  - **–Current is result; cause is applied V-sec**

Units of magnetic flux density

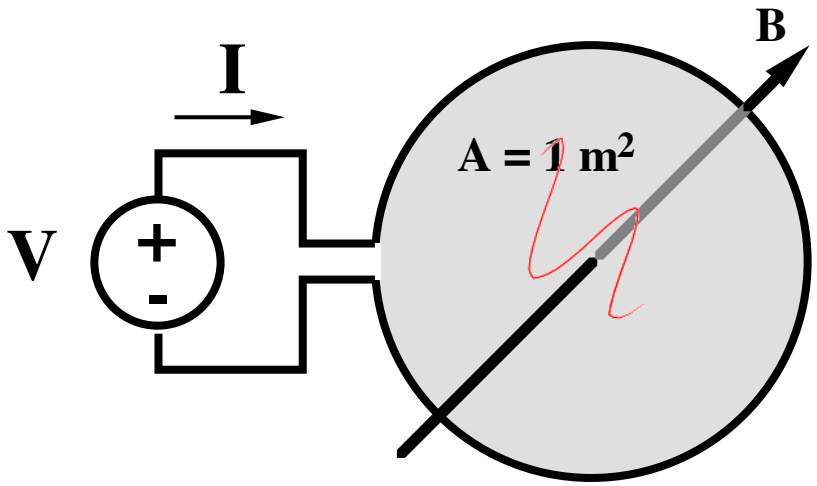
- Magnetic flux density B

$$[tesla] = \left[\frac{V \cdot \sec}{m^2}\right]$$



Meaning

- Apply 1V for 1sec to loop with area of 1m^2 (cause)
- Result is B field of 1 tesla (effect)
- What about current???



What about current?

- Observed that resulting current for a given V-sec/m^2 depends on material in which field lines exist
- Described with permeability μ, magnetic field H:

$$\vec{H} = \left(\frac{1}{\mu}\right)\vec{B}$$

- H gives current through Ampere's law

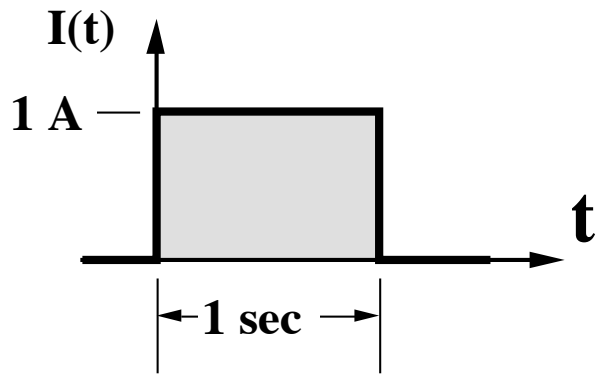
$$I_{encl} = \oint \vec{H} \cdot \vec{d\ell}$$

- Units: H must have units [A/m]
  $\Rightarrow$ Permeability μ will have units [Hy/m]
- Hint: μ will be involved in value of inductance!

Units of electric flux density

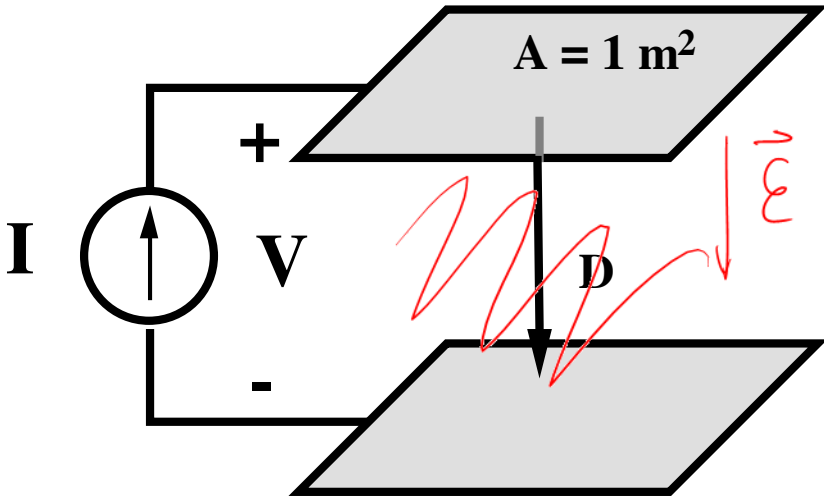
- Electric flux density D

$$\left[\frac{coul}{m^2}\right] = \left[\frac{A \cdot \sec}{m^2}\right]$$



Meaning

- Apply 1A for 1sec to capacitor plates with area of 1m^2 (cause)
- Result is D flux of 1 A-sec/m^2 (effect)
- What about voltage?



What about voltage?

- Observed that resulting voltage for a given A-sec/m^2 depends on material in which field lines exist
- Described with permittivity ε, electric field E:

$$\vec{E} = \left(\frac{1}{\varepsilon}\right)\vec{D}$$

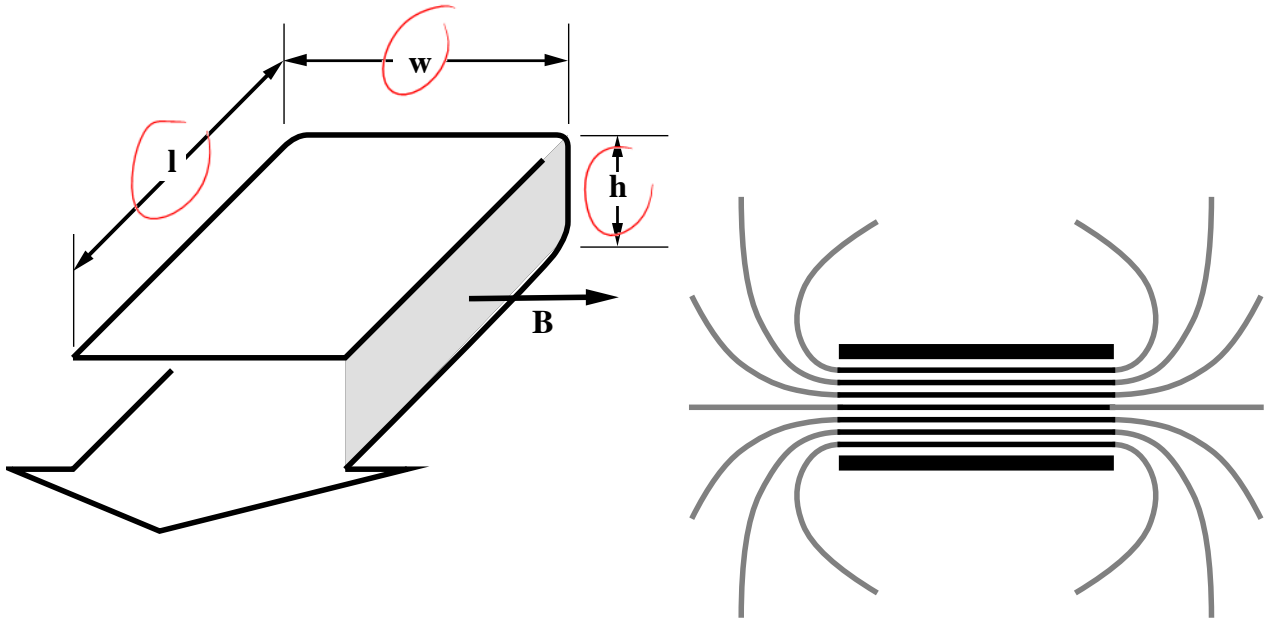
- E gives voltage through path integral

$$V_{ab} = \int_a^b \vec{E} \cdot \vec{d\ell}$$

- Units: E must have units [V/m]
  $\Rightarrow$ Permittivity ε will have units [F/m]
- Hint: ε will be involved in value of capacitance!

Parallel Plate Electromagnetics

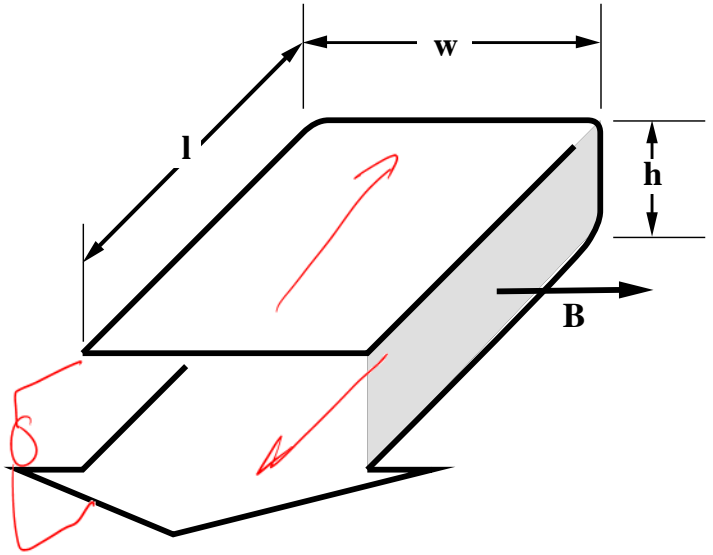
- Area = 1m^2 a little large for our purposes ...
- Use geometry suited to PCB design: parallel plates
- Determine inductance, capacitance
- Assumption: Field density negligible outside volume enclosed by plates

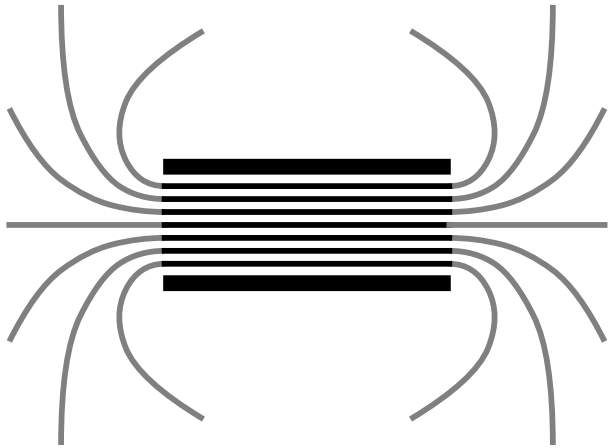


Magnetic Field / Inductance

Procedure:

- B from V-sec, area perpendicular to field lines
- H from μ, B
- Current I from H, path integral
- Inductance from definition of L





Magnetic Field / Inductance

B from V-sec, geometry

$$B = \frac{V_L \cdot t}{\ell \cdot h}$$

H from μ, B

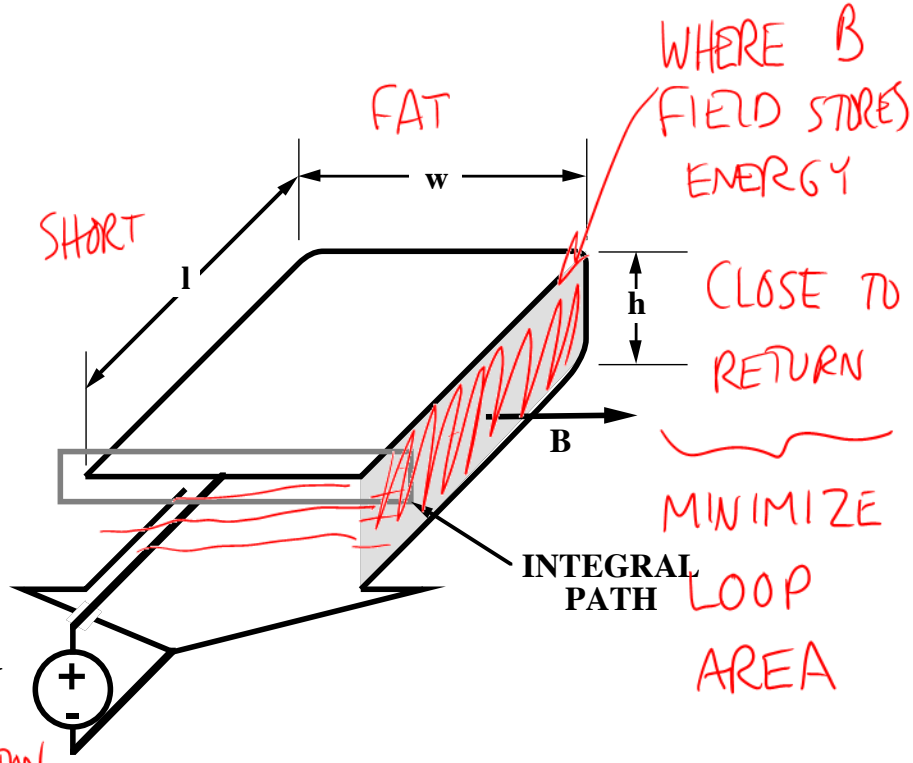
$$H = \left(\frac{1}{\mu}\right) B = \frac{V_L \cdot t}{\mu \cdot \ell \cdot h}$$

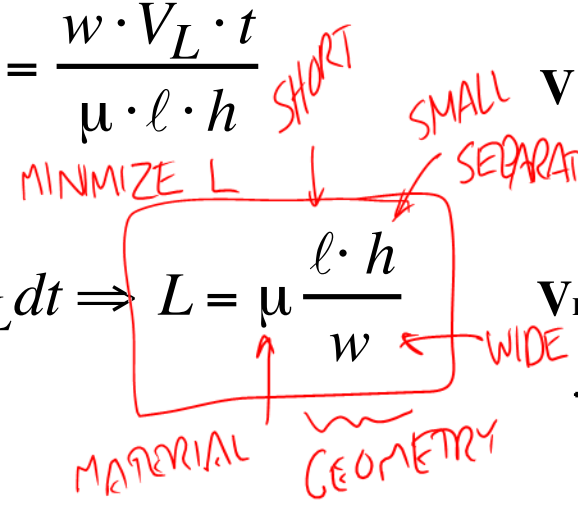
Path integral

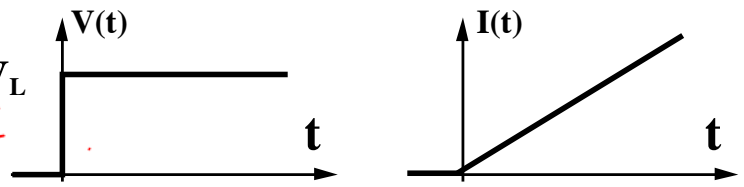
$$I = \oint \vec{H} \cdot \vec{d\ell} = \frac{w \cdot V_L \cdot t}{\mu \cdot \ell \cdot h}$$

Inductance

$$I = \left(\frac{1}{L}\right) \int V_L dt \Rightarrow L = \mu \frac{\ell \cdot h}{w}$$



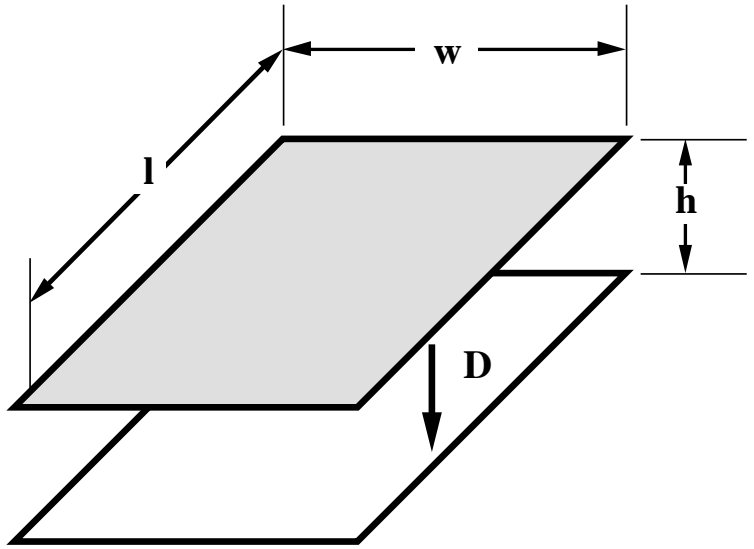


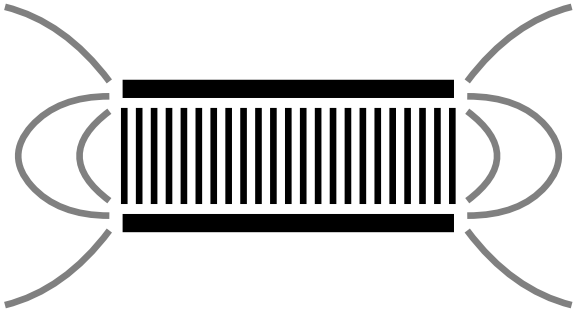


Electric Field / Capacitance

Procedure:

- D from A-sec, area perpendicular to field lines
- E from ε, D
- Voltage V from E, path integral
- Capacitance from definition of C





Electric Field / Capacitance

D from A-sec, geometry

$$D = \frac{I_C \cdot t}{\ell \cdot w}$$

E from ε, D

$$H = \left(\frac{1}{\varepsilon}\right) D = \frac{I_C \cdot t}{\varepsilon \cdot \ell \cdot w}$$

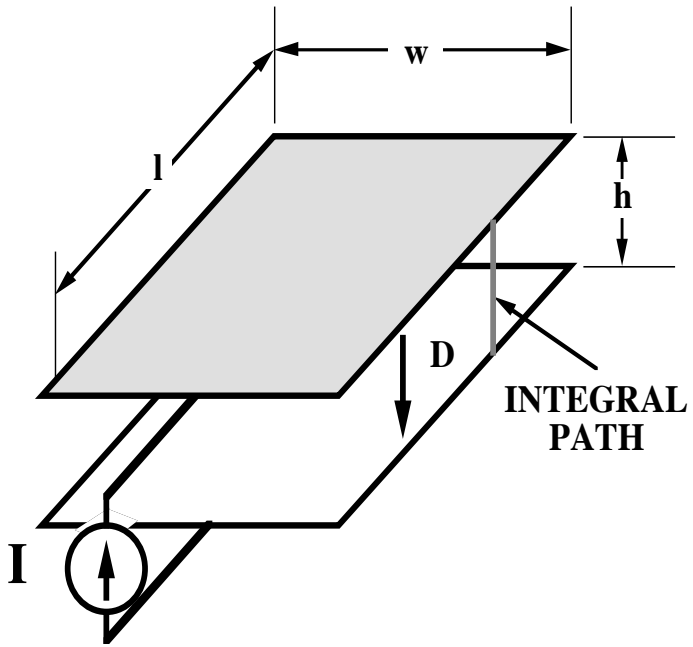
Path integral

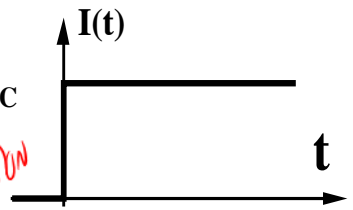
$$V = \int \vec{E} \cdot \vec{d\ell} = \frac{h \cdot I_C \cdot t}{\varepsilon \cdot \ell \cdot w}$$

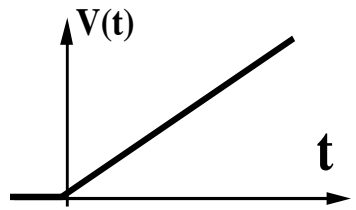
Capacitance

$$V = \left(\frac{1}{C}\right) \int I_C dt \Rightarrow C = \varepsilon \frac{\ell \cdot w}{h}$$

$\frac{A}{\text{SEPARATION}}$







MINIMIZE CAP (REDUCE COUPLING)

$\ell, w \downarrow$ SMALL $\quad h \uparrow$ FAR AWAY

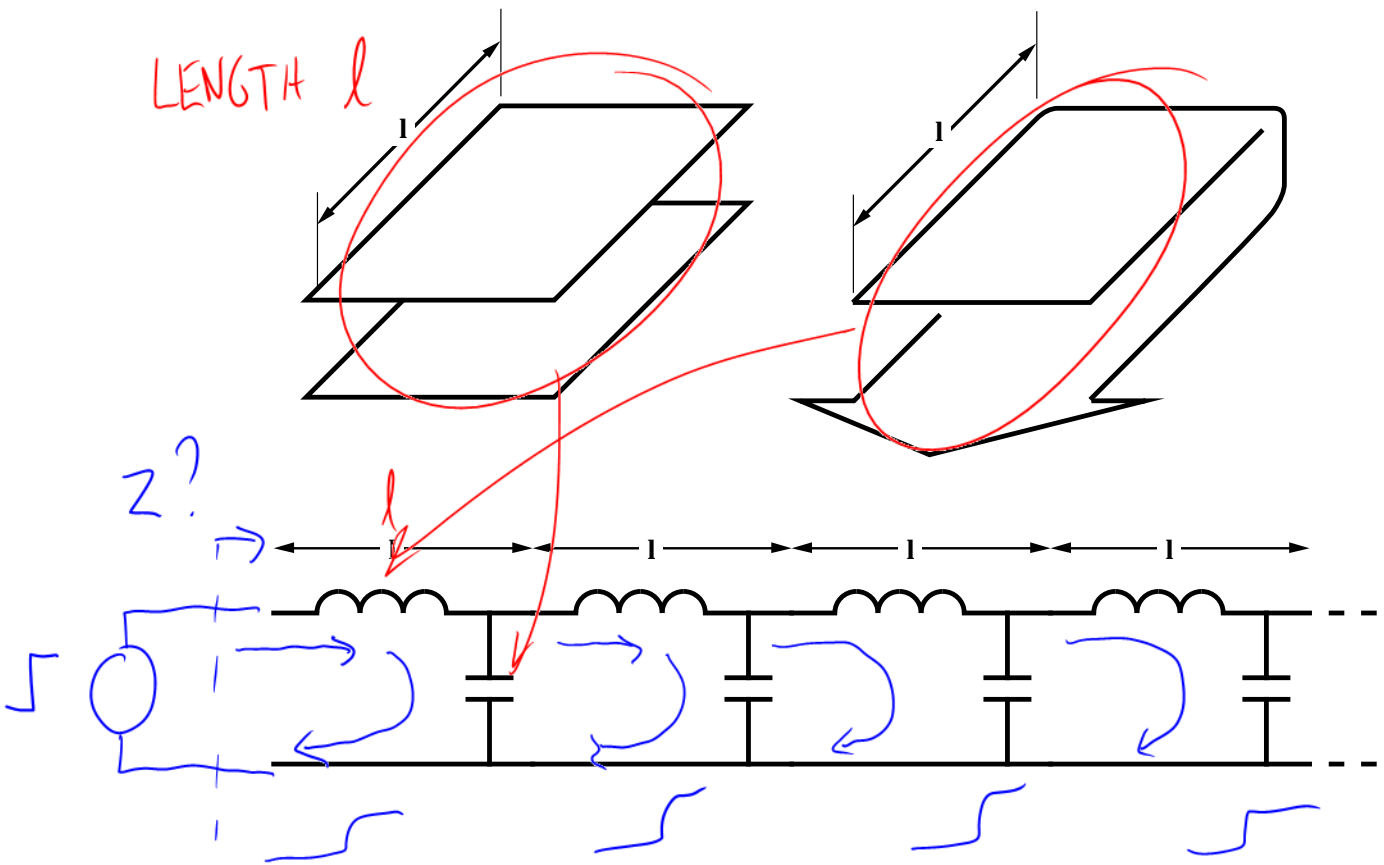
MAXIMIZE CAP (LOWER Z_{SD})

$\ell, w \uparrow$ BIG $\quad h \downarrow$ CLOSE

Parallel Plate Summary

- PCB trace: Energy in both electric, magnetic fields

$$C = \varepsilon \frac{\ell \cdot w}{h} \qquad L = \mu \frac{\ell \cdot h}{w}$$

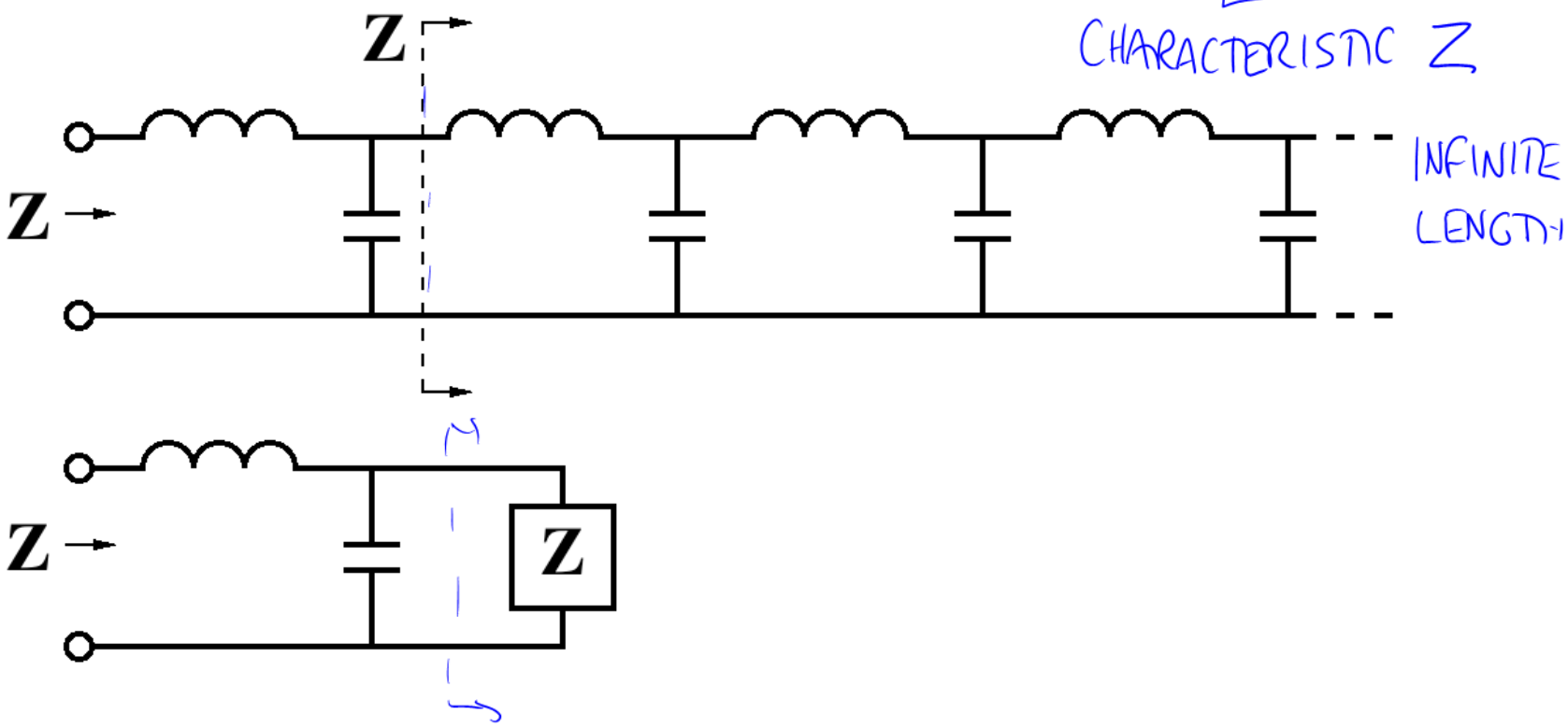


Transmission Line Impedance

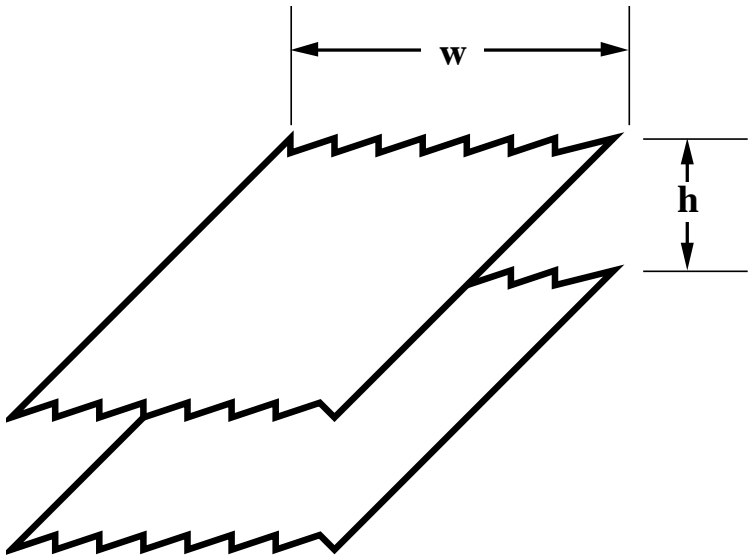
- Lumped L, C model (limit as segment length→0)

$$Z = j\omega L + \left(\frac{1}{j\omega C}\right) \Big\| Z \Rightarrow Z = \sqrt{\frac{L}{C}} = \sqrt{\left(\mu\frac{\ell h}{w}\right)\left(\frac{1}{\varepsilon}\frac{h}{\ell w}\right)} = \frac{h}{w}\sqrt{\frac{\mu}{\varepsilon}}$$

CHARACTERISTIC Z



Qualitative interpretation



$$Z = \underbrace{\frac{h}{w}}_{\text{GEOMETRY}} \underbrace{\sqrt{\frac{\mu}{\varepsilon}}}_{\text{MATERIAL}}$$

Low impedance

- Wide, close to return path (supply distribution)
- High current (energy in magnetic field)

High impedance

- Narrow, far from return (low power signal)
- Low current (energy in electric field)

Summary: Parallel Plate Electromagnetics

- Electric Field
  Represented by capacitance
  Voltage is result; cause is applied A-sec (charge)

- Magnetic Field
  Represented by inductance
  Current is result; cause is applied V-sec

- To minimize energy stored (and potentially coupled into and/or radiated from) magnetic field:
  Always think of current return path; provide easy (low energy, low inductance) return
  Minimize area of loop for current return
  Maximize width of current path for low impedance

Ideal vs. Real Components:

Capacitor
Inductor
Transformer
Resistor
Conductor
Transmission Lines
Ferrite Beads

Capacitors

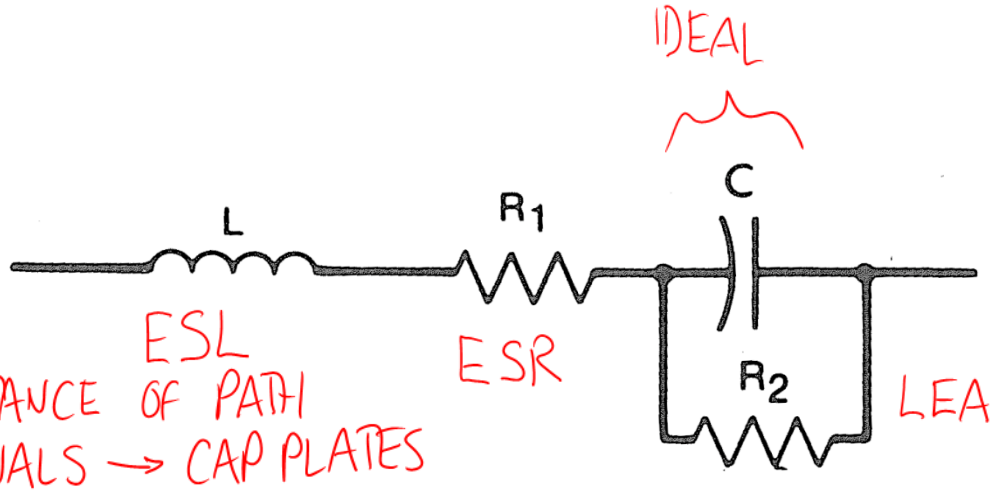


Figure 5-1. *Equivalent circuit for a capacitor.*

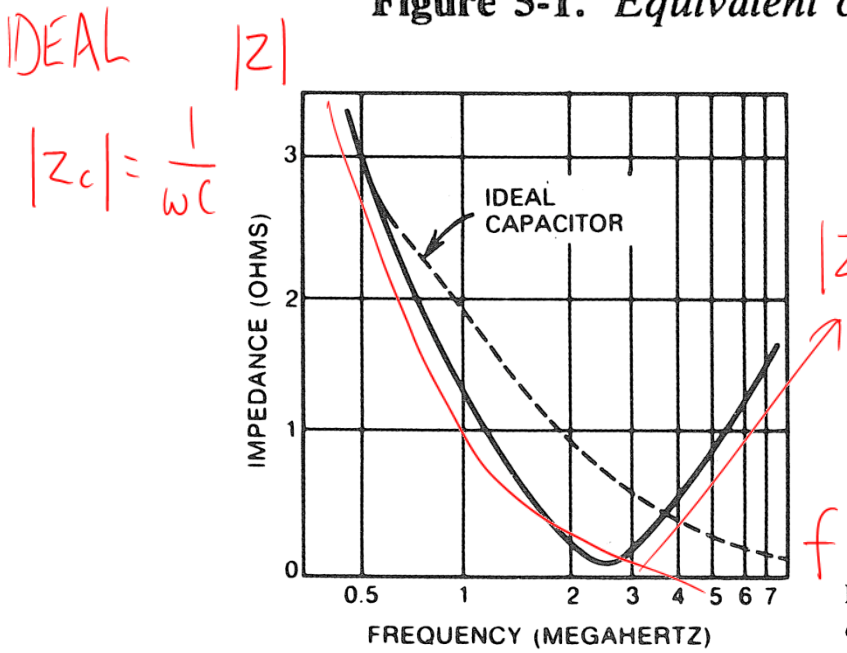


Figure 5-2. *Effect of frequency on the impedance of a 0.1 μF paper capacitor.*

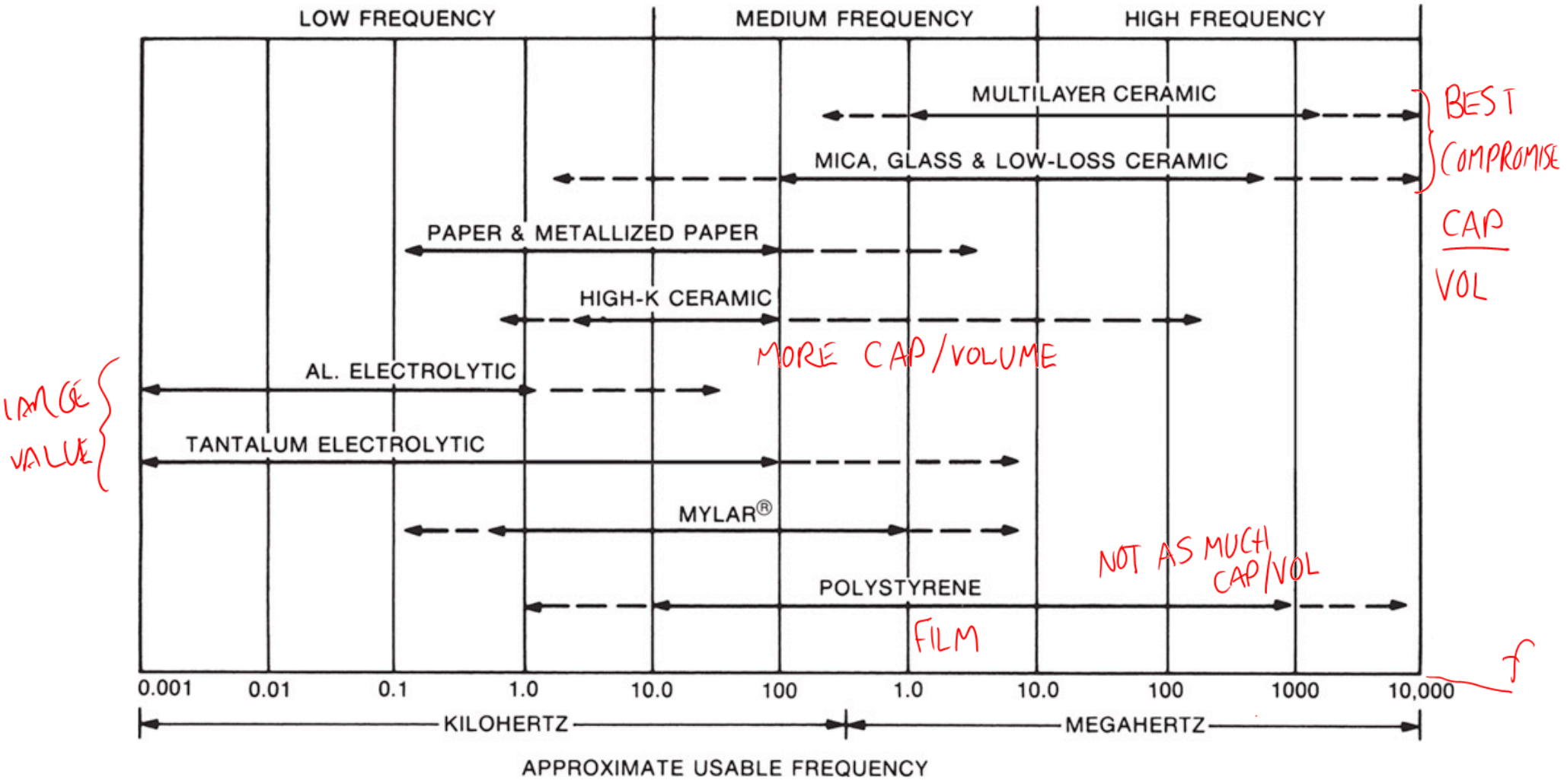


Figure 5-3: Approximate usable frequency ranges for various types of capacitors

Multilayer Ceramic Capacitor (MLCC)

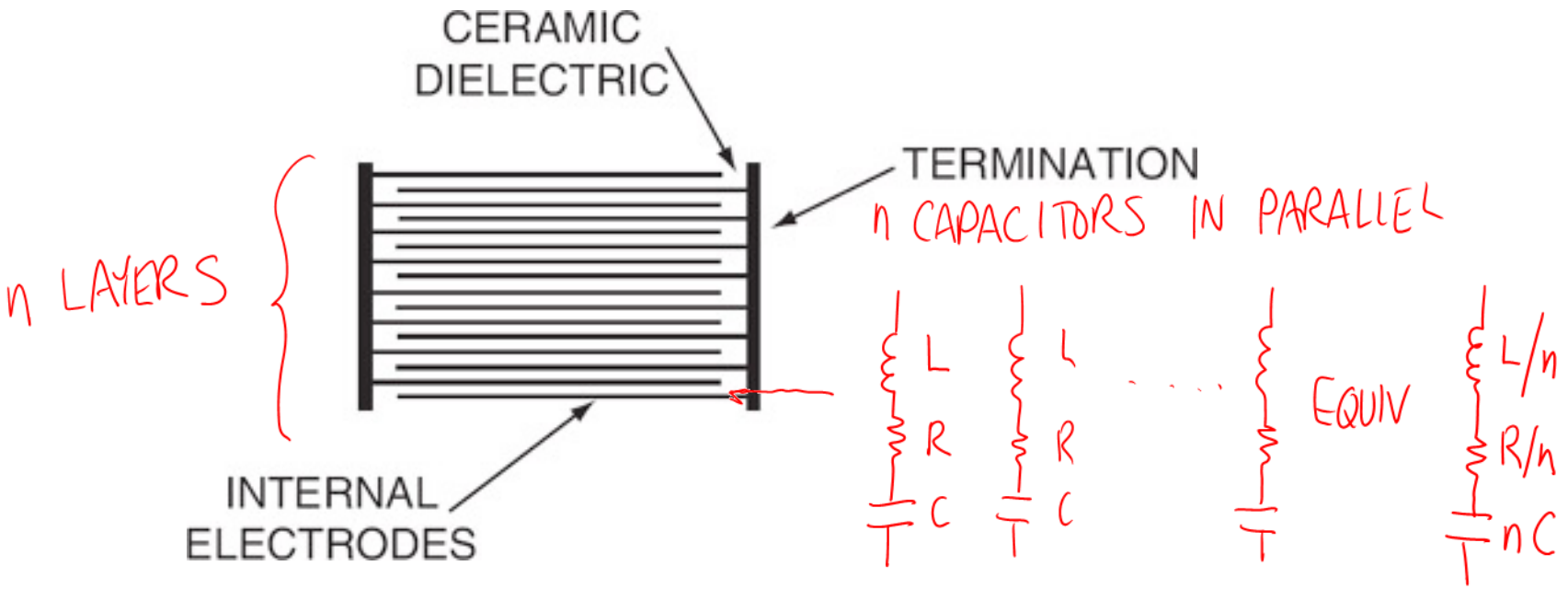


Figure 5-5: Multilayer ceramic capacitor construction

Advantage: Increase C, decrease L

Values up to 10µF – 100 µF, depending on rated voltage

LOWER V ⇒ THINNER DIELECTRIC
⇒ MORE C / VOLUME

Film Capacitor

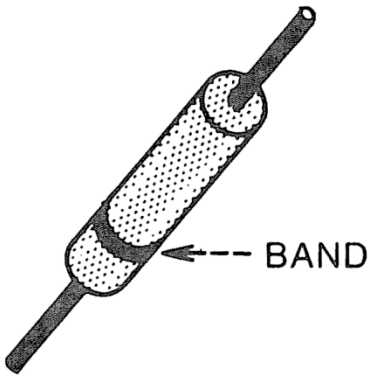
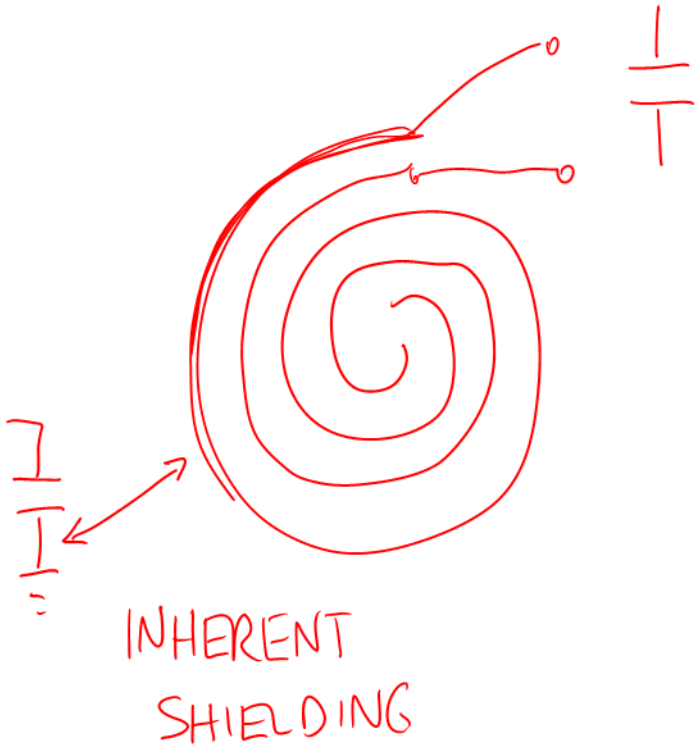


Figure 5-4. *Band on tubular capacitor indicates the end that is connected to the outside foil. This end should be connected to ground.*



Feedthrough Capacitor

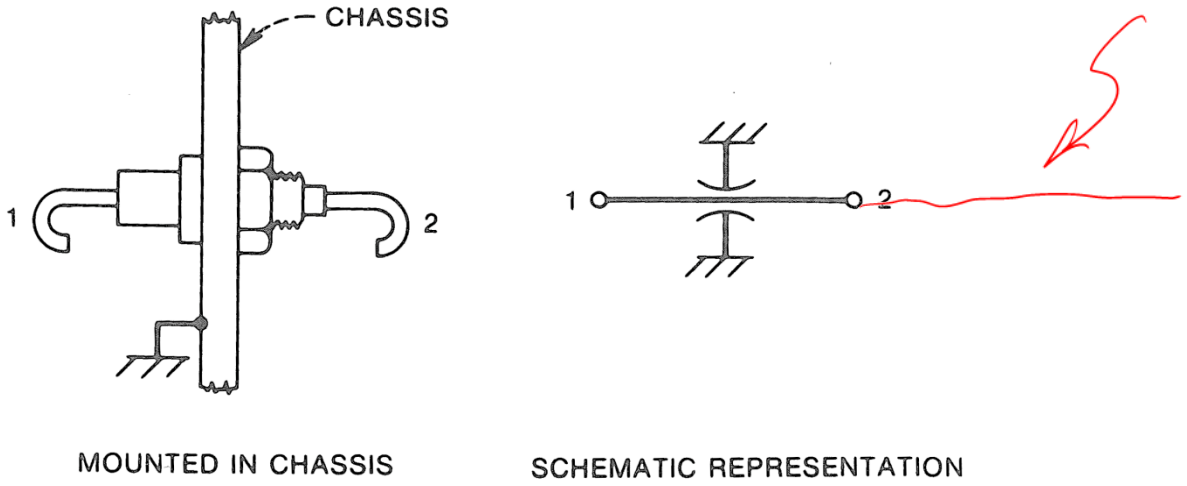


Figure 5-6: Typical feed-through capacitor

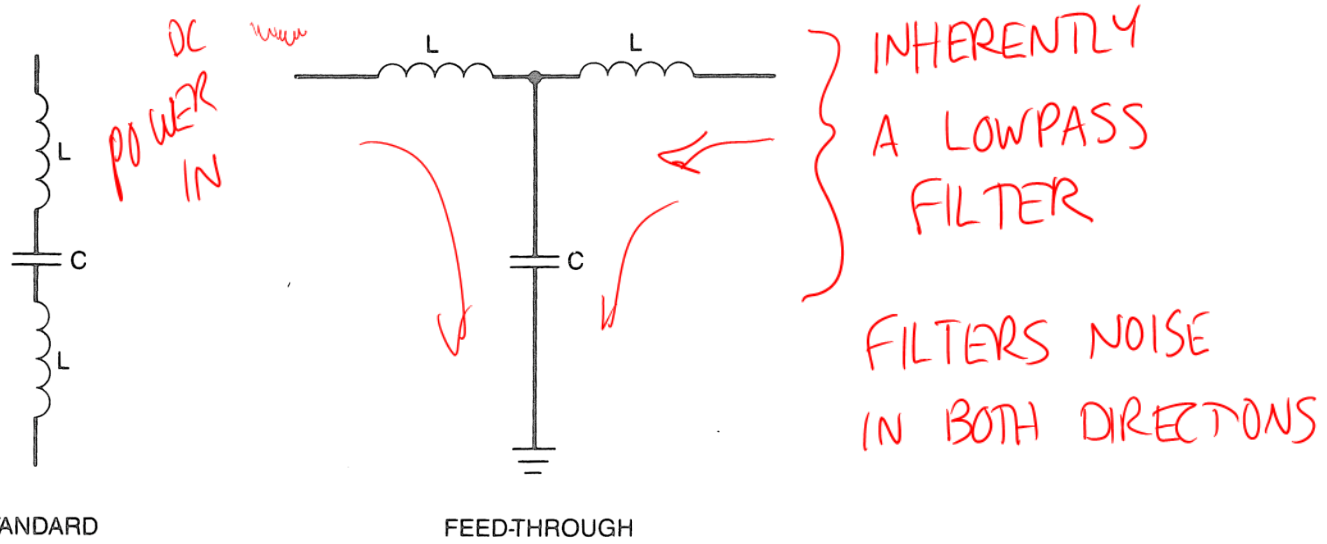


Figure 5-7: Lead inductance in standard and feed-through capacitors

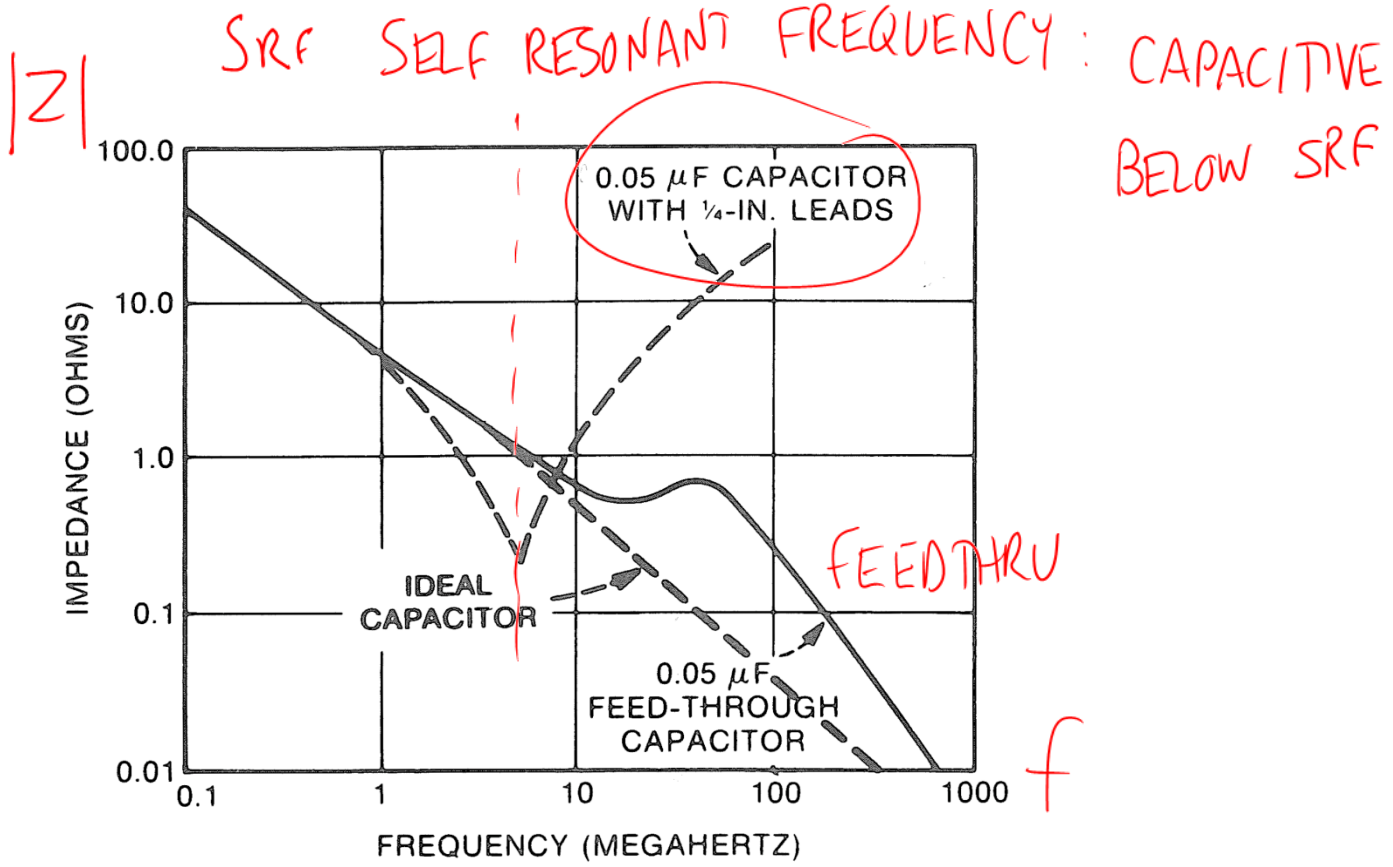


Figure 5-8: Impedance of 0.05-μF capacitors, showing improved performance of feed-through capacitor

Table 5-2: Self-Resonant Frequencies of Ceramic Capacitors MHz

	Self-Resonant Frequency	
Capacitance Value (pf)	**1/4-in Leads**	**1/2-in Leads**
10,000	12	"-"
1000	35	32
500	70	65
100	150	120
50	220	200
10	500	350

Inductors

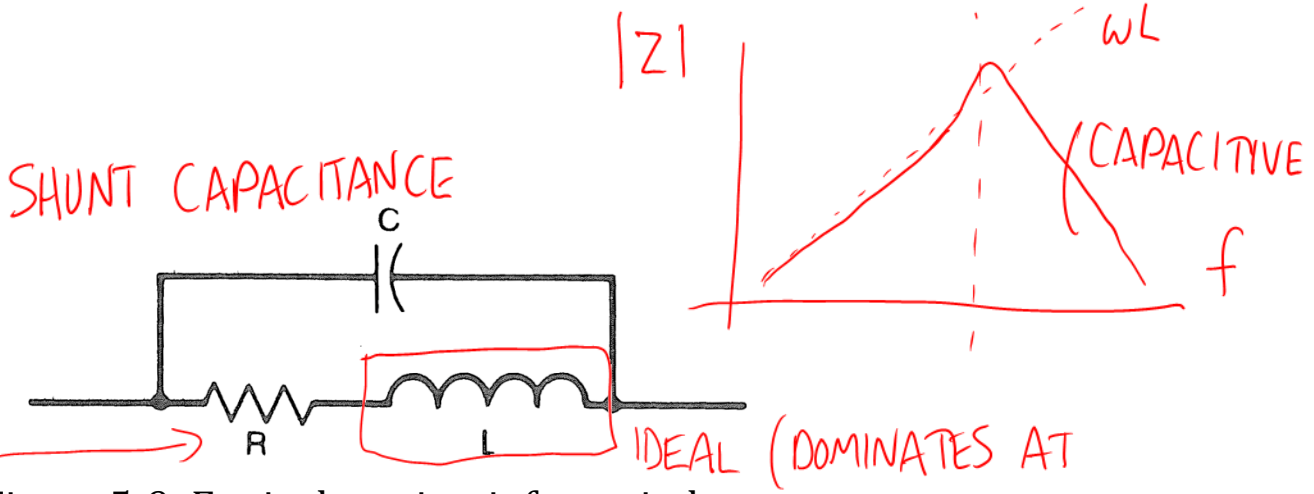


Figure 5-9: Equivalent circuit for an inductor

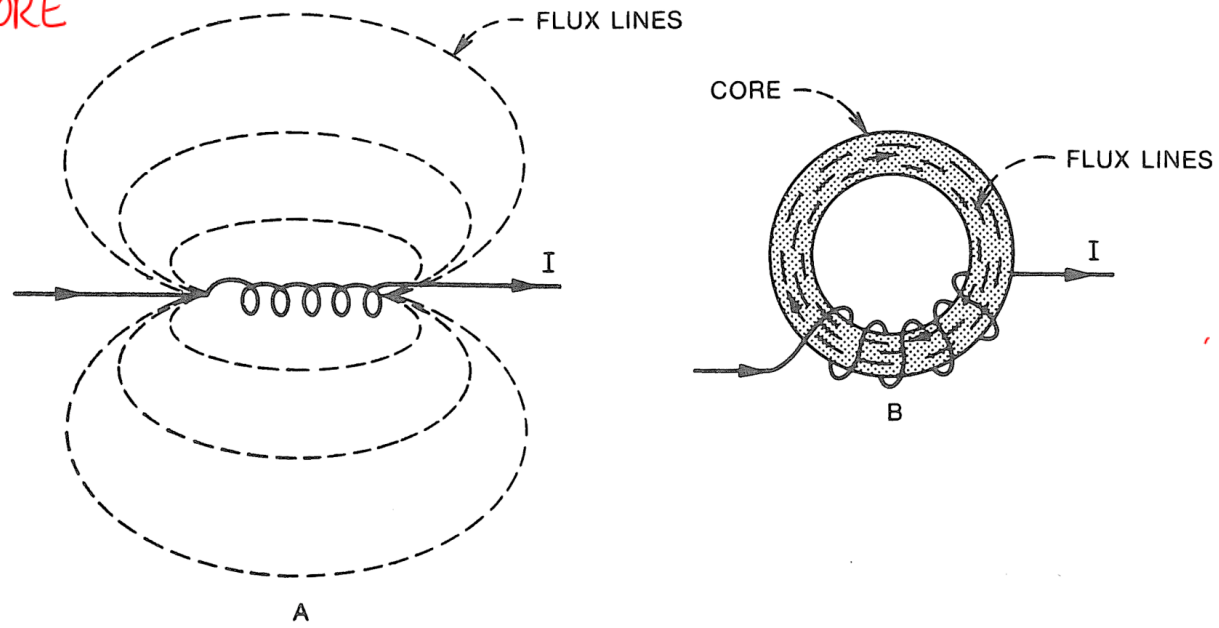


Figure 5-10: Magnetic fields from *(A)* air core and *(B)* closed magnetic core inductors

Transformers

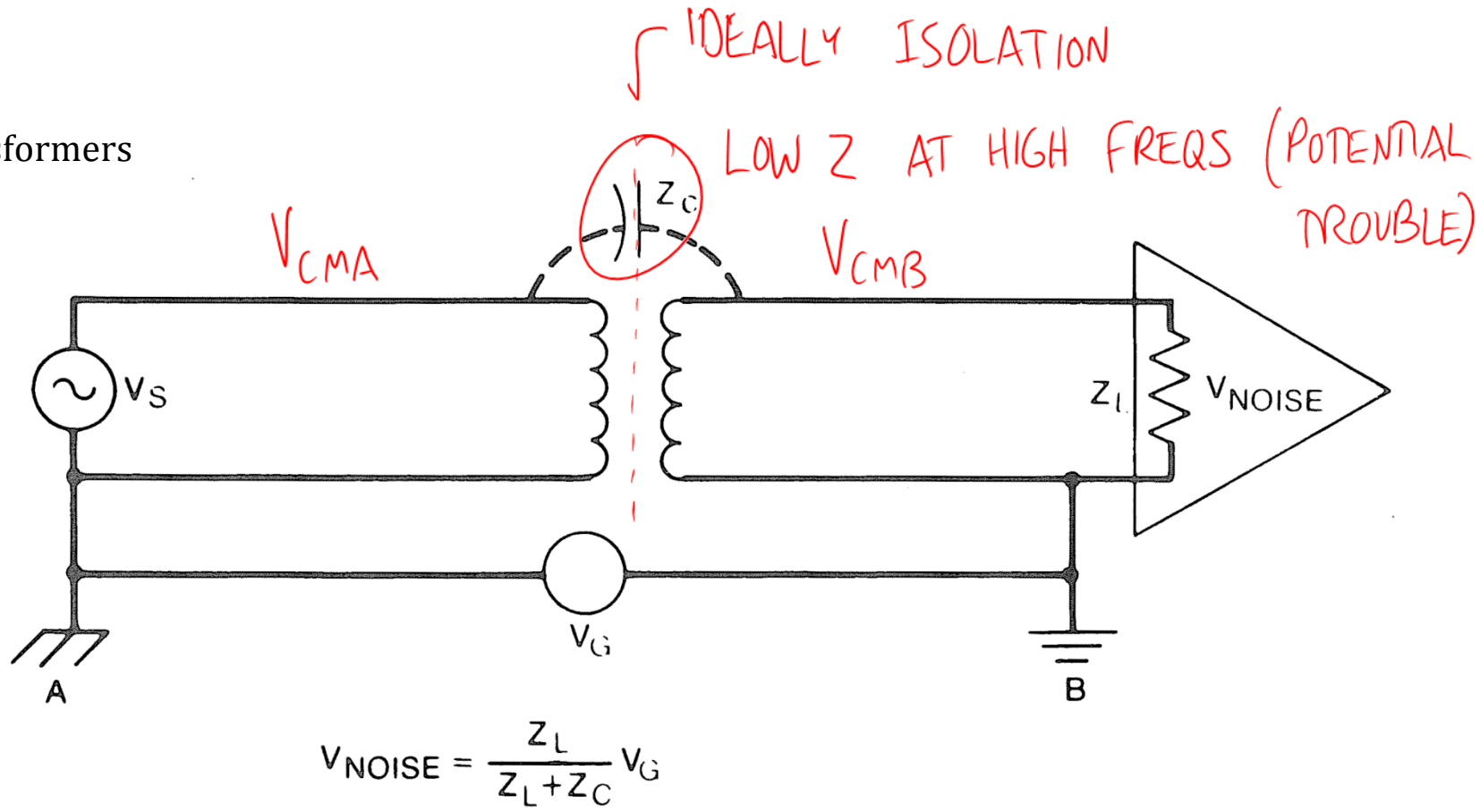


Figure 5-11: An actual transformer has capacitive as well as magnetic coupling between primary and secondary windings

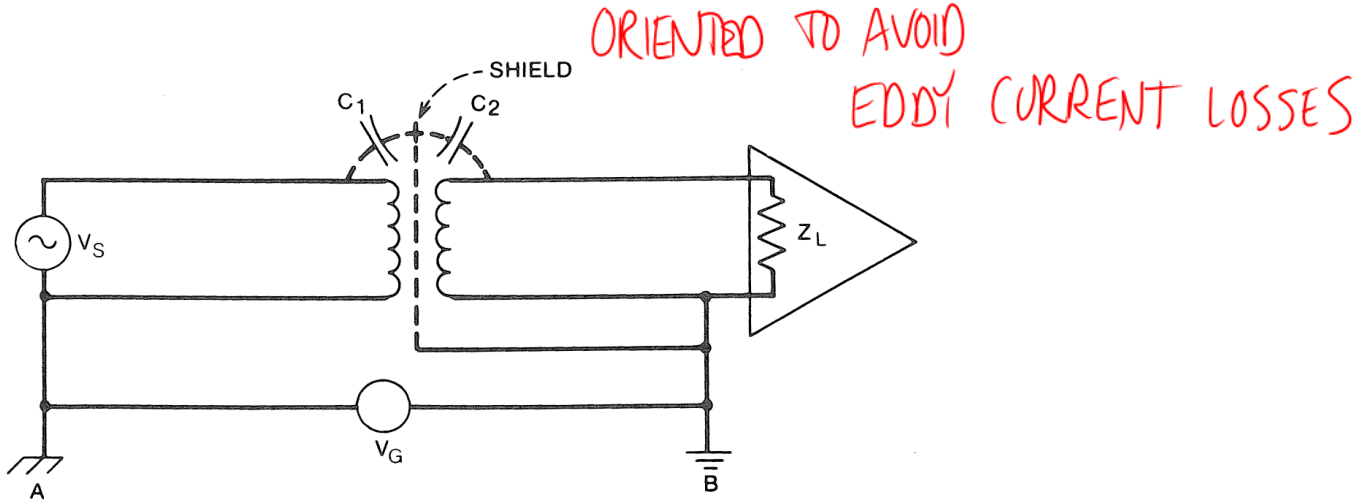


Figure 5-12: Grounded electrostatic shield between transformer windings breaks capacitive coupling

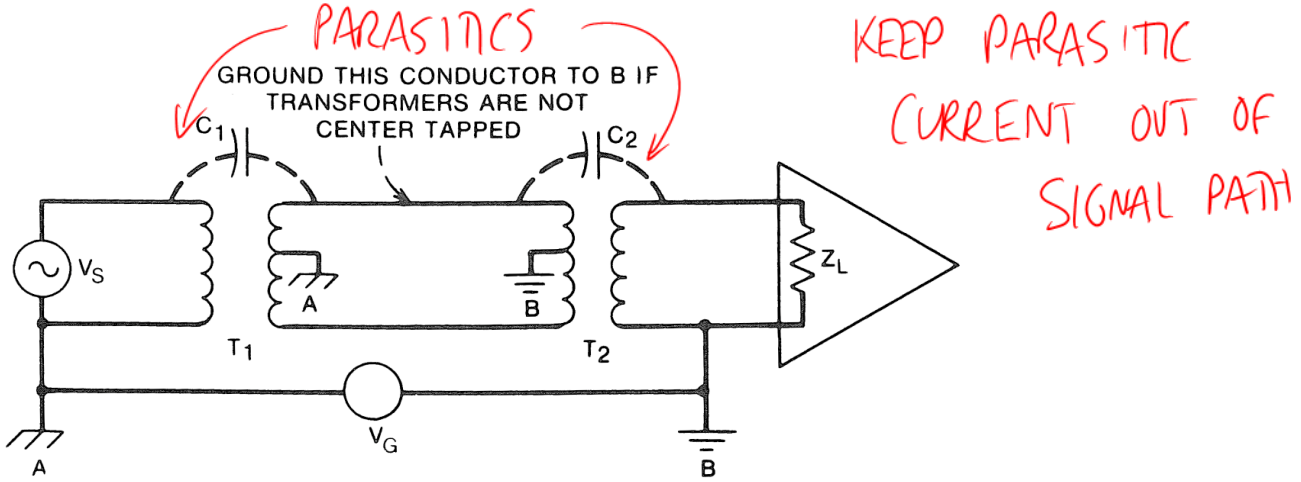


Figure 5-13: Two unshielded transformers can provide electrostatic shielding

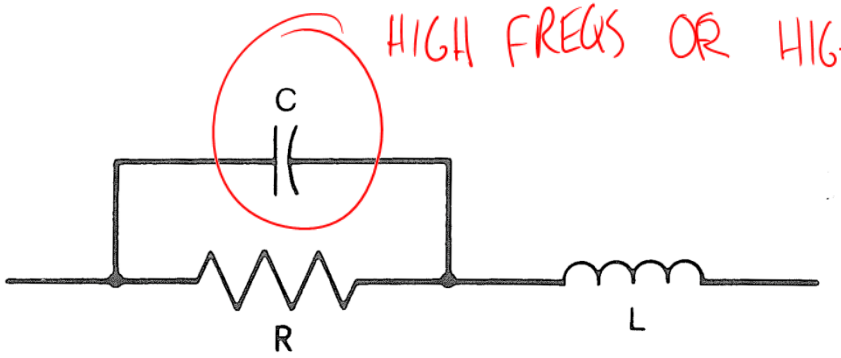


Figure 5-14: Equivalent circuit for a resistor

Table 5-3 Impedance of a 1-MΩ, ½-W Carbon Resistor Measured at Various Frequencies

	Impedance	
Frequency (kHz)	Magnitude (kΩ)	Phase Angle (degrees)
1	1000	0
9	1000	−3
10	990	−3
50	920	−11
100	860	−16
200	750	−23
300	670	−28
400	610	−32
500	560	−34

Another good reason to prefer SM metal film to carbon composition resistors:

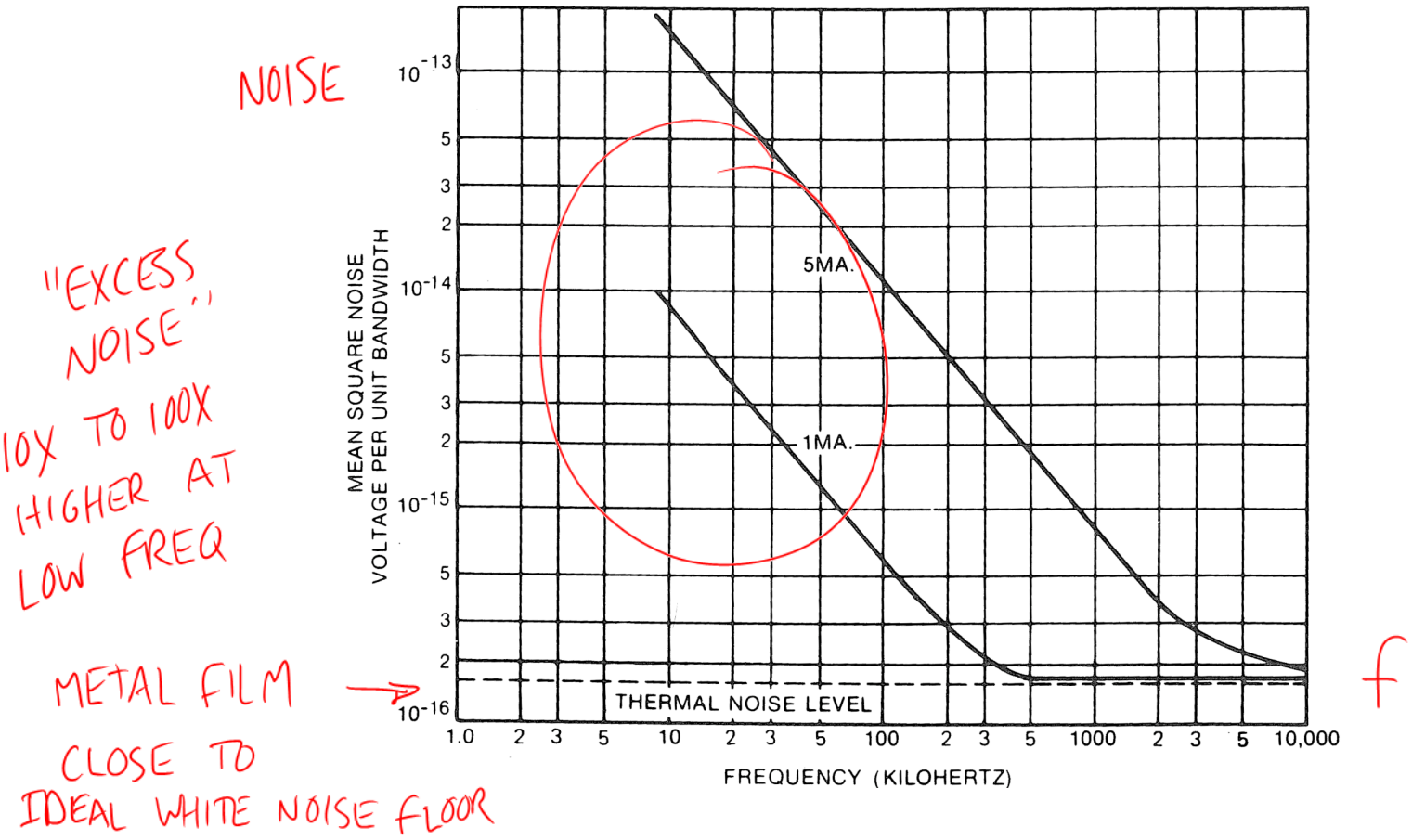


Figure 5-15: Effect of frequency and current on noise voltage for a 10-kΩ. carbon composition resistor

Conductors

LOWER Z? FATTER WIRE DOESN'T HELP MUCH FOR INDUCTANCE

Table 5-4 Inductance and Resistance of Round Conductors

Wire Size (AWG)	Diameter (in.)	Resistance (mΩ/in.)	Inductance (μH per in.) 0.25 in. Above Ground Plane	0.5 in. Above Ground Plane	1 in. Above Ground Plane
26	0.016	3.39	0.021	0.025	0.028
24	0.020	2.13	0.020	0.023	0.027
22	0.025	1.34	0.019	0.022	0.026
20	0.032	0.85	0.017	0.021	0.024
18	0.040	0.53	0.016	0.020	0.023
14	0.064	0.21	0.014	0.017	0.021
10	0.102	0.08	0.012	0.015	0.019

R 40X

L 2X

One Minute Quiz

For a 22 AWG wire 0.25" above ground plane, at what frequency does the reactive impedance of the wire inductance $|Z_L|$ equal the DC resistance?

$|Z_L| = R$ BOUNDARY BETWEEN LOW f, HIGH f

DC RES 1.34 mΩ

L = 19 nH $|Z_L| = \omega L = 2\pi f (19nH) \Rightarrow f = \frac{1.34m\Omega}{2\pi(19E\text{-}9H)} = 11\ kHz$ "HIGH FREQ"

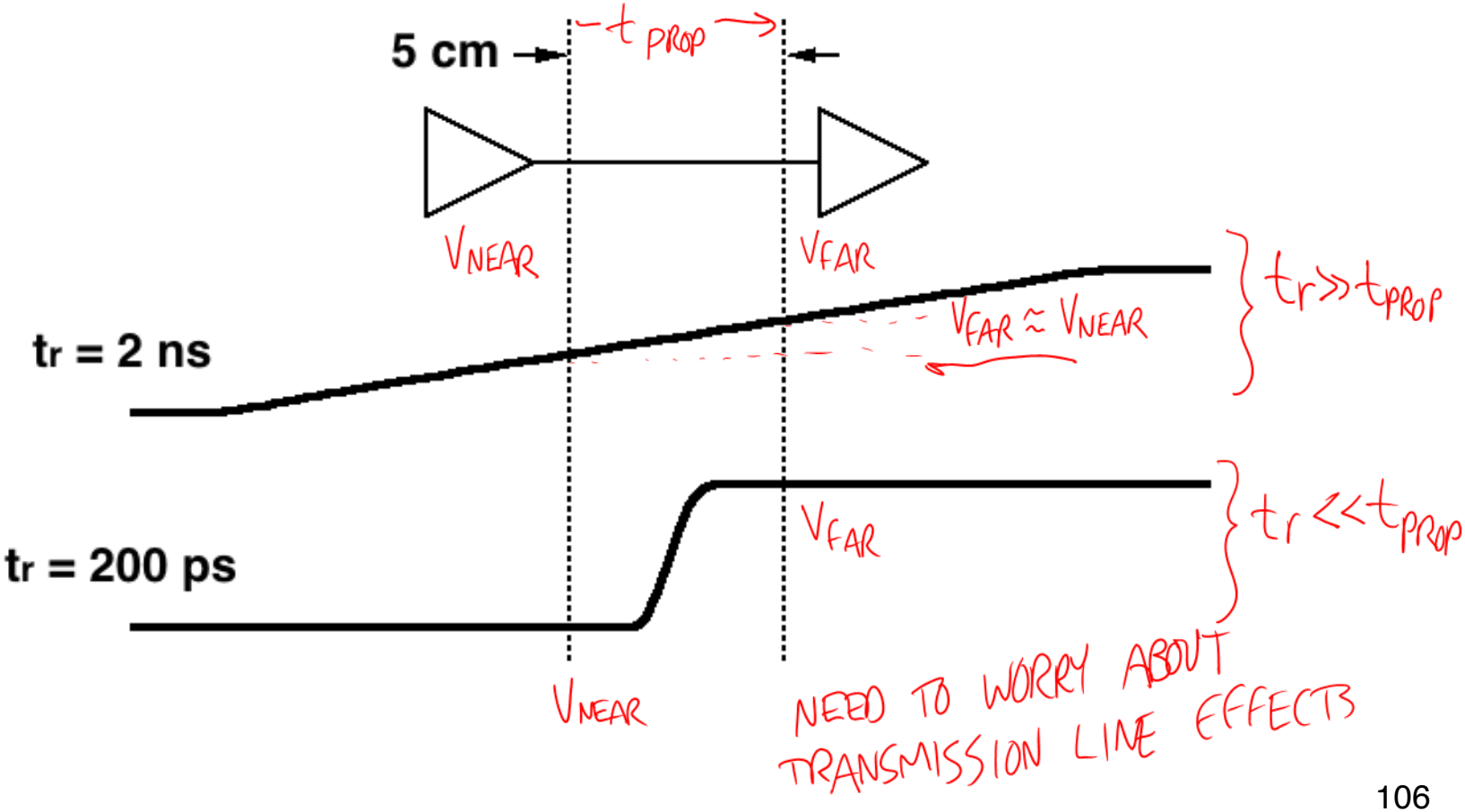
Transmission Lines

- When conductors become long (a significant fraction of the wavelength of the signals on them) they can no longer be represented as a simple *lumped-parameter* series R-L network
- The voltage and current will be different at different points along the conductor.
- Under these circumstances, the signal conductor and its return path must be considered together as a transmission line, and a *distributed-parameter* model of the line must be used.
- A common rule, when working in the frequency domain, is that the conductor should be treated as a transmission line if its length is greater than 1/10 of a wavelength
- In the case of a digital signal, in the time domain, when the signal rise time is less than twice the propagation delay (the reciprocal of the velocity of propagation) of the line.

Example: Slow, fast logic families

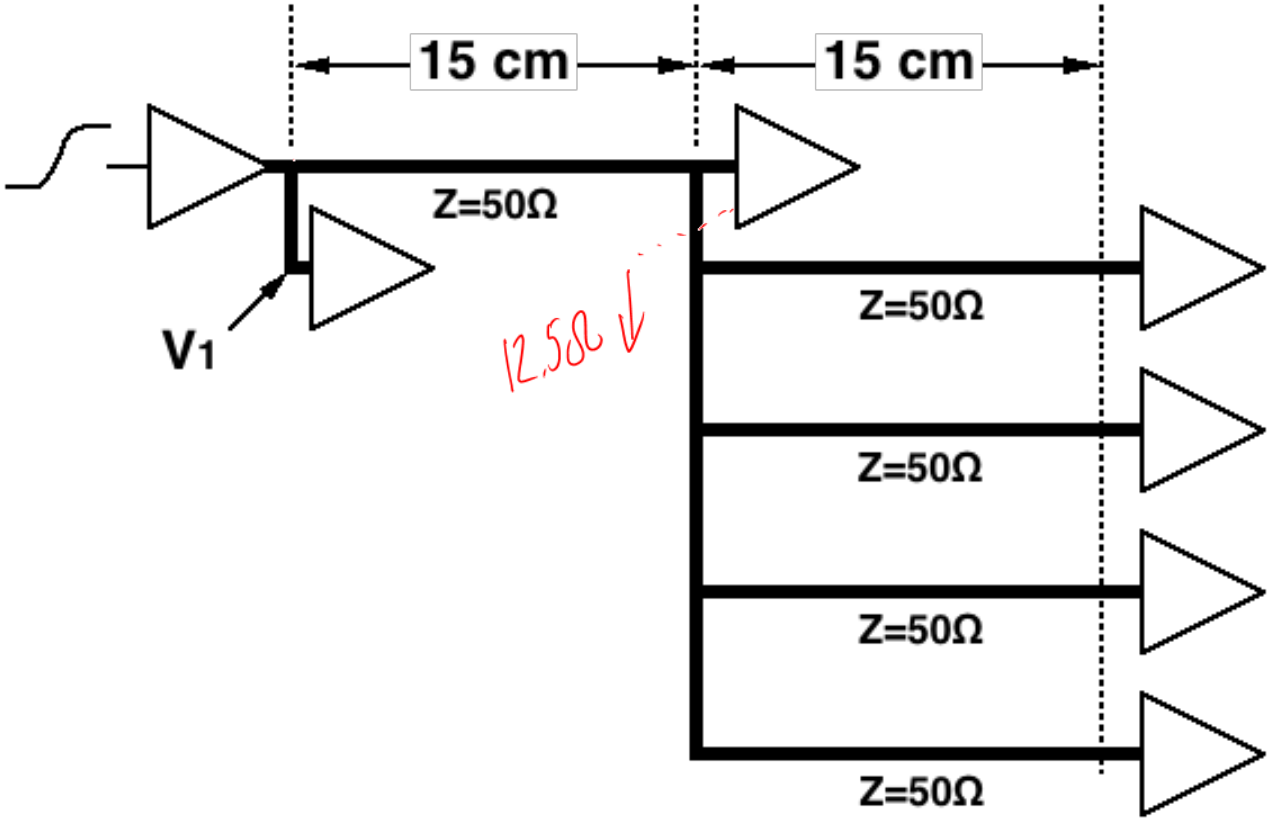
Faster Edge Rates

- Transmission Line Effects
- Rise time x Propagation velocity < Trace length



Reflection Example

- Clock Distribution Network

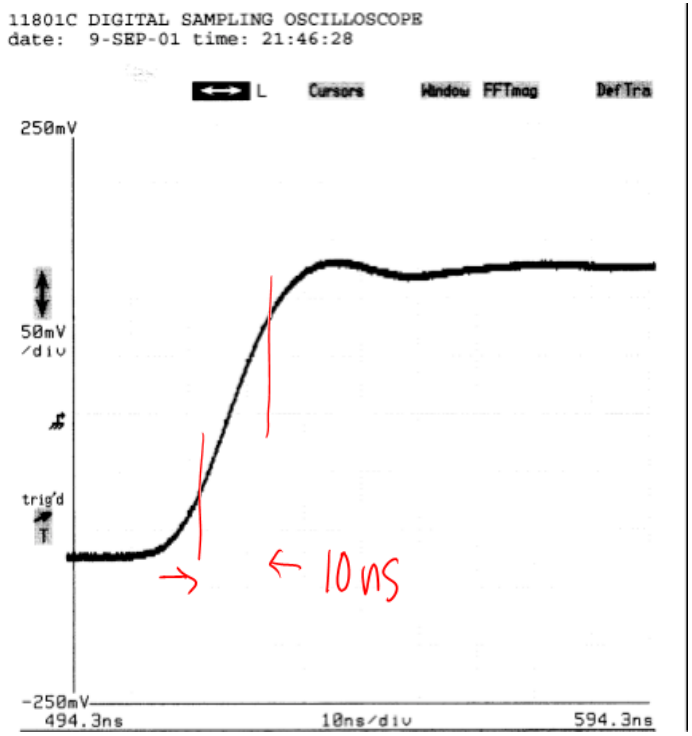


Reflection Example: $t_r \approx 10ns$

"LENGTH" OF EDGE

$$\underbrace{(1.0E-8[\text{sec}])}_{RISE\ TIME} \cdot \underbrace{(0.7 \cdot (3.0E+10[cm/\text{sec}]))}_{VELOCITY} = 210cm > 30cm$$

MAX LENGTH OF TRANSMISSION LINE

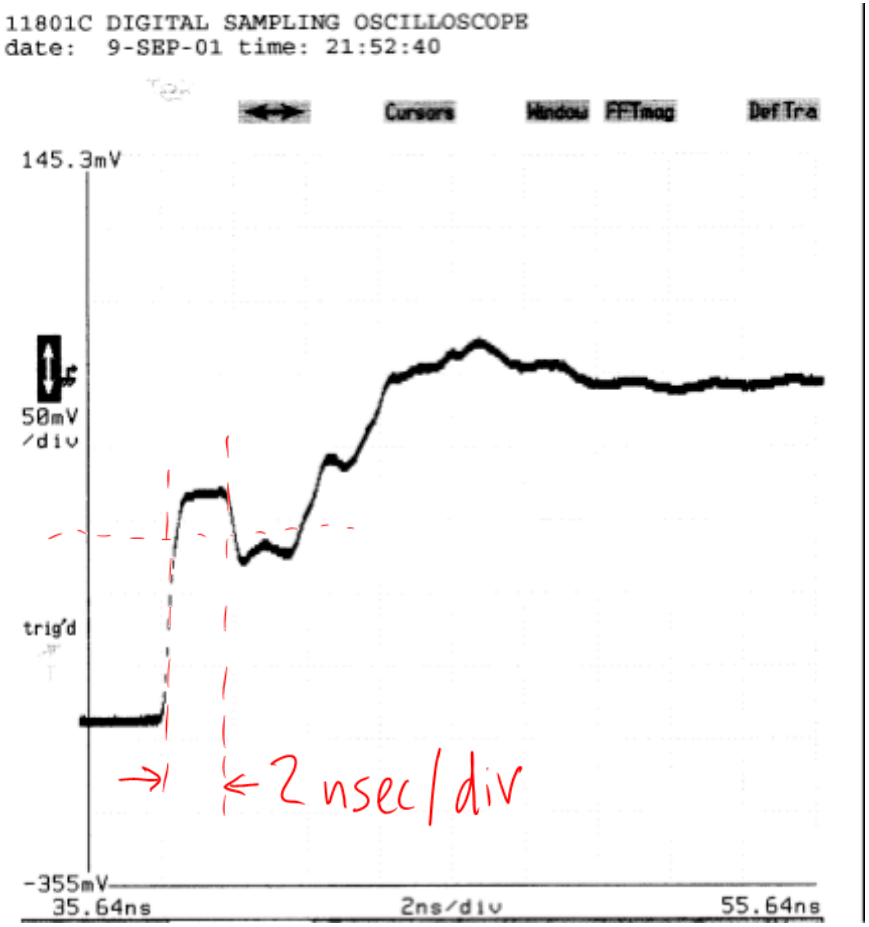


Transmission line effects negligible

Reflection Example: $t_r \approx 200ps$

$$\underbrace{\left(2.0E-10[\text{sec}]\right)}_{RISE\ TIME}\cdot\underbrace{\left(0.7\cdot\left(3.0E+10\left[cm/\text{sec}\right]\right)\right)}_{VELOCITY}=4.2cm<30cm$$

- Transmission line reflection problems:
  - –Multiple clocking
  - –Confusion for multilevel signaling (e.g. Rambus®)



Types of transmission lines

CABLE PCB CABLE

COAX MICROSTRIP STRIPLINE BALANCED LINE WAVEGUIDE

Note that the conductors of a transmission line are just the guides for the electromagnetic energy. The electromagnetic energy is propagated in the dielectric material. In a transmission line, the velocity of propagation v of the electromagnetic energy is equal to

$$v = \frac{c}{\sqrt{\varepsilon_r}}, \qquad (5\text{-}14)$$

DIELECTRIC CONST

The three most important properties of a transmission line are its characteristic impedance, its propagation constant, and its high-frequency *loss.*

Lossy transmission line

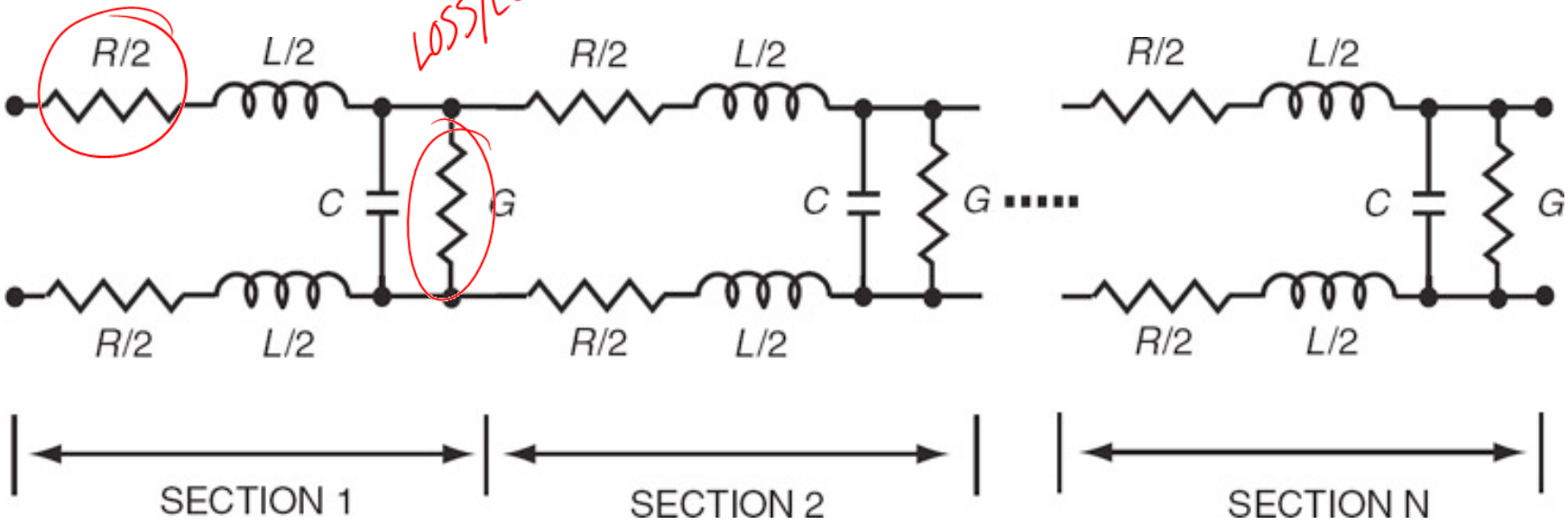


Figure 5-18: Distributed parameter model of a two-conductor transmission line

R, L, G, C PER UNIT LENGTH

Characteristic Impedance:

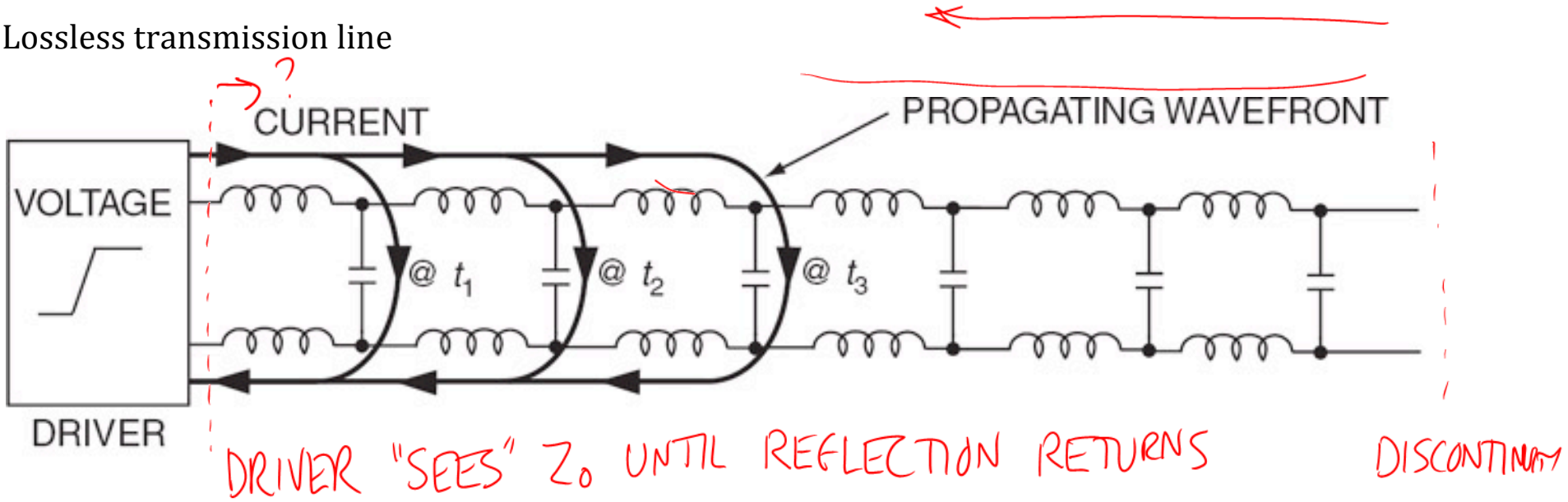
$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \qquad (5\text{-}15)$$

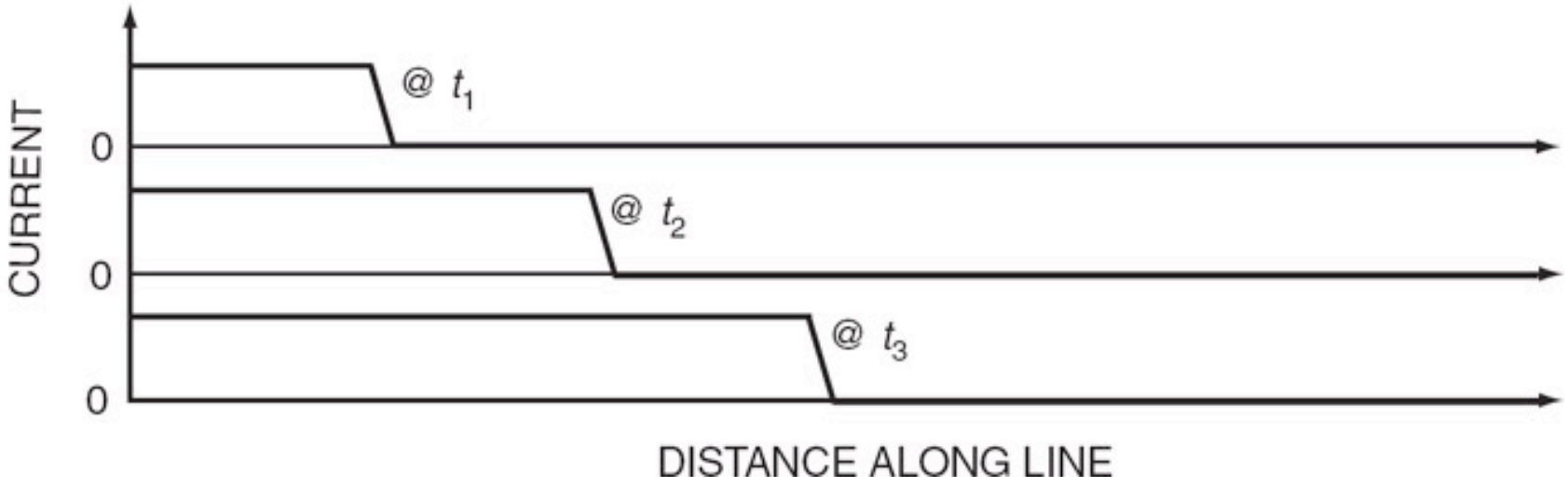
IN GENERAL, SOME VARIATION VS. ω DUE TO R, G LOSSES

IF (NEGLIGIBLE) LOSS $R \to 0$, $G \to 0$

$Z_0 = \sqrt{\frac{L}{C}}$ ω INDEPENDENT

Lossless transmission line





Propagation along lossy line

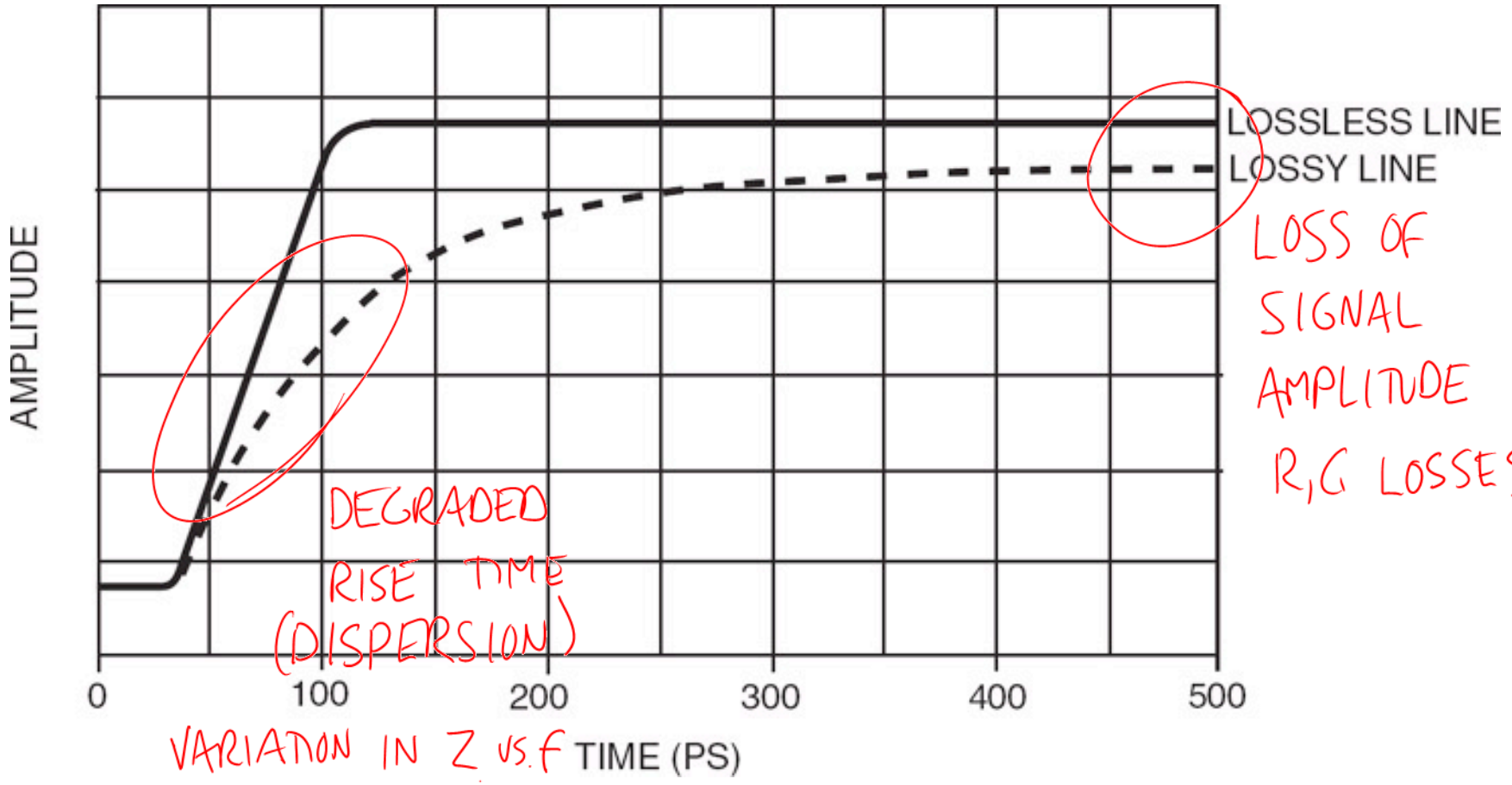


Figure 5-21: Time domain response of a square wave on a lossy transmission line, showing both amplitude and rise time degradation

CAN COUNTERACT WITH GAIN, EQUALIZATION IN RECEIVER

Ferrites

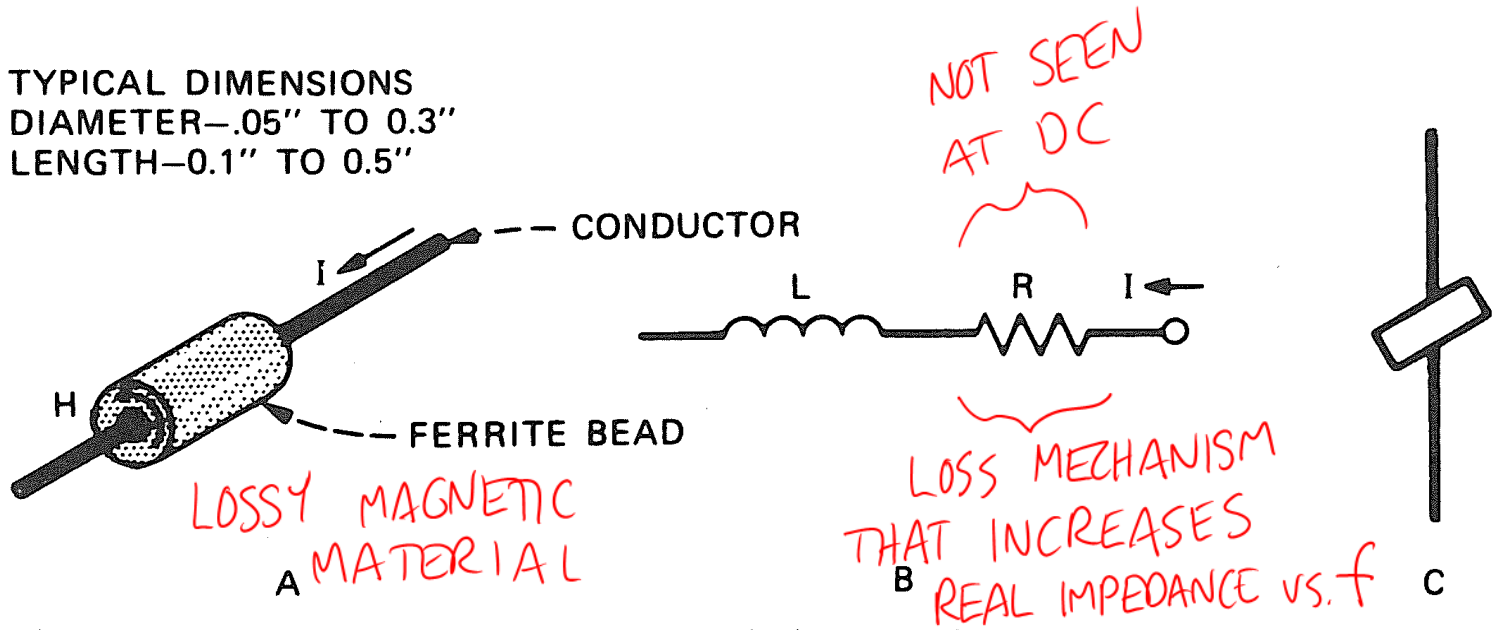


Figure 5-23: *(A)* Ferrite bead on conductor, *(B)* high-frequency equivalent circuit, and (C) typical schematic symbol

Ferrites specified by impedance vs. frequency

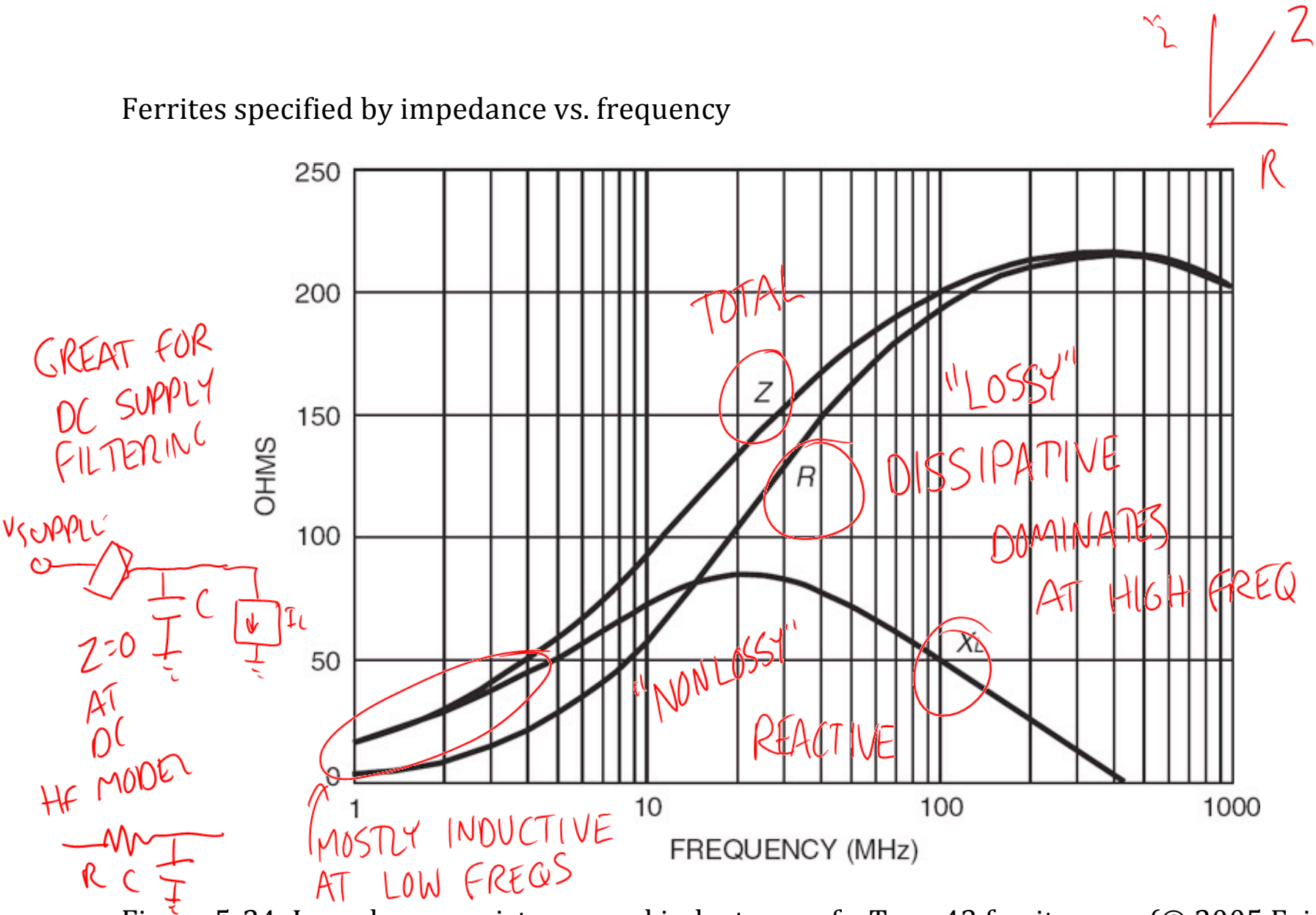


Figure 5-24: Impedance, resistance, and inductance of a Type 43 ferrite core. (© 2005 Fair-Rite Corp., reproduced with permission

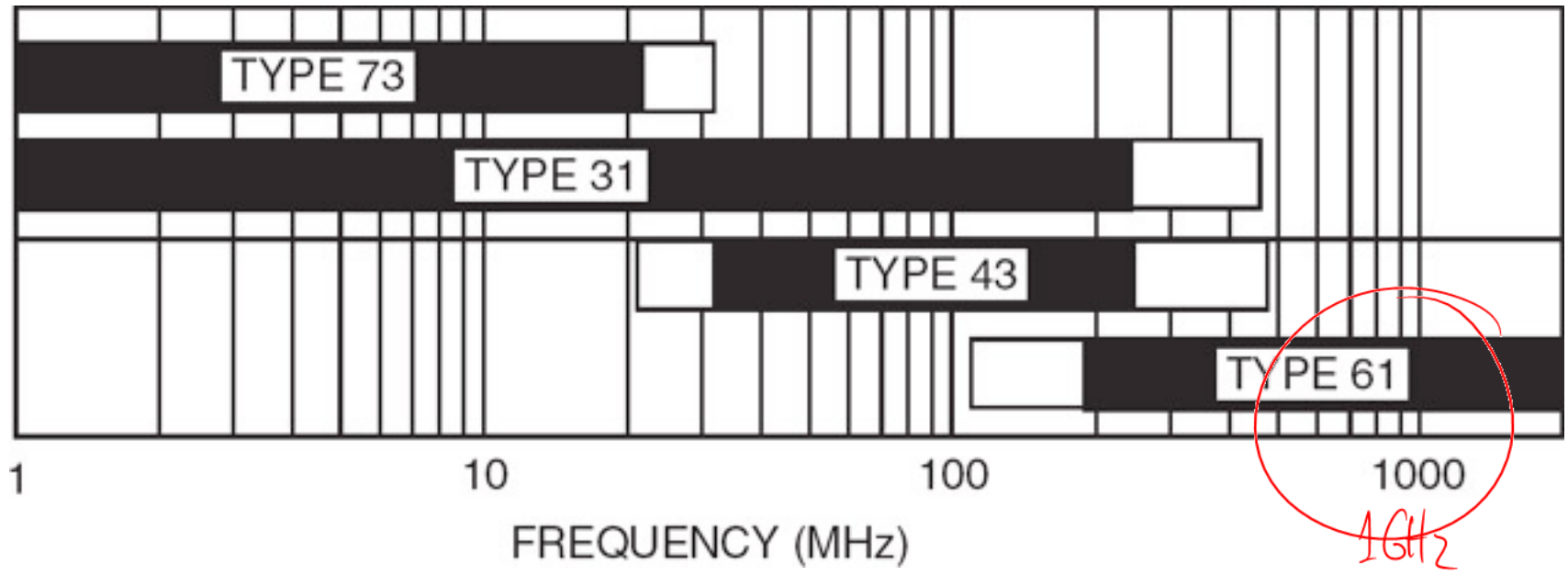


Figure 5-25: Recommended frequency range of various ferrite materials when used in noise suppression applications. (© 2005 Fair-Rite Corp., reproduced with permission

SPECIFIED BY |Z| AT FREQ / OVER f RANGE

REACTIVE OR DISSIPATIVE

NON-LOSSY LOSSY

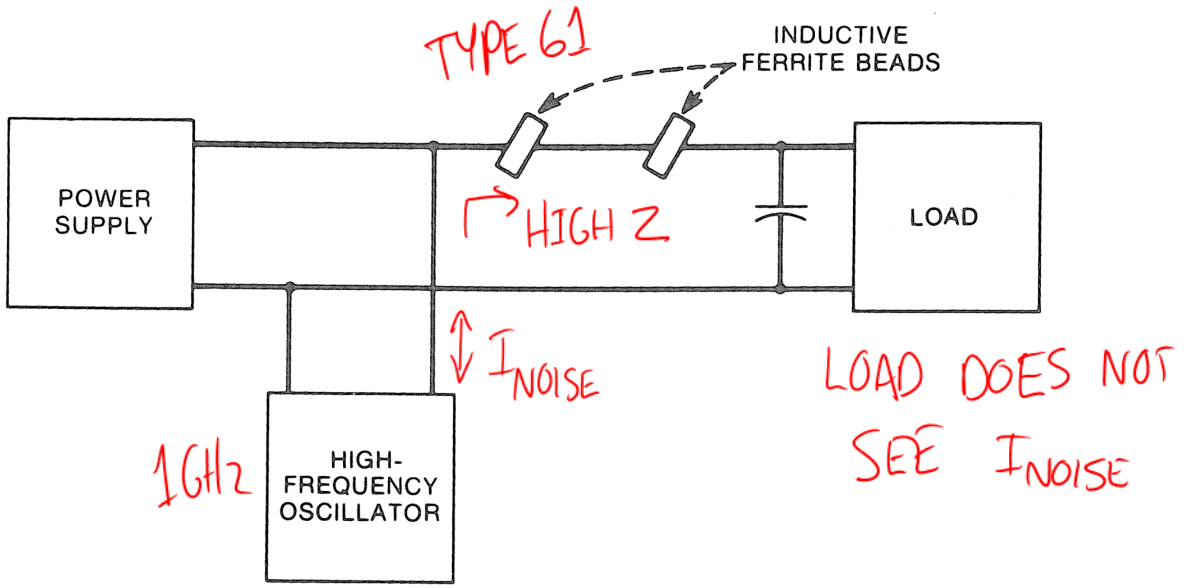


Figure 5-26: Ferrite bead used to form a L-filter to keep high-frequency oscillator noise from the load

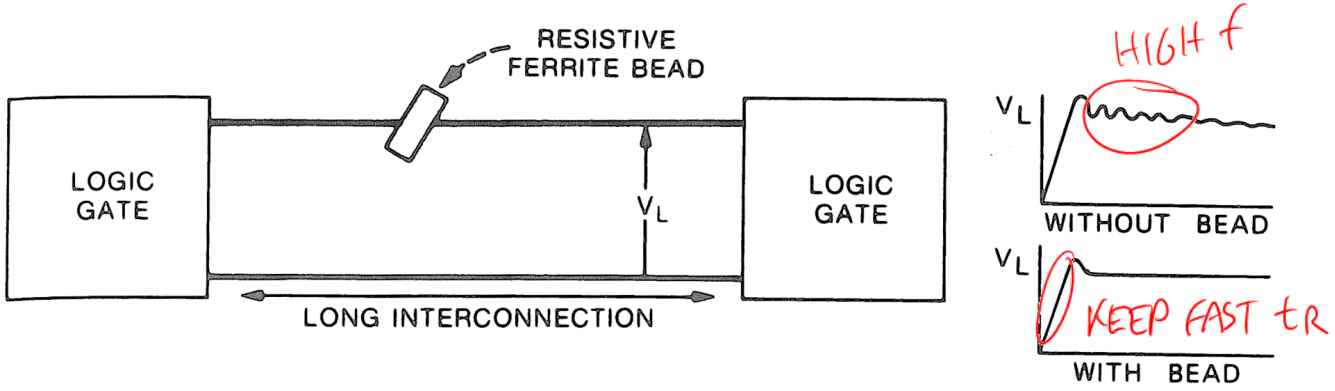


Figure 5-27: Resistive ferrite bead used to damp out ringing on long interconnection between fast logic gates

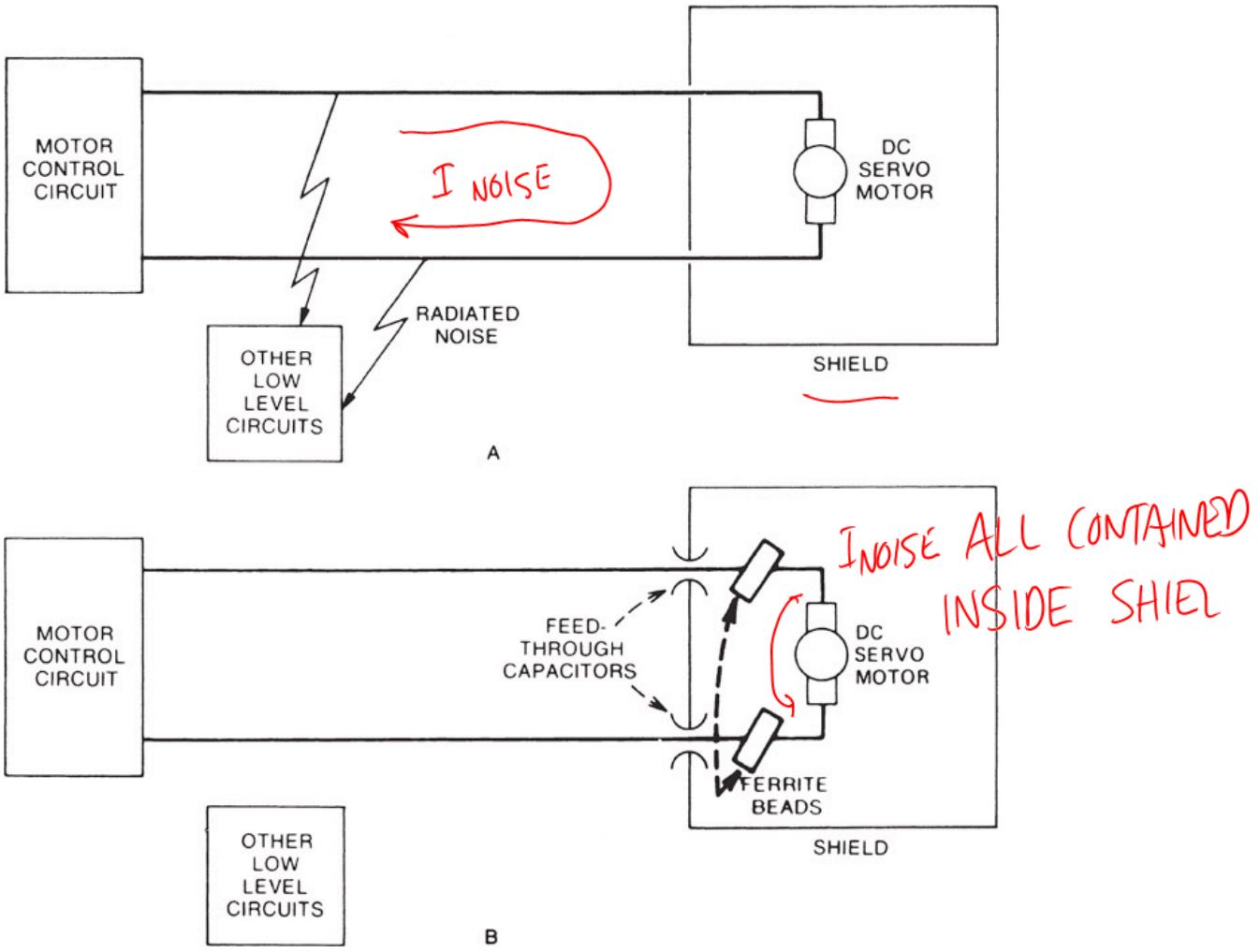


Figure 5-29: *(A)* High-frequency commutation noise of motor is interfering with low-level circuits, *(B)* ferrite bead used in conjunction with feed-through capacitors to eliminate interference

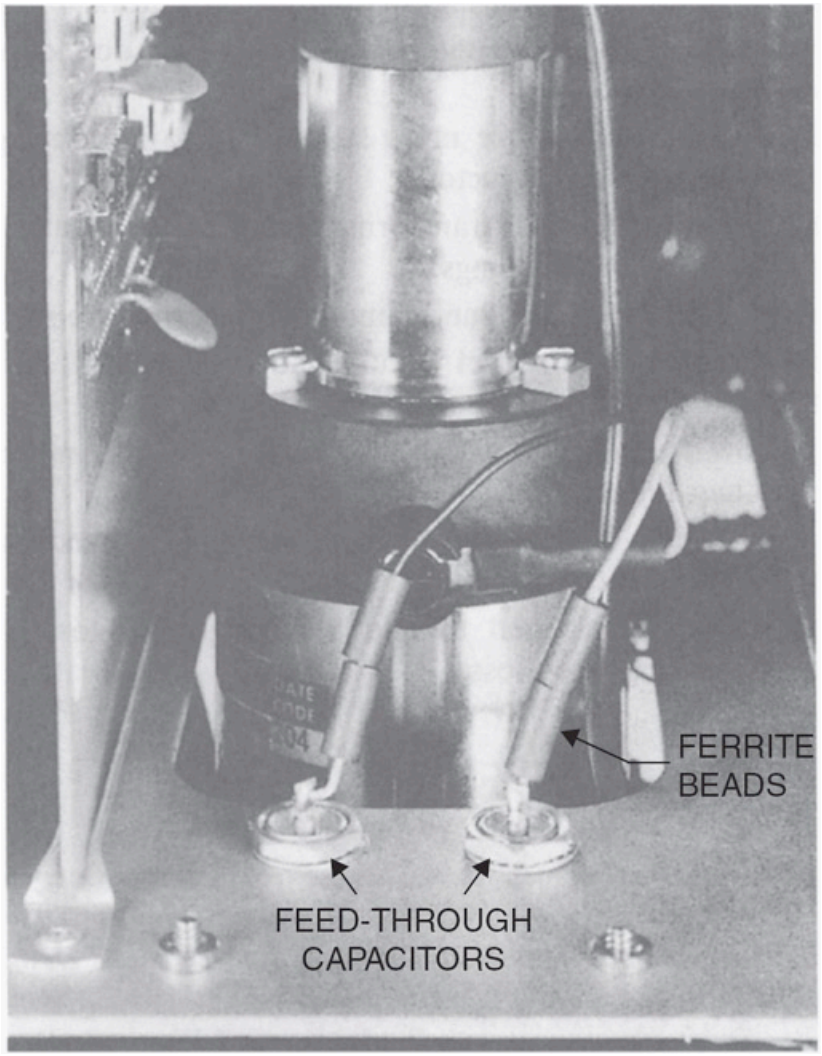


Figure 5-30: Ferrite beads and feed-through capacitors used to filter commutation noise on dc motor's power leads

Caution: Saturation of ferrite in presence of DC bias

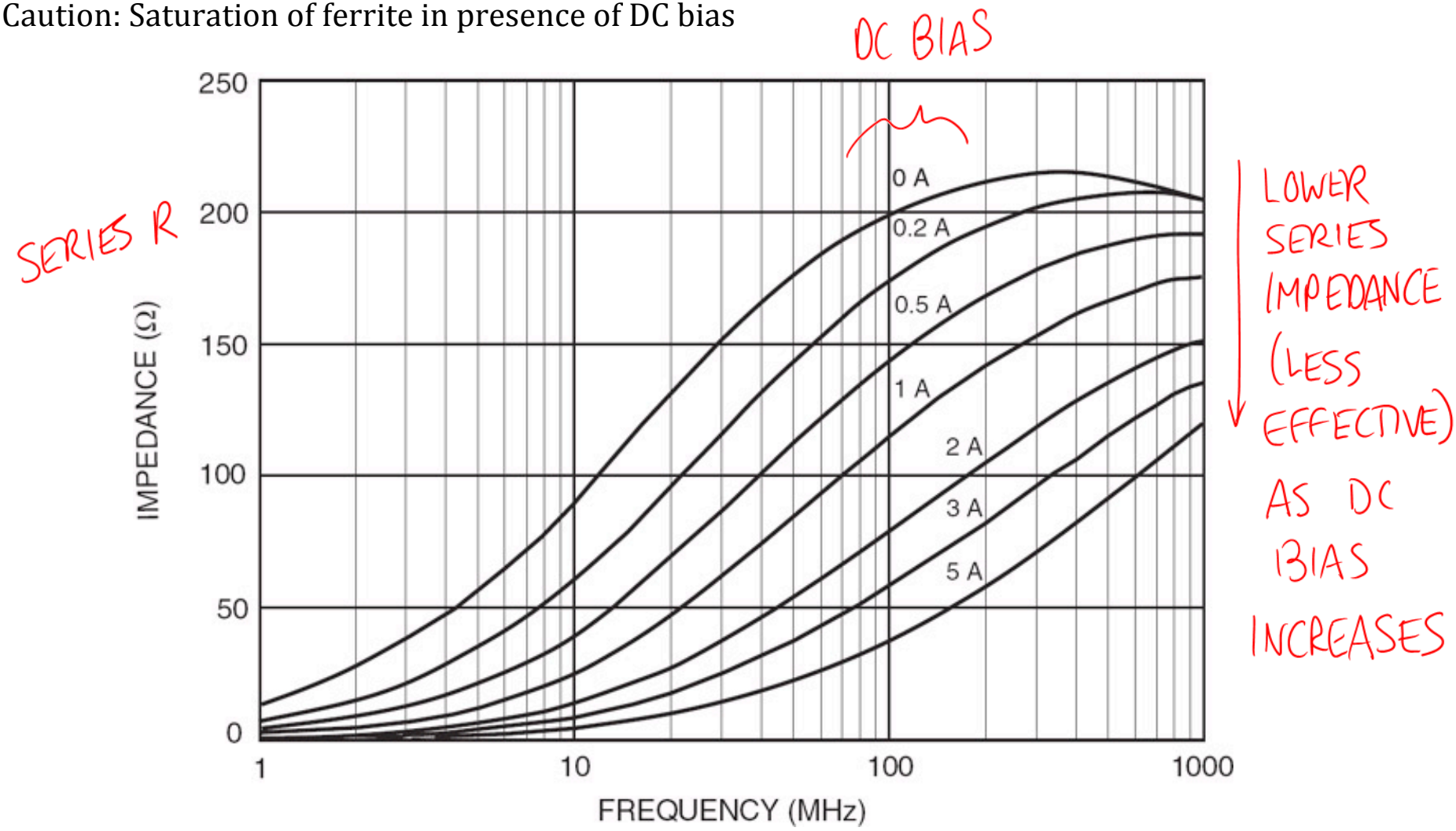


Figure 5-31: Impedance versus frequency plot of a ferrite bead as a function of the dc bias current.
(© 2005, Fair-Rite Products Corp., reproduced with permission

- Ferrite cores are commonly used as CM chokes (sec. 3.5) on multiconductor cables.
- The ferrite core acts as a one-turn transformer or common-mode choke, and can be effective in reducing the conducted and/or radiated emission from the cable, as well as suppressing high-frequency pickup in the cable.
- Figure 5-32 shows a ferrite core on a universal serial bus (USB) cable used to reduce the radiated emission from the cable.
- Snap-on cores (shown in Fig 5-22) can also be applied easily as an after-the-fact fix to cables, even if they have large connectors at the ends.

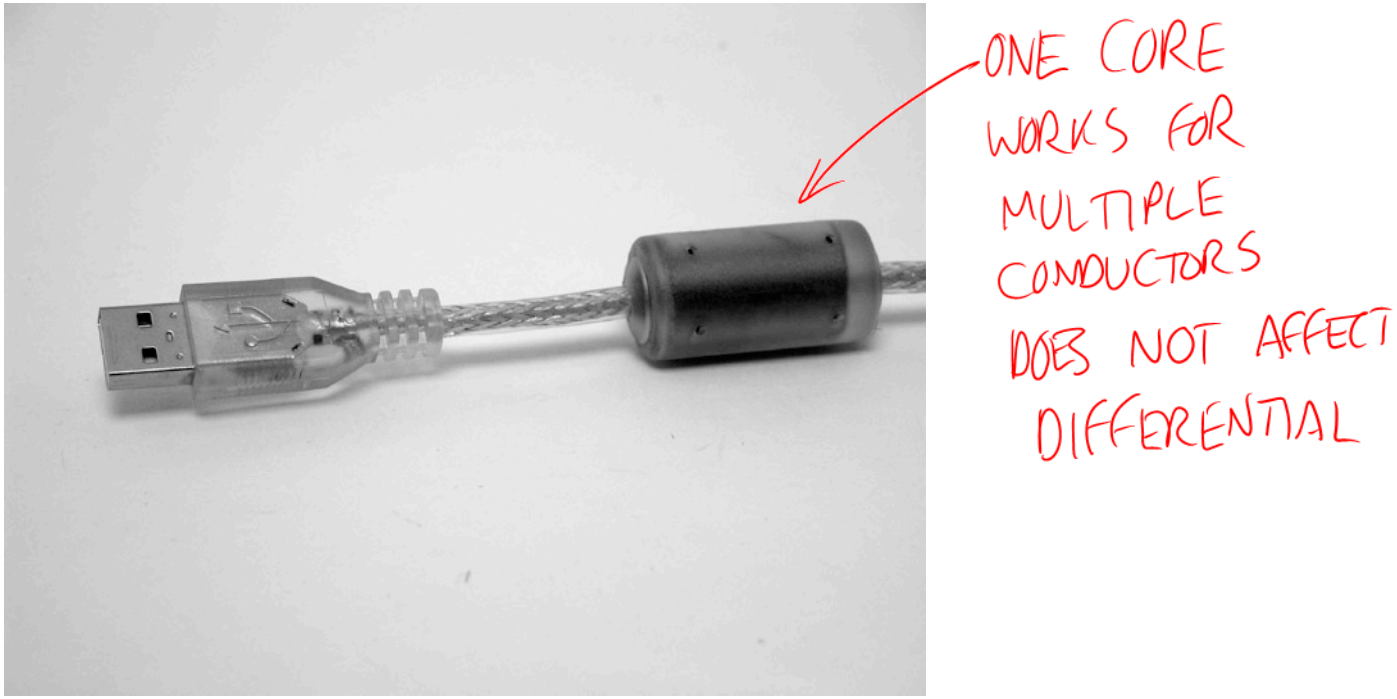


Figure 5-32: Ferrite core used on a USB cable to suppress radiated emissions

Summary: Ideal vs. Real Components:

- Capacitors
  All capacitors have a self resonant frequency (SRF) and look inductive for frequencies > SRF
  Multilayer ceramic capacitors (MLCC) have highest SRF and are least nonideal
- Inductor
  Closed core inductors (e.g. toroids) create less external magnetic field
  Parasitic capacitance limits frequency range over which inductors behave inductively
- Transformer
  Parasitic capacitance also limits effectiveness of transformer isolation
- Resistor
  In terms of noise, metal film resistors are more nearly ideal than carbon composition
- Conductor
  Above audio frequencies, a conductor has more inductive reactance than resistance.
  Flat rectangular conductor will have less ac resistance and inductance than a round shape.
- Transmission Lines
  Important when conductor length is longer than 1/10 wavelength
- Ferrite Beads
  When used for noise suppression, ferrites are used in the frequency range where their impedance is resistive.
  Ferrites couple ac resistance (loss) into a circuit with little or no low-frequency impedance.
  Ferrites are normally characterized by specifying their impedance versus frequency.

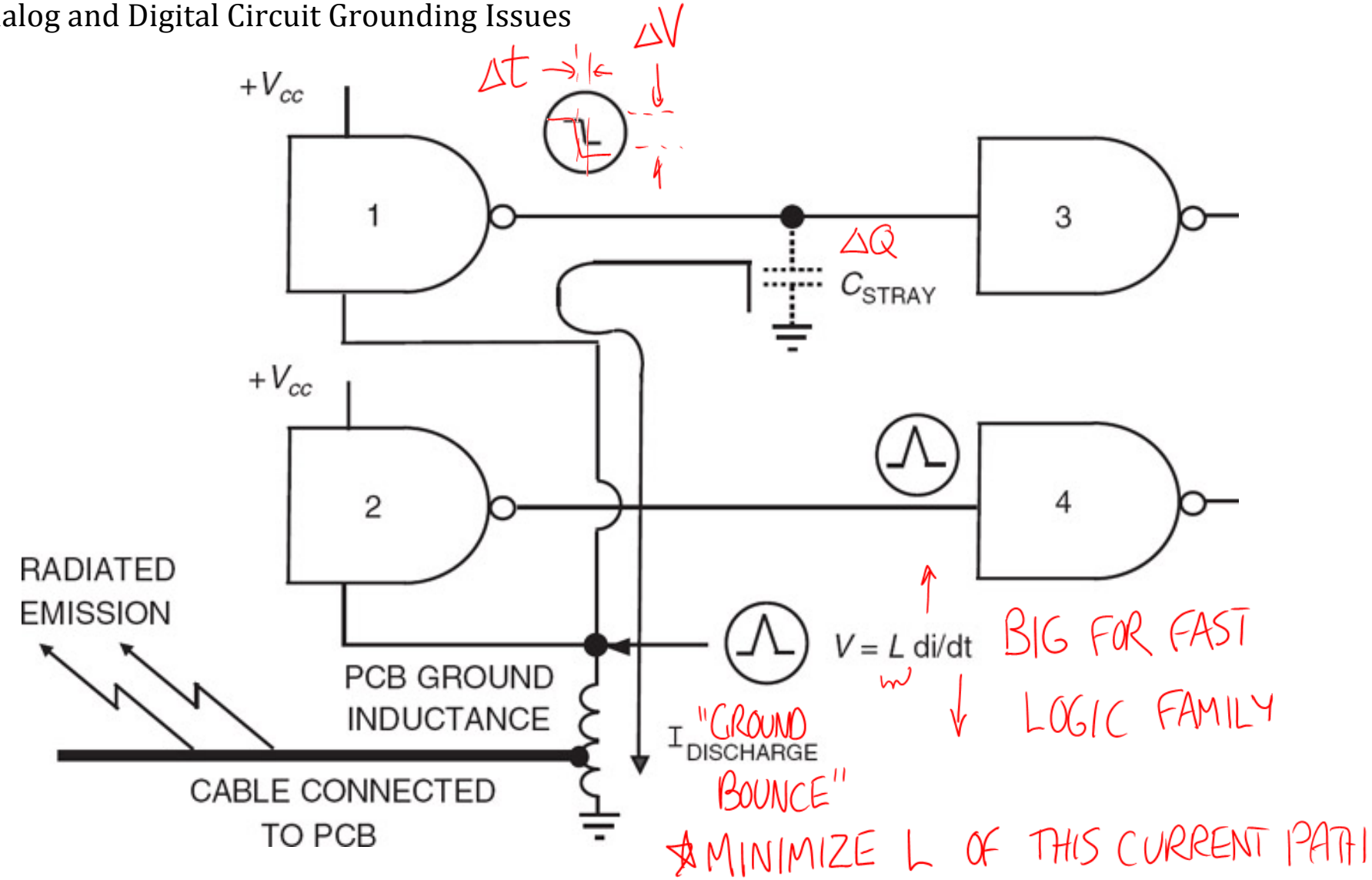


Figure 10-1: Ground noise is created when output of gate 1 switches from high to low

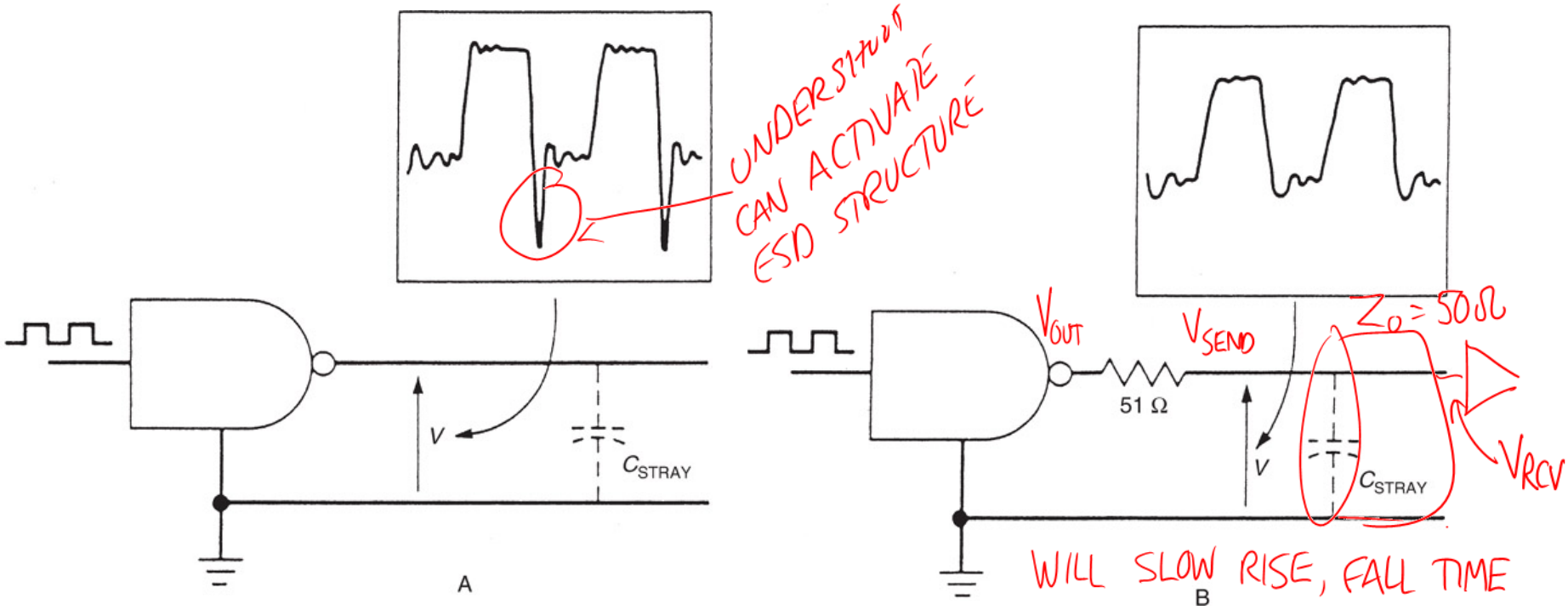
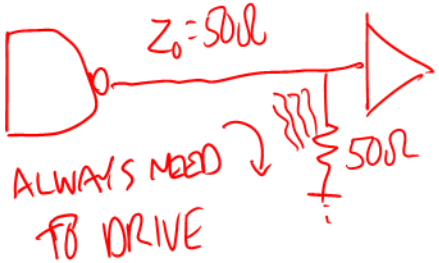


Figure 10-2
TTL output voltage waveshape with (A) ringing caused by stray capacitance and ground inductance, and
(B) ringing damped by the addition of an output resistor

TERMINATION OPTIONS WHEN TRANSMISSION LINE EFFECTS ARE

RECEIVE END



TERMINATE AT SEND END

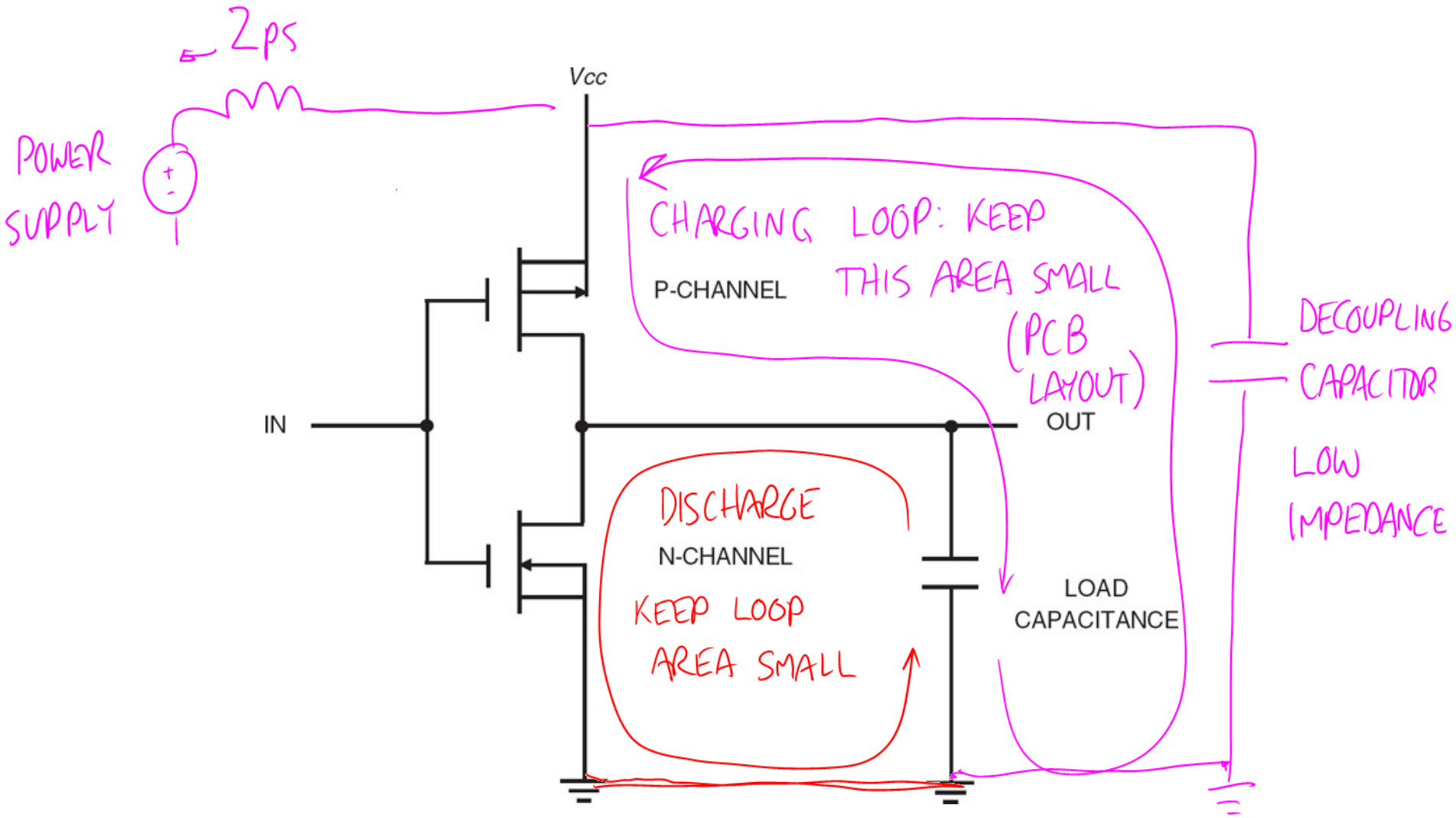


Figure 10-3: Basic schematic for a CMOS logic gate that has a totem pole output circuit

Table 10-1: Impedance of a 1-in Long Printed Circuit Board Trace (15 nH of inductance)

Frequency (MHz)	Rise Time (ns)	Impedance (Ω)
1	318	0.1
10	32	1
30	11	2.8
50	6.4	4.7
100	3.2	9.4
300	1.1	28
500	0.64	47
1000	0.32	94

IMPORTANCE OF MINIMIZING TRACE LENGTH FOR CHARGE DISCHARGE CURRENTS

1 GHz

A typical printed circuit board (PCB) trace (a 1-oz copper conductor 0.006 in. wide, and 0.02 in. from a return conductor) has a resistance of 82 mΩ/in (Eq. 5-10) and a loop inductance of 15 nH/in (Eq. 10-5). The impedance of the 15-nH inductance versus frequency, which is related to the logic rise/fall time by Eq. 10-2, is given in Table 10-1.

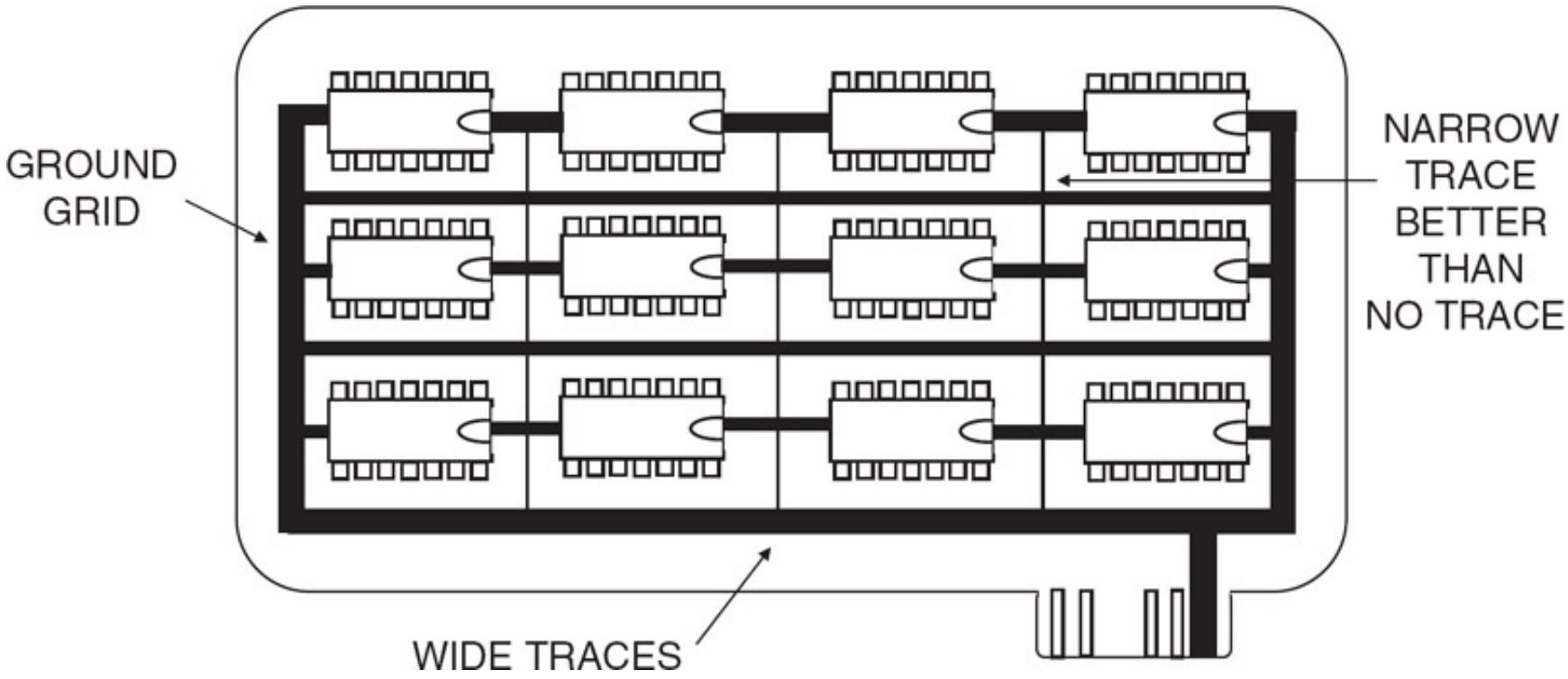


Figure 10-5: A grid-type ground on a printed circuit board

BAD: SLOT

LARGE
LOOP
AREA
HIGHER L,
|Z|

Figure 10-6: Typical printed circuit board ground plane

OK TO HAVE SMALL HOLES AS LONG AS
A SMALL LOOP CURRENT PATH IS AVAILABLE

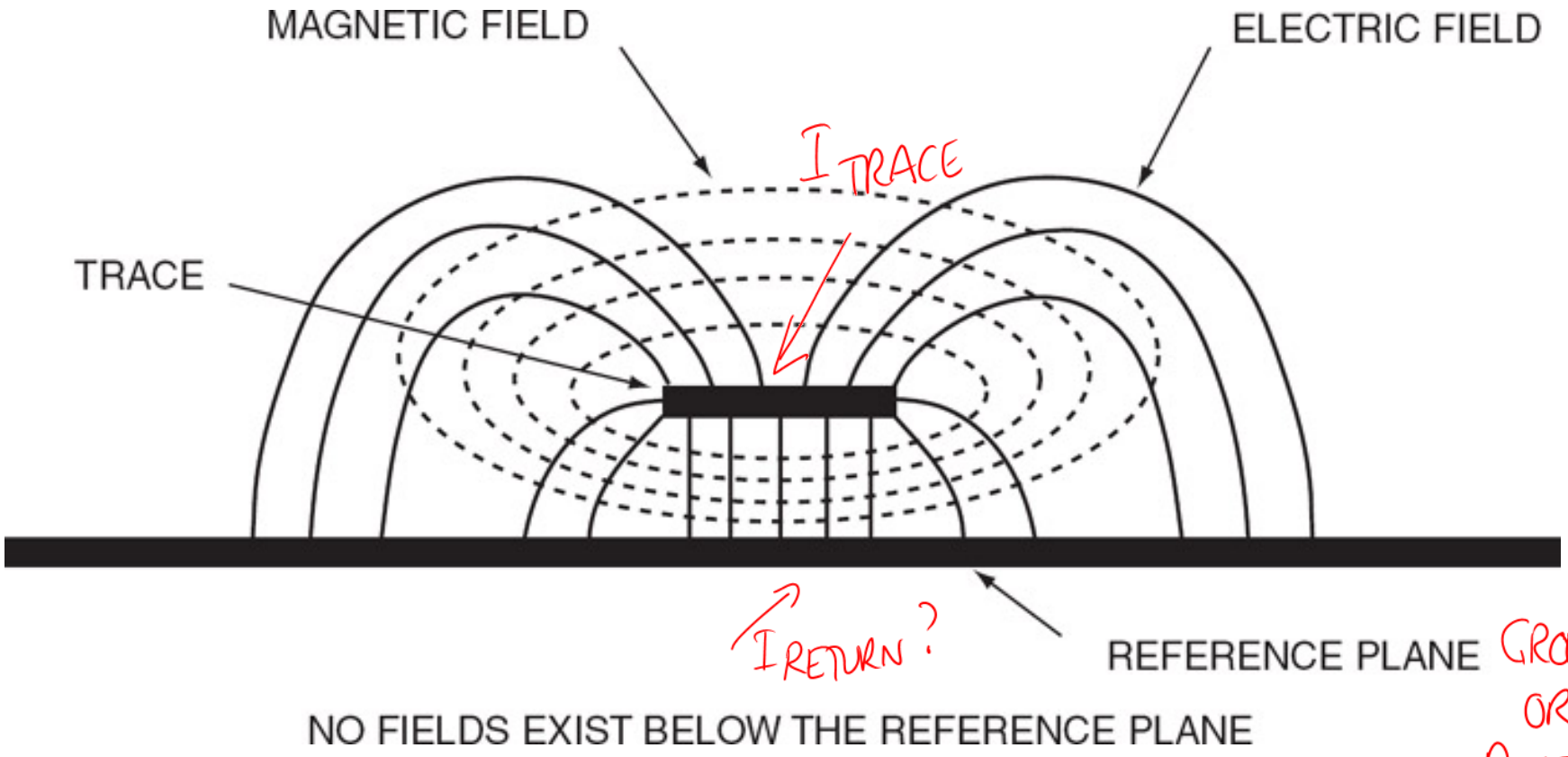


Figure 10-7: Electric and magnetic fields surrounding a microstrip line

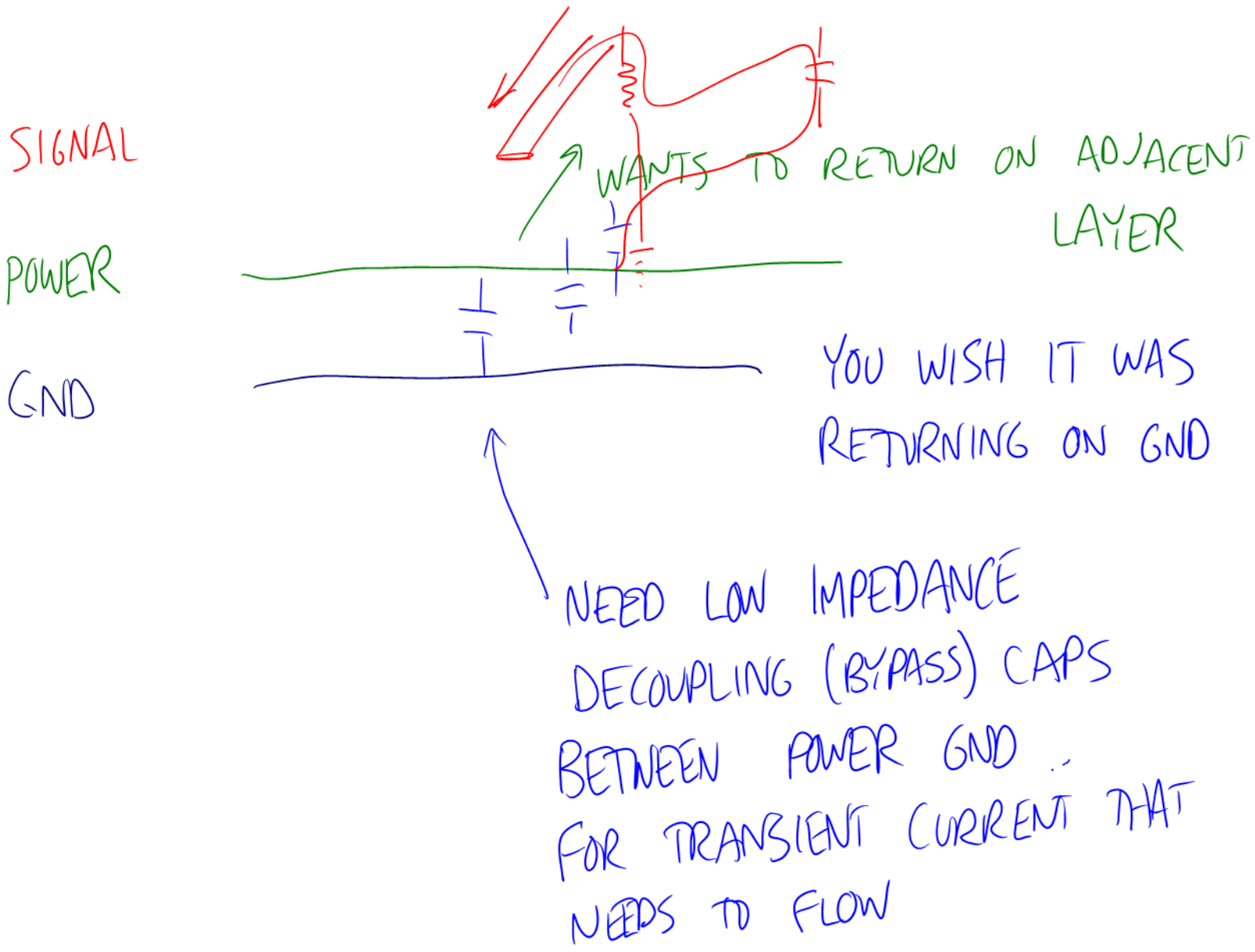
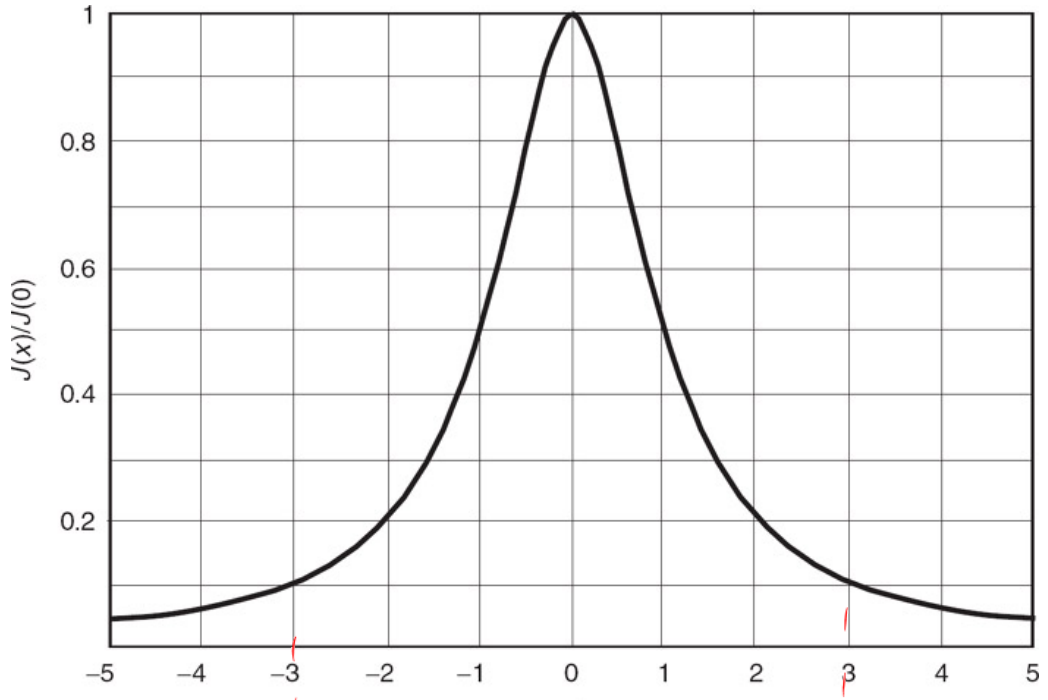
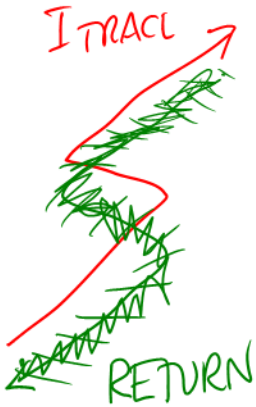

SIGNAL
POWER
GND
WANTS TO RETURN ON ADJACENT LAYER
YOU WISH IT WAS RETURNING ON GND
NEED LOW IMPEDANCE DECOUPLING (BYPASS) CAPS BETWEEN POWER GND FOR TRANSIENT CURRENT THAT NEEDS TO FLOW

Figure 10-9: Normalized reference plane current density for a microstrip line



NORMALIZED CURRENT DENSITY



RETURN CURRENT "WANTS" TO BE UNDERNEATH

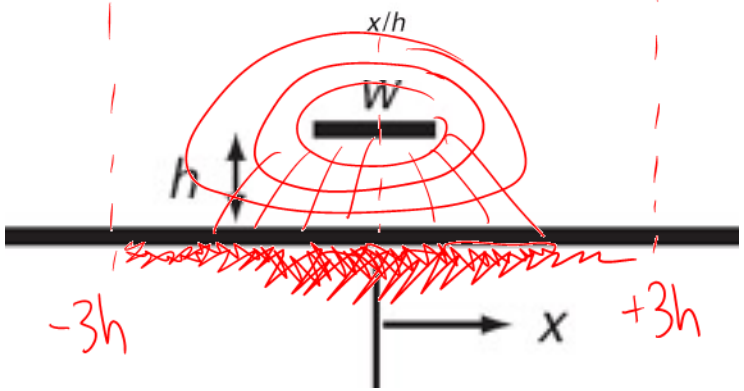
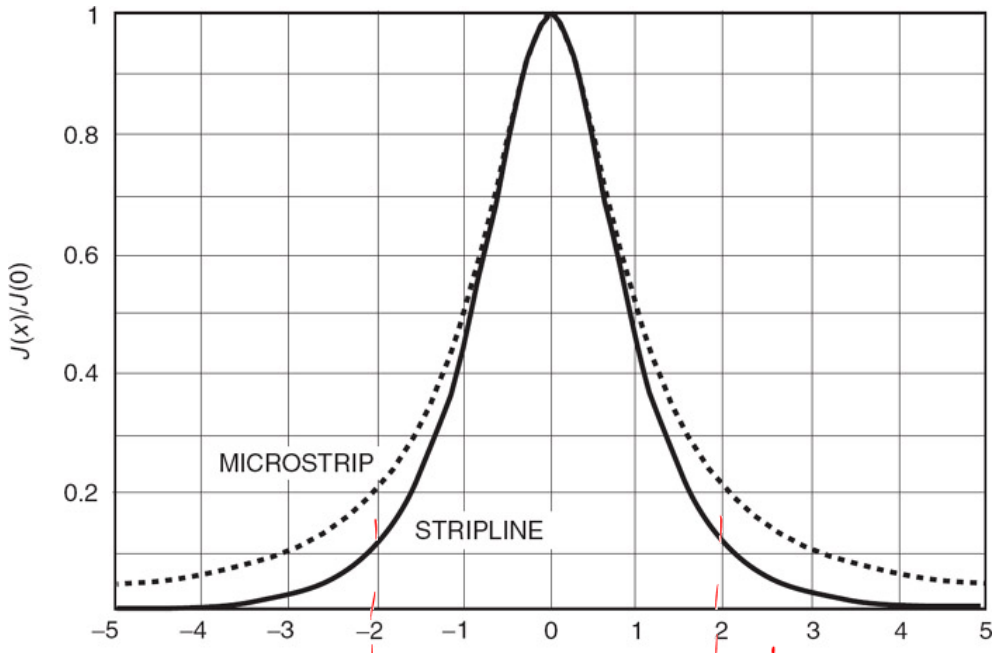


Figure 10-8: Configuration of a microstrip line

CURRENT "WANTS" TO RETURN IN A CLOSE (SMALL LOOP) PATH

⇒ BE SURE PCB LAYOUT ALLOWS A CONTINUOUS PATH FOR THIS LOOP!

Figure 10-12: Normalized reference plane current densities for a stripline (solid) and microstrip (dotted)



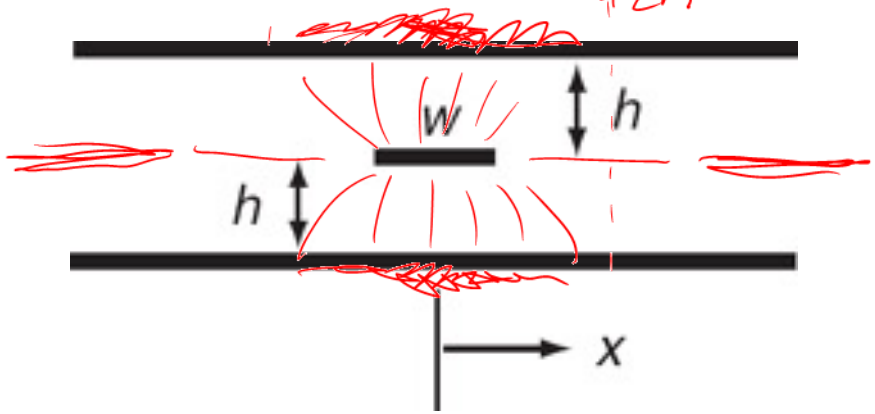


Figure 10-11: Configuration of a stripline

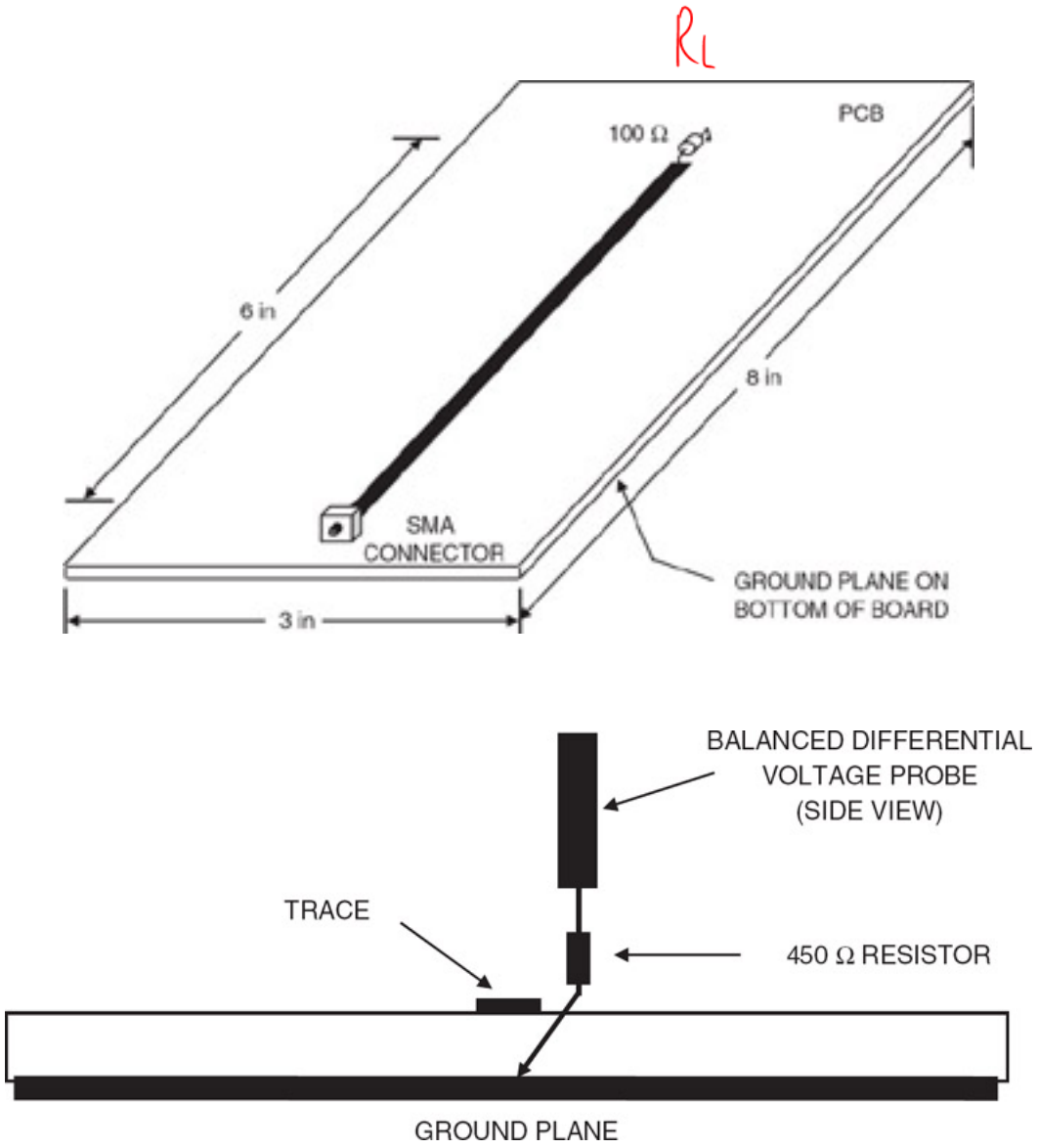


Figure 10-17: Test board for ground plane inductance measurements

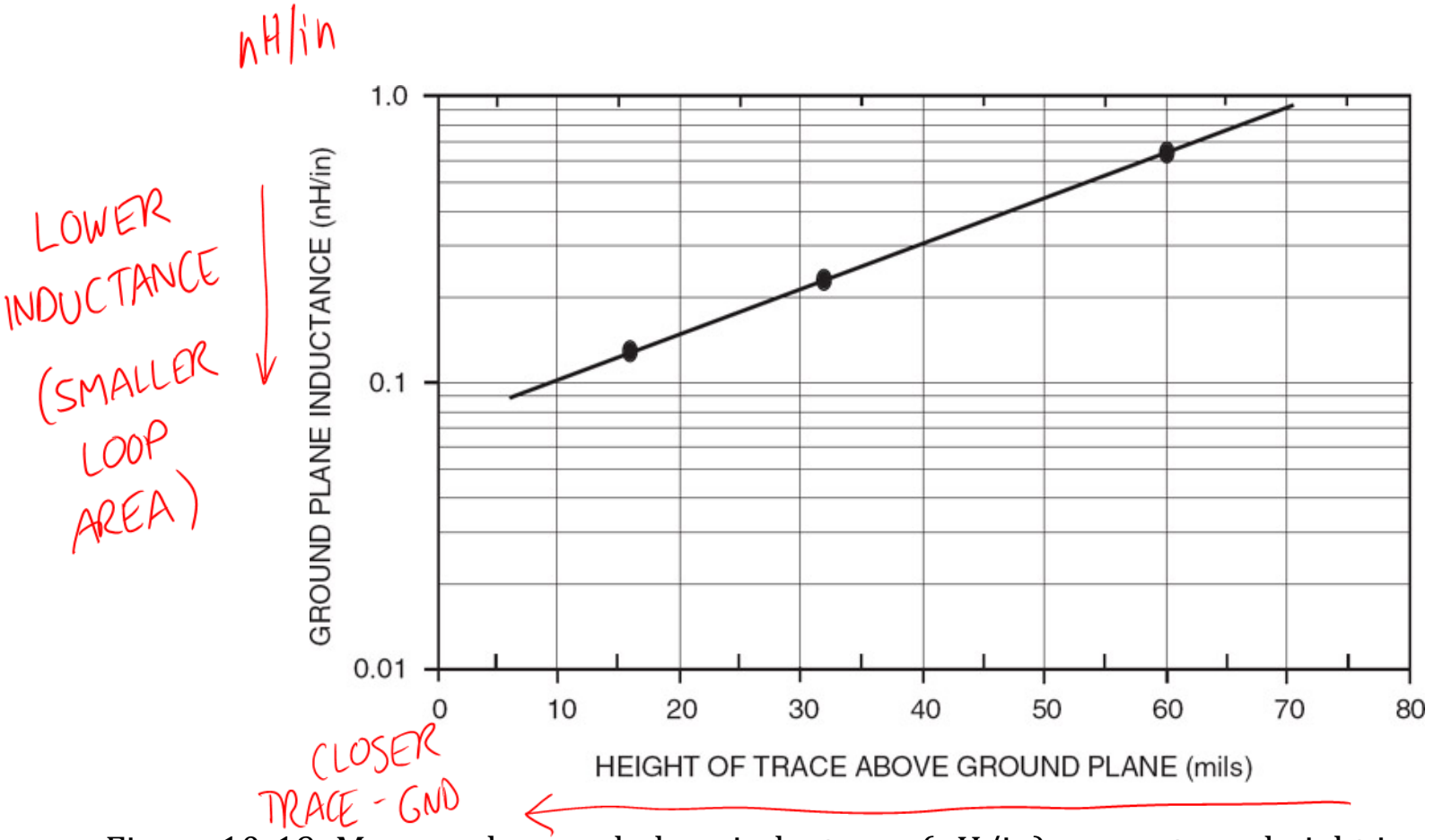


Figure 10-19: Measured ground plane inductance (nH/in) versus trace height in mils (1-mil = 0.001 in). Data point for 7-mil trace height omitted from plot because it is believed to be in error, see Section 10.6.2.3

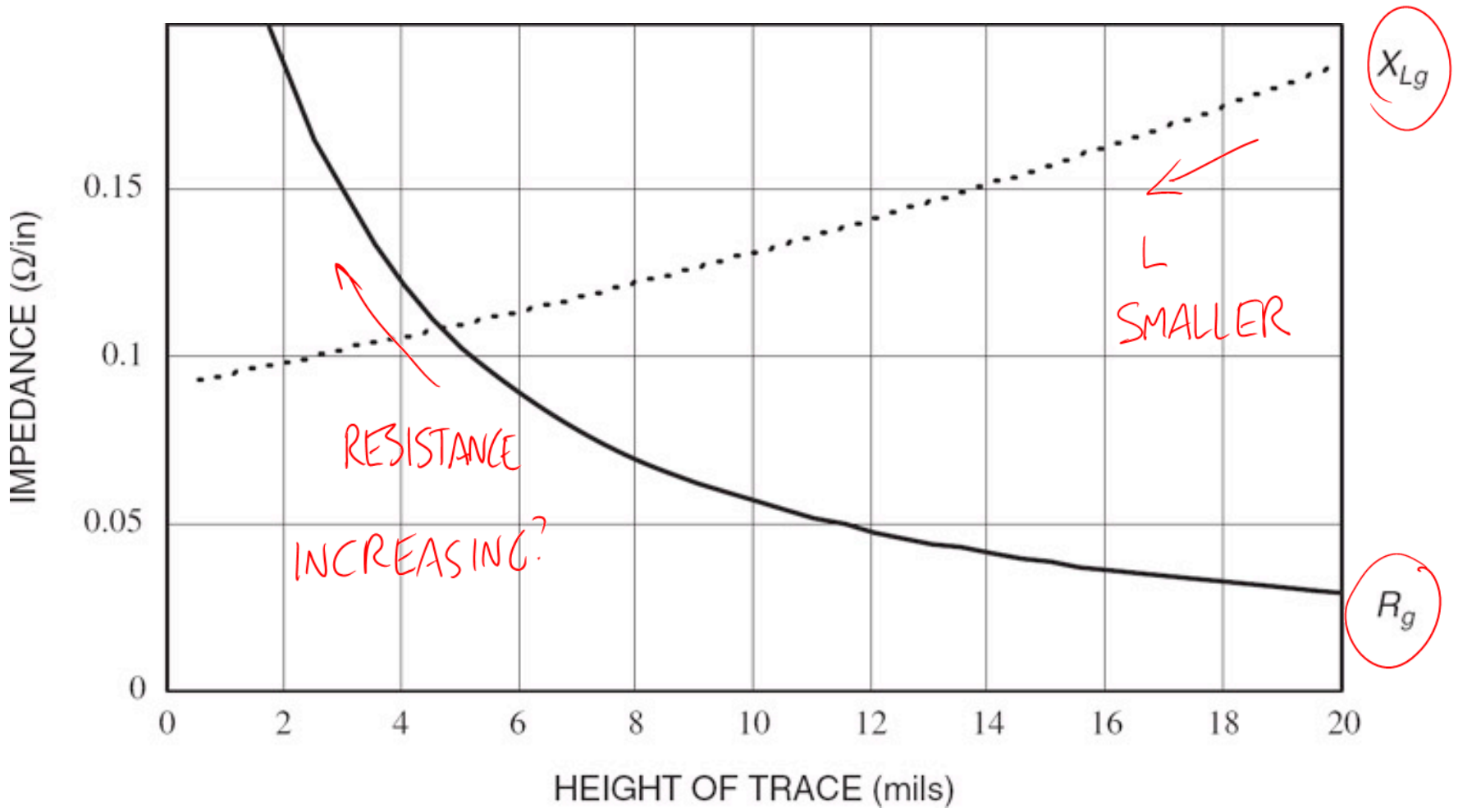
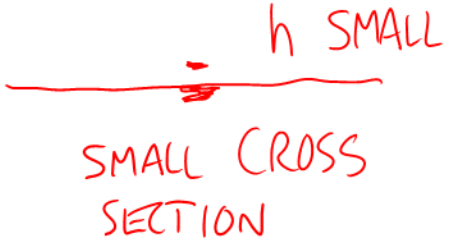
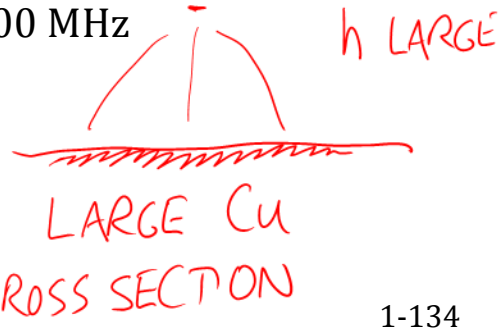


Figure 10-23: Ground plane inductive reactance *XLg* and resistance *Rg* for a 0.010-in-wide trace, as a function of trace height in mils at a frequency of 200 MHz





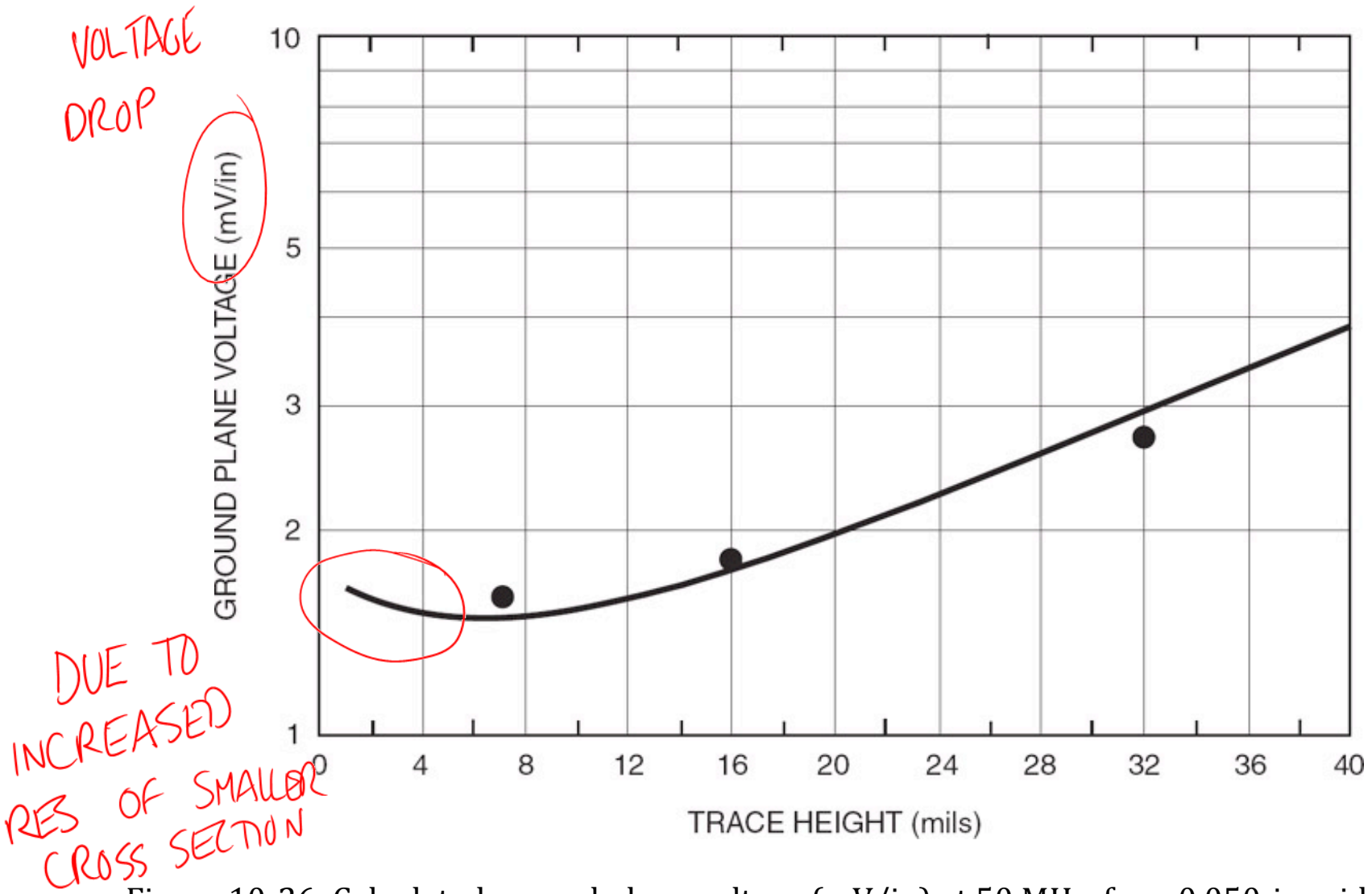


Figure 10-26: Calculated ground plane voltage (mV/in) at 50 MHz, for a 0.050-in-wide trace. Measured values are indicated by the dots

FIG 10.8

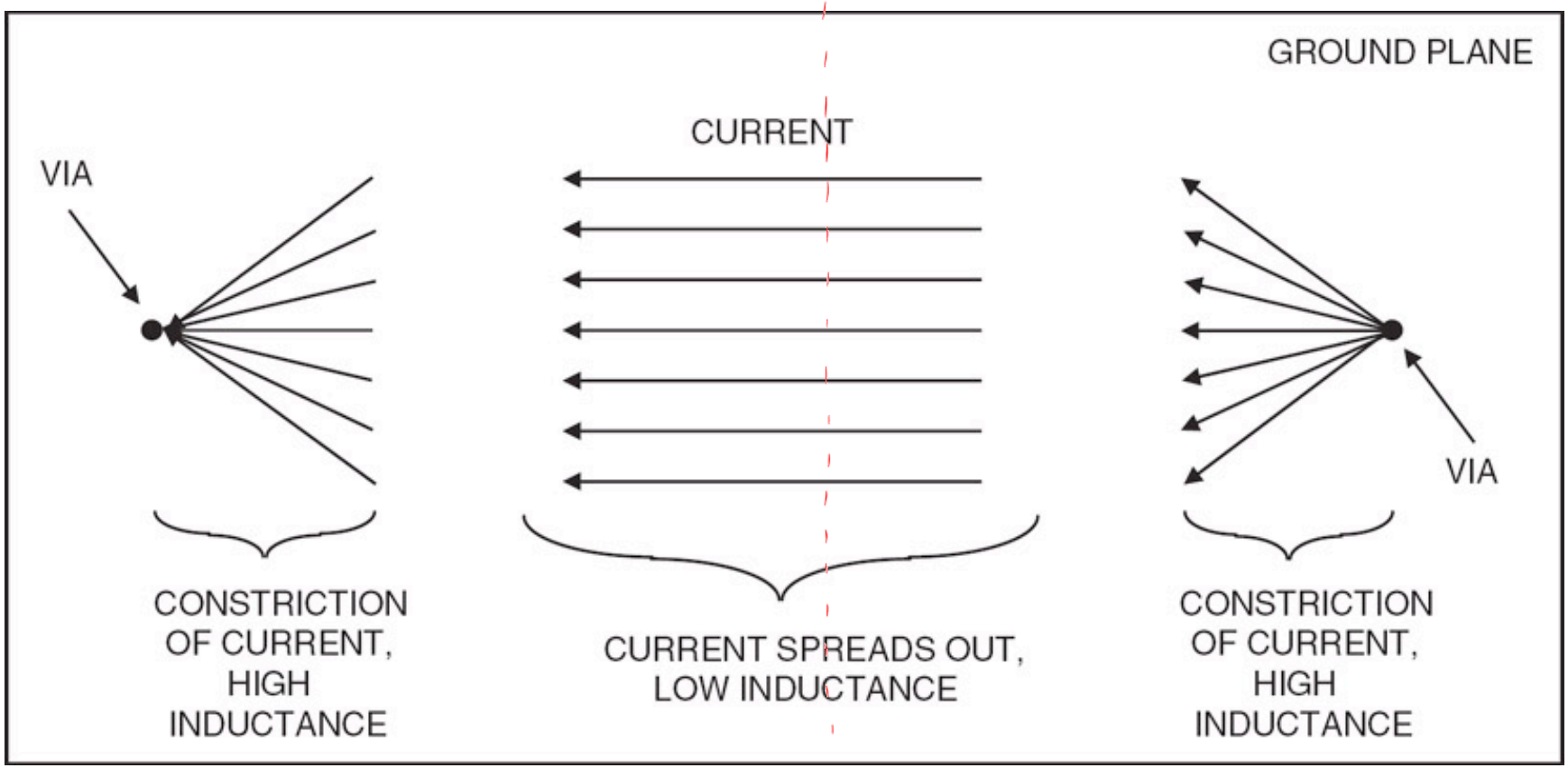
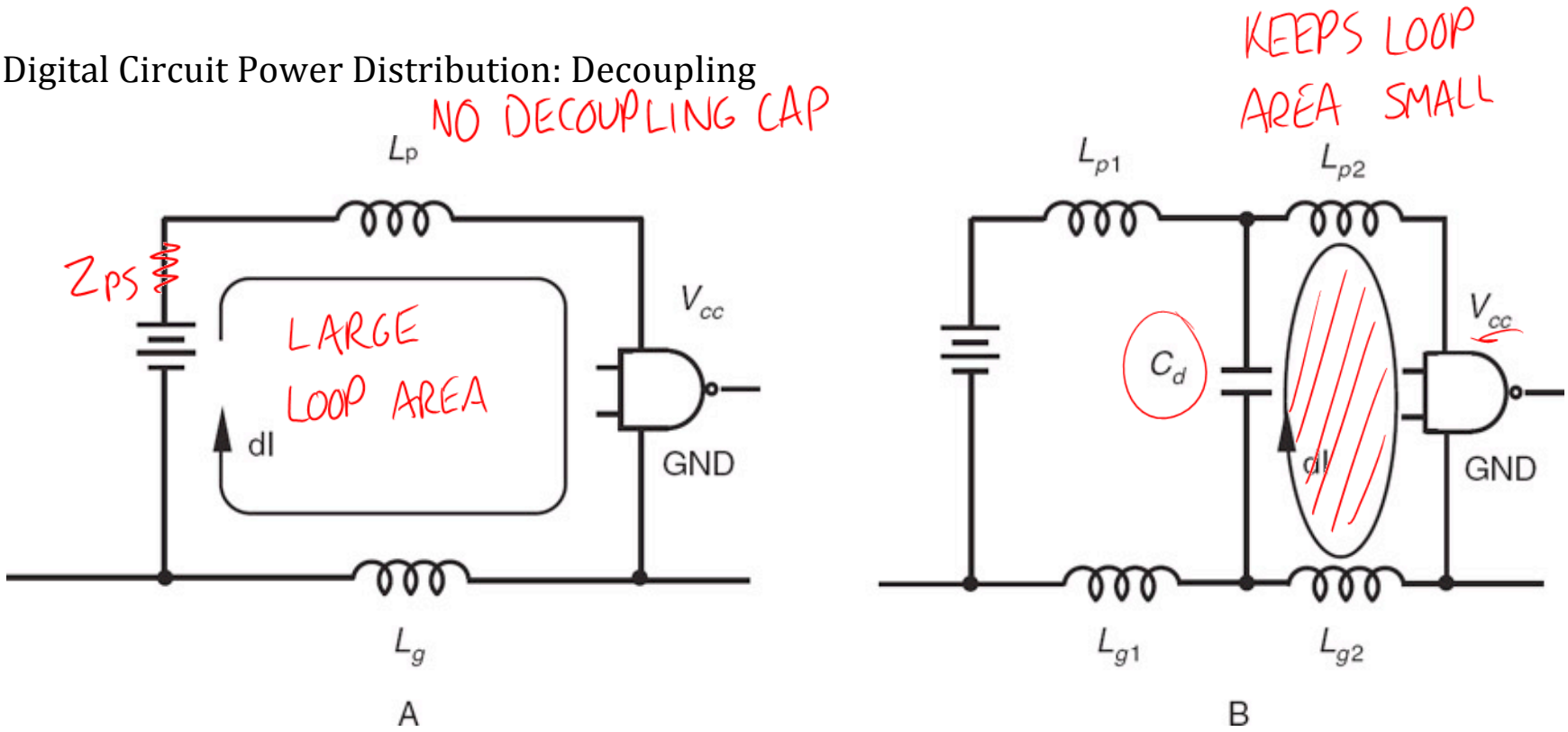


Figure 10-27: Representation of the ground plane current under a microstrip trace

USE MULTIPLE VIAS IF POSSIBLE LOWER TOTAL Z

Digital Circuit Power Distribution: Decoupling



1. Reduce the effect of one integrated circuit (IC) upon another (inter-IC coupling).
2. Provide a low impedance between power and ground, so that the IC operates as intended by its designers (intra-IC coupling).[*]

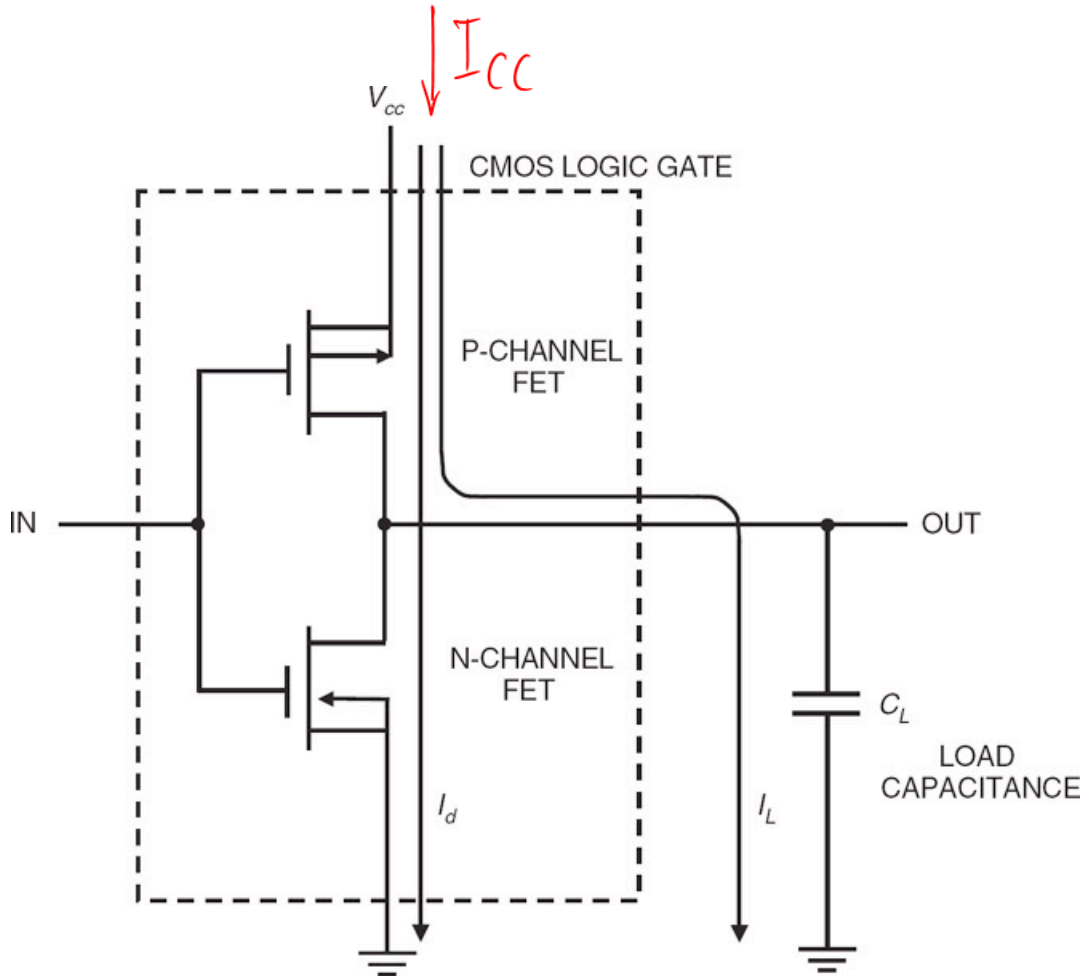


Figure 11-2: Transient currents produced when a CMOS logic gate switches

$\frac{1}{\pi t_r}$

Figure 11-3: Isosceles triangular wave

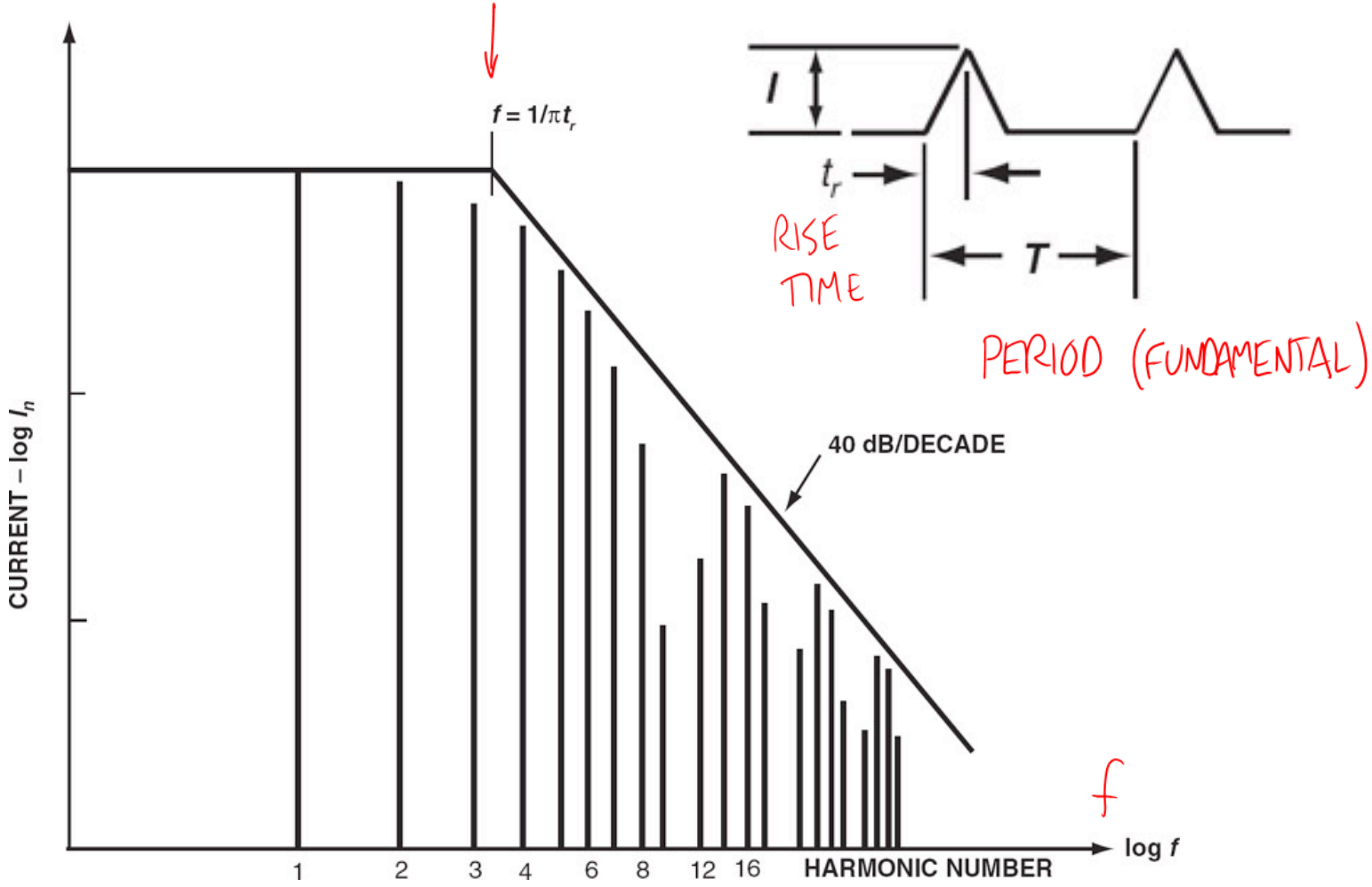
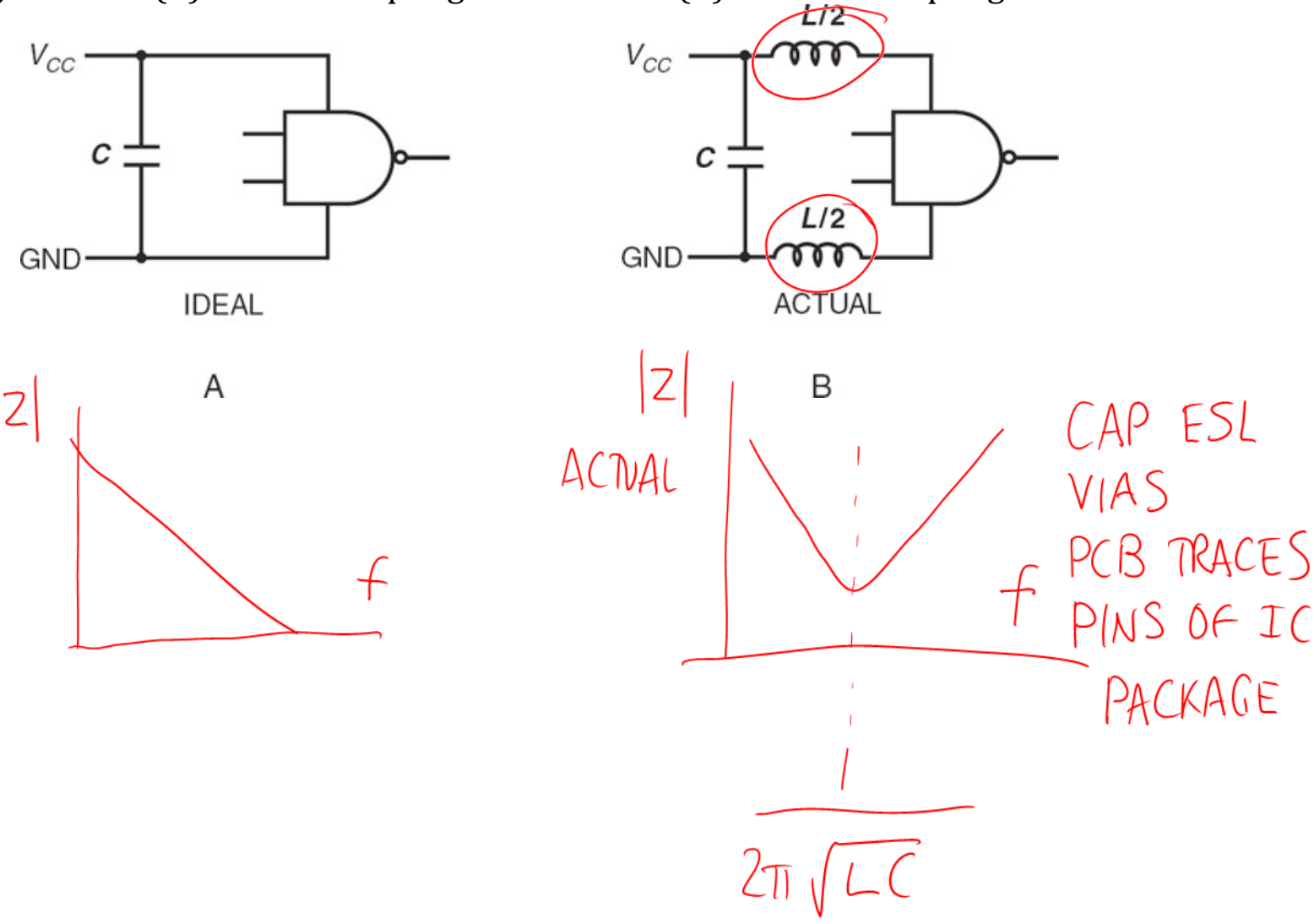


Figure 11-4: Envelope of Fourier spectrum of an isosceles triangular wave

FREQ RANGE FOR WHICH $|Z_{DECOUPLING}|$ NEEDS TO BE LOW

Figure 11-6: (*A*) Ideal decoupling network and (*B*) actual decoupling network



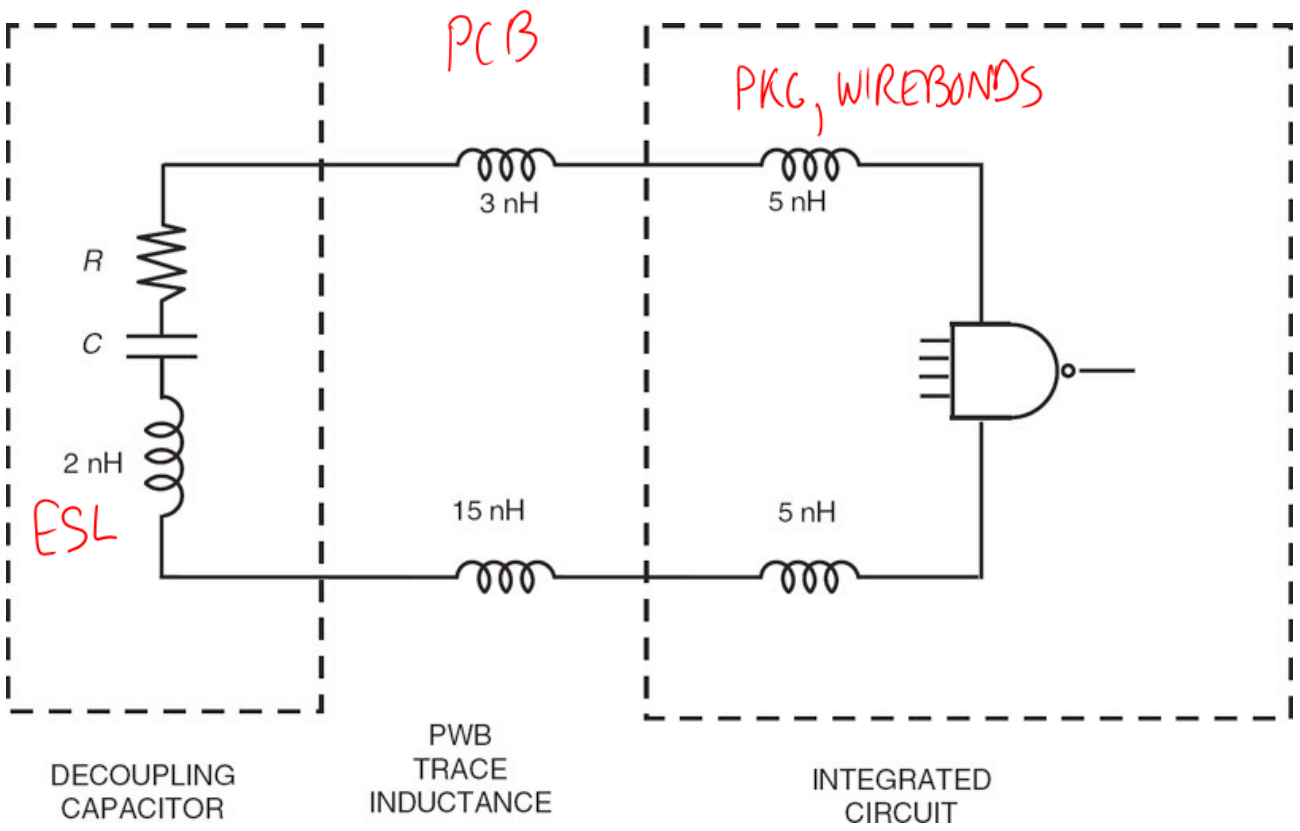


Figure 11-7: Equivalent circuit for decoupling capacitor connected to an integrated circuit, for a DIP package with power and ground on diagonally opposite pins of the IC

30 nH IN LOOP!

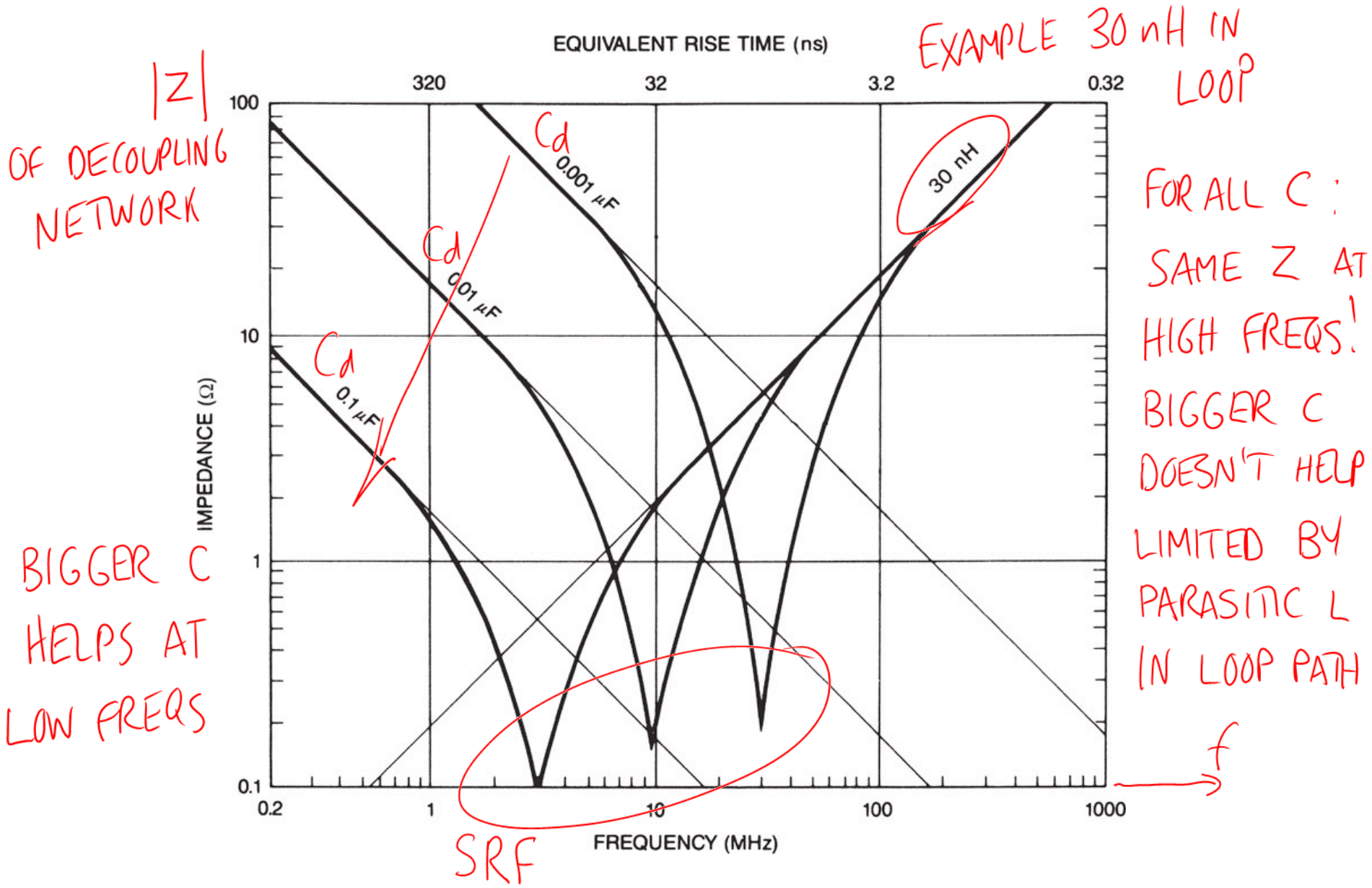


Figure 11-8: Impedance of different value decoupling capacitors in series with 30 nH of inductance

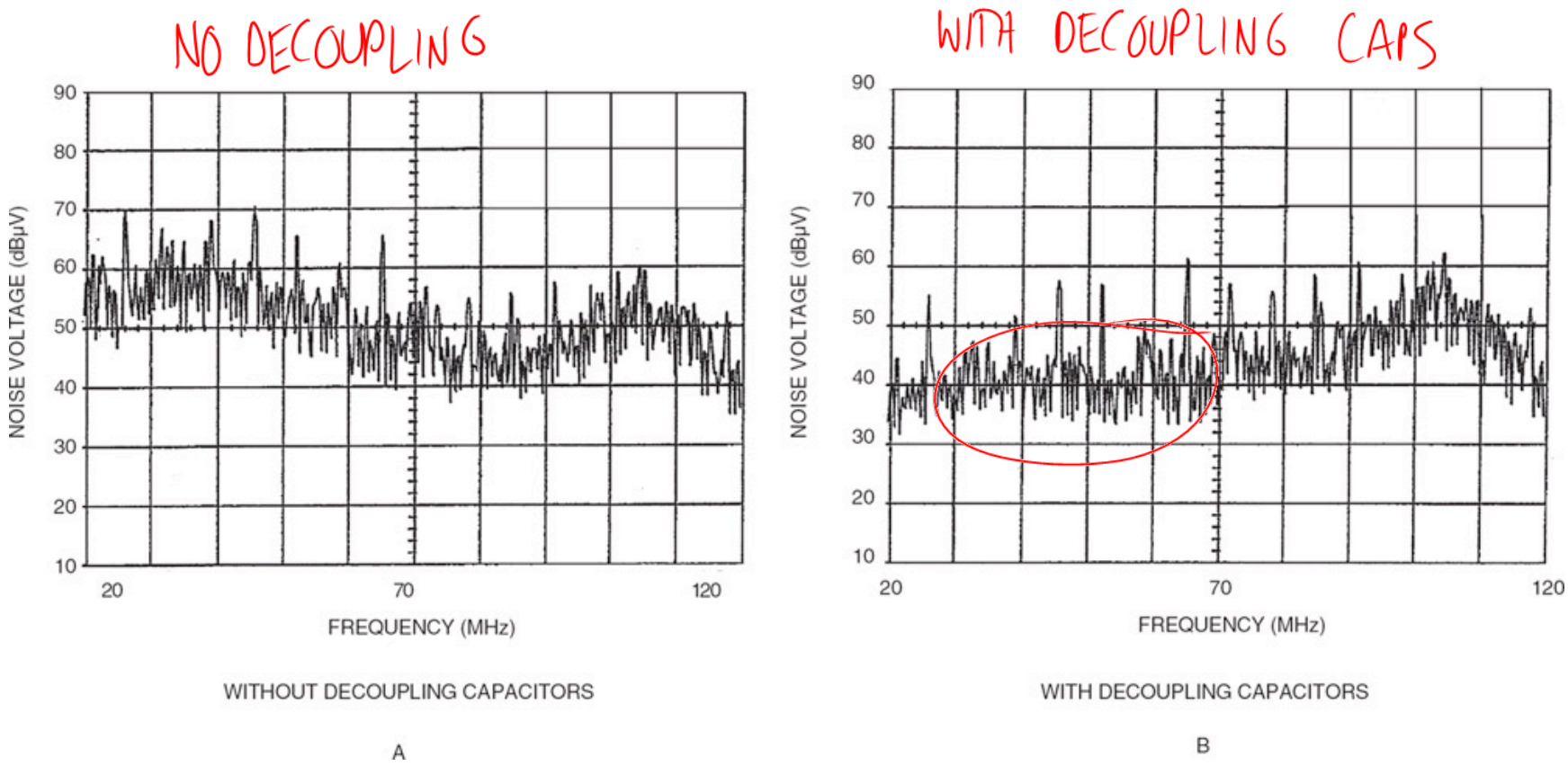


Figure 11-9: Measured V_{cc}-to-ground noise voltage versus frequency for a printed circuit board with and without decoupling capacitors

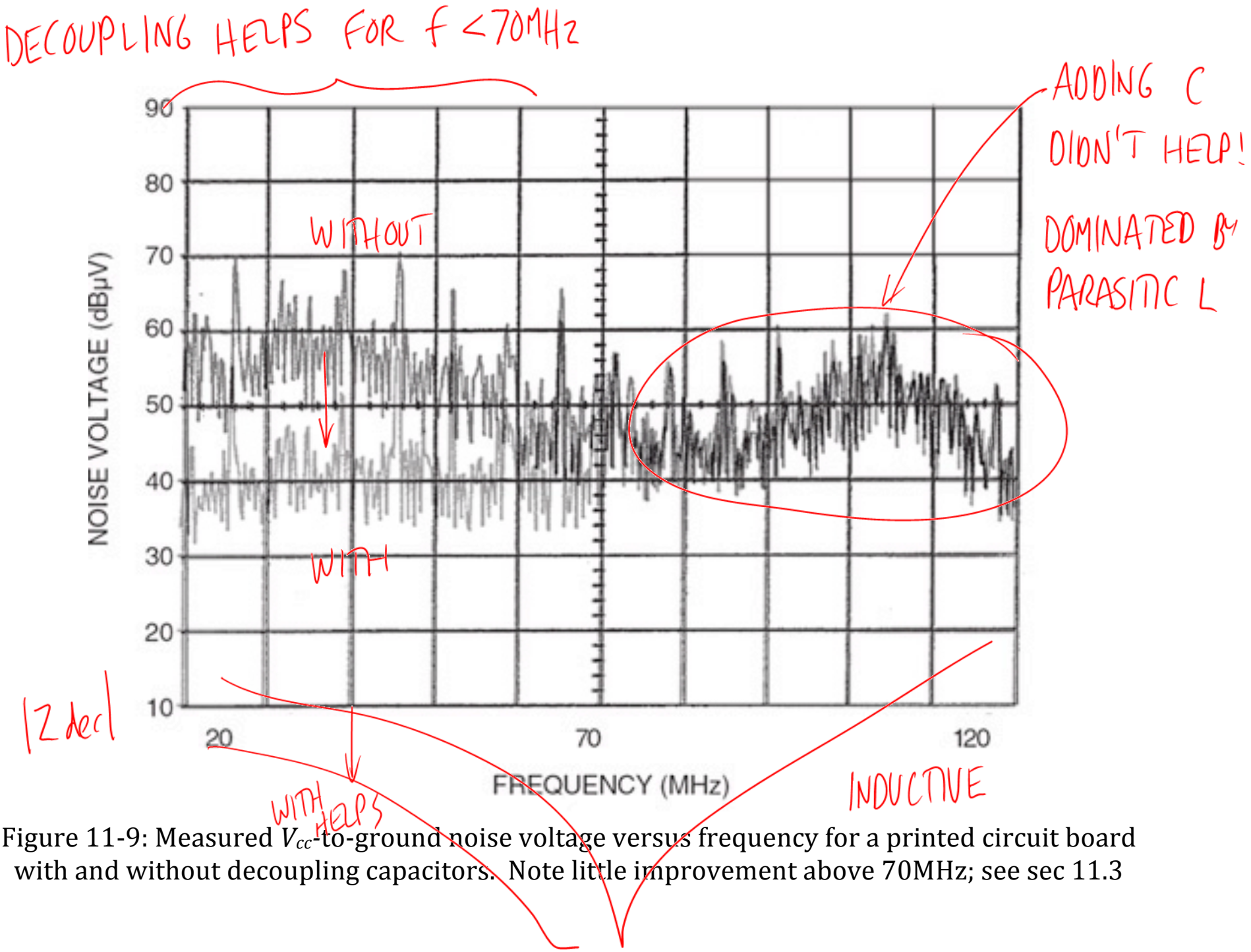
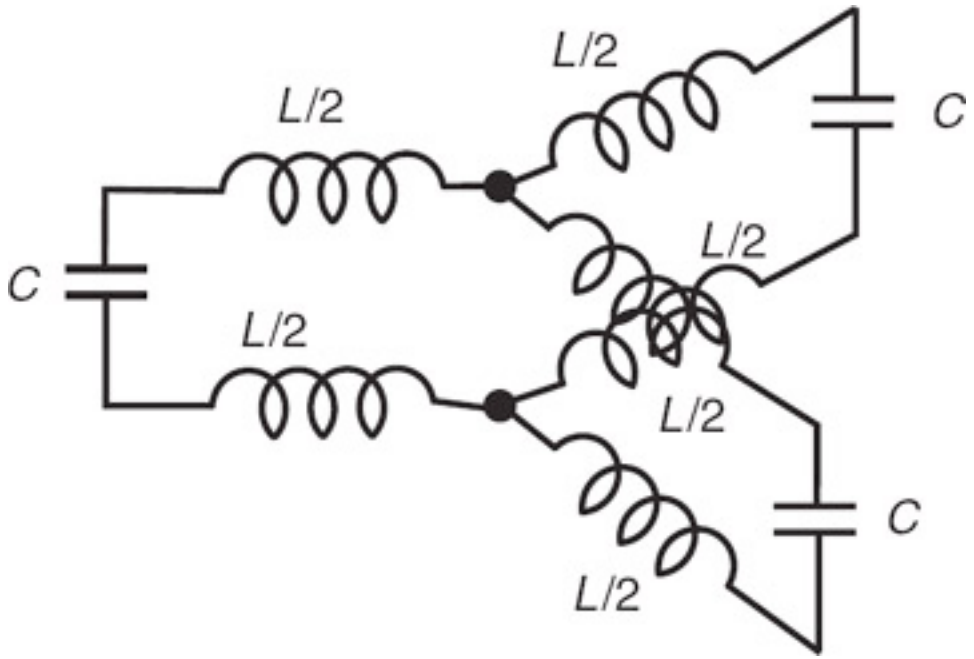


Figure 11-9: Measured V_{cc}-to-ground noise voltage versus frequency for a printed circuit board with and without decoupling capacitors. Note little improvement above 70MHz; see sec 11.3

DECOUPLING CAPS

C_1, C_2, C_3



The requirements for effectively paralleling multiple *L–C* networks are as follows:

1. Make all the capacitors the same value; this way they share the current equally.
2. Each capacitor must feed the IC through a different inductance than the others. Therefore, they cannot be located together, because of the mutual inductance that would occur. Spread them out.

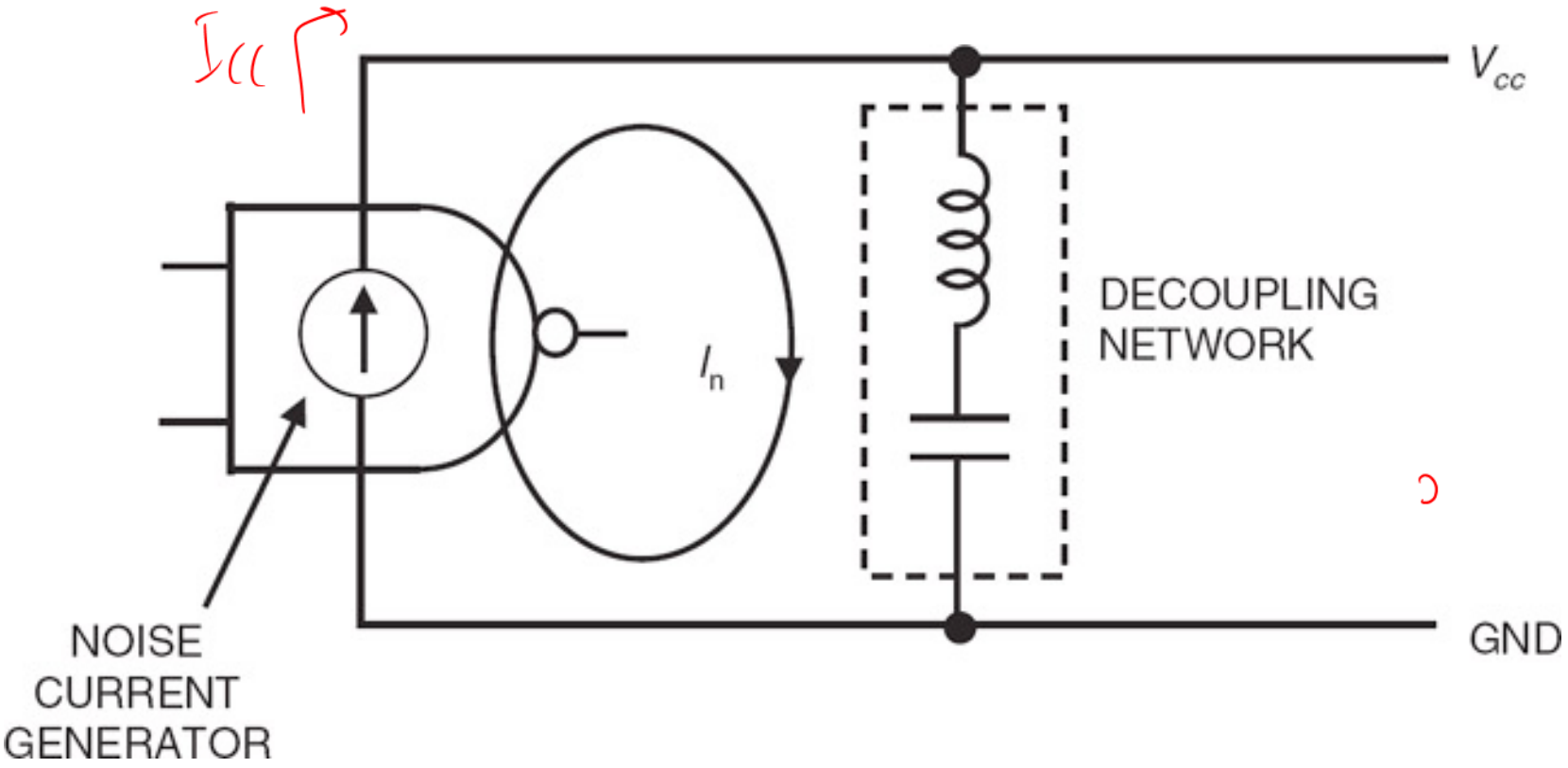


Figure 11-11: The IC as a noise current generator

MODEL FOR I_{CC}

ANALYSIS MODEL: IMPEDANCE OF DECOUPLING NETWORK

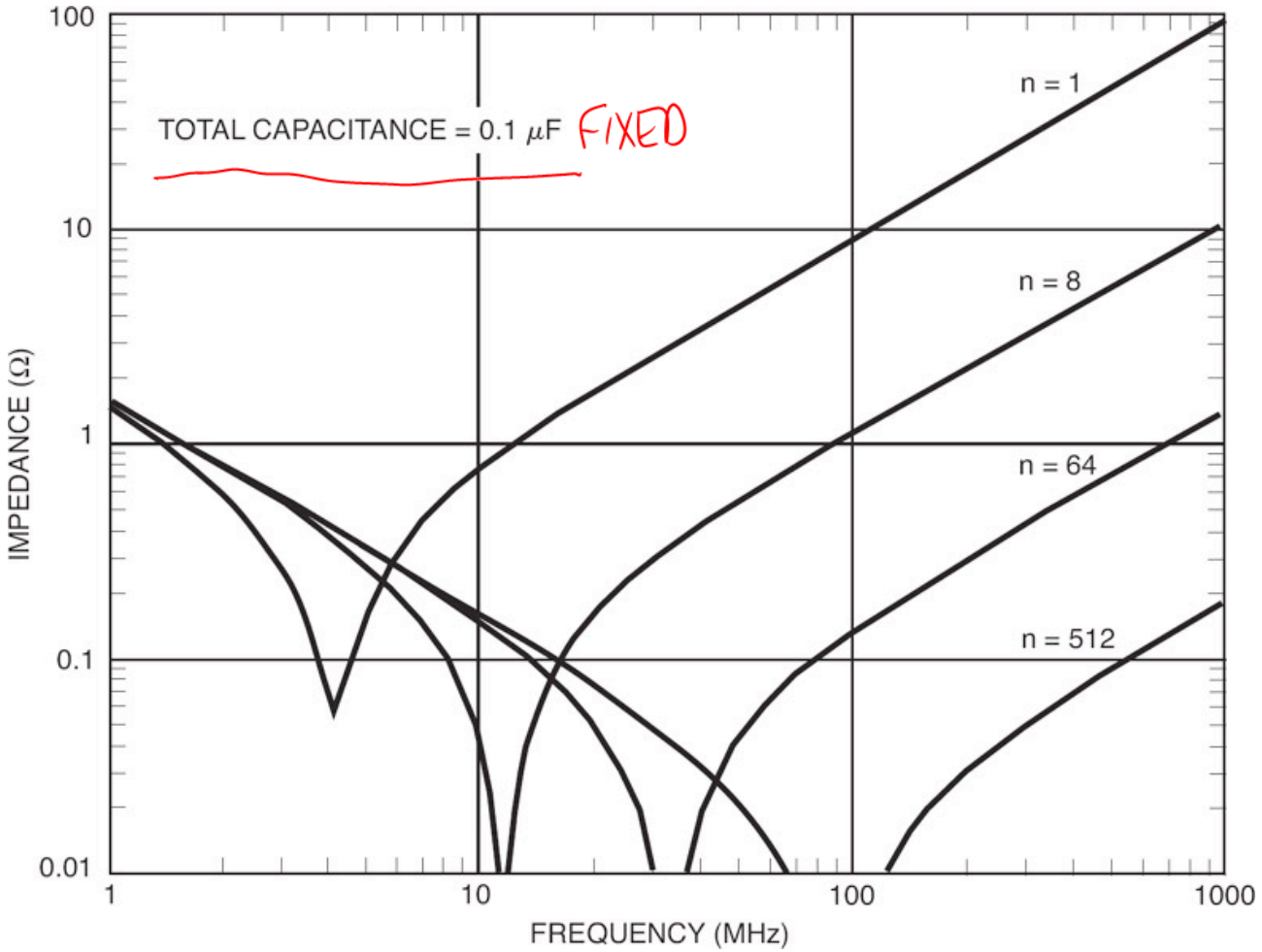
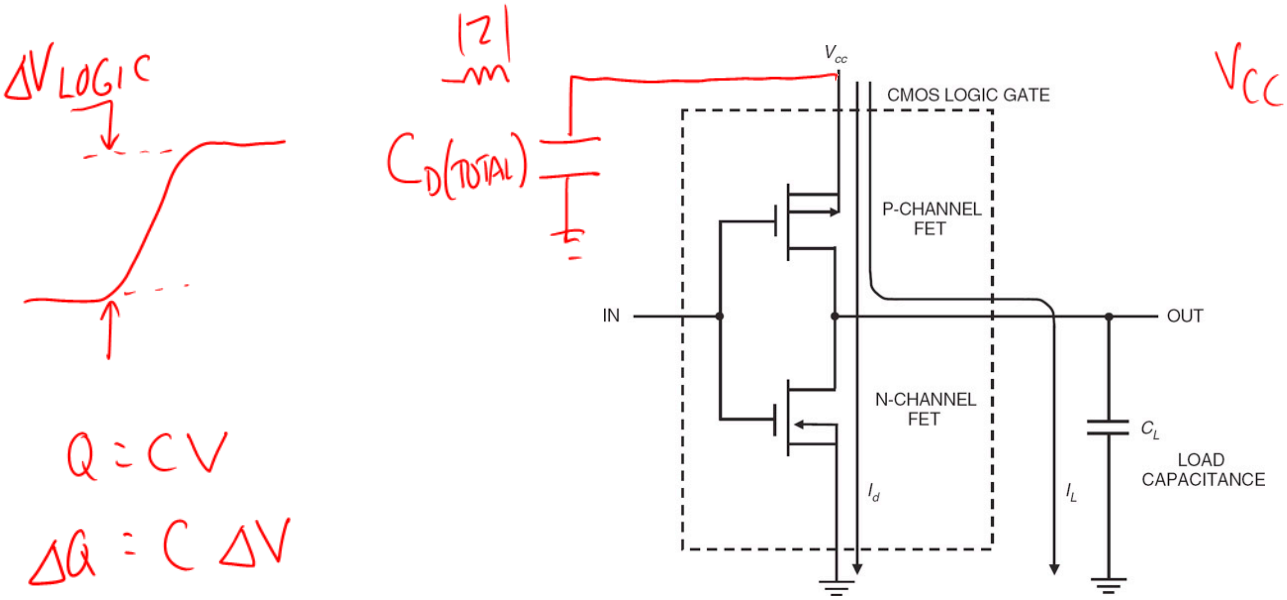


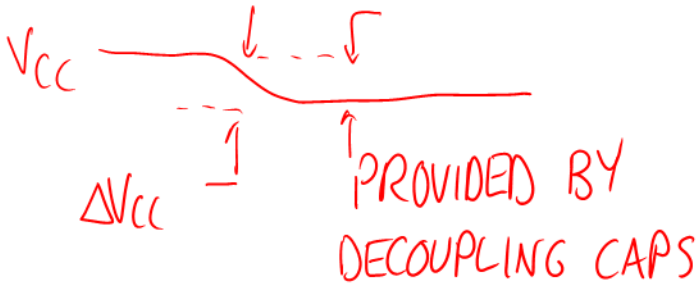
Figure 11-12 is a plot of the impedance versus frequency for various numbers (1, 8, 64, 512) of identical *L*–*C* networks in parallel. In all cases, the *total* capacitance equals 0.1 μF and the inductance in series with each capacitor is 15 nH.

Decoupling capacitor strategy

What is ΔQ required by load?

How much supply voltage ΔV_{CC} can circuit tolerate?

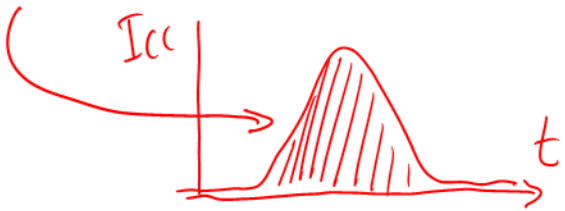




$Q = CV$

$\Delta Q = C \Delta V$

$\Delta Q = C_{L(TOTAL)} \Delta V_{LOGIC}$



$\Delta Q = C_{D(TOTAL)} \Delta V_{CC}$

EQUATE BY CHARGE CONSERVATION

$C_{L(TOTAL)} \Delta V_{LOGIC} = C_{D(TOTAL)} \Delta V_{CC}$

$C_{D(TOTAL)} = C_{L(TOTAL)} \frac{\Delta V_{LOGIC}}{\Delta V_{CC}}$

$C_{L(TOTAL)}$: TOTAL LOAD CAP

$\frac{\Delta V_{LOGIC}}{\Delta V_{CC}}$: SWING / CHANGE IN SUPPLY

TO MINIMIZE L

AS MANY SMALL, LOW ESL CAPS AS POSSIBLE DISTRIBUTED OVER PCB

(ALSO HELP FROM DISTRIBUTED PCB LAYER CAP)

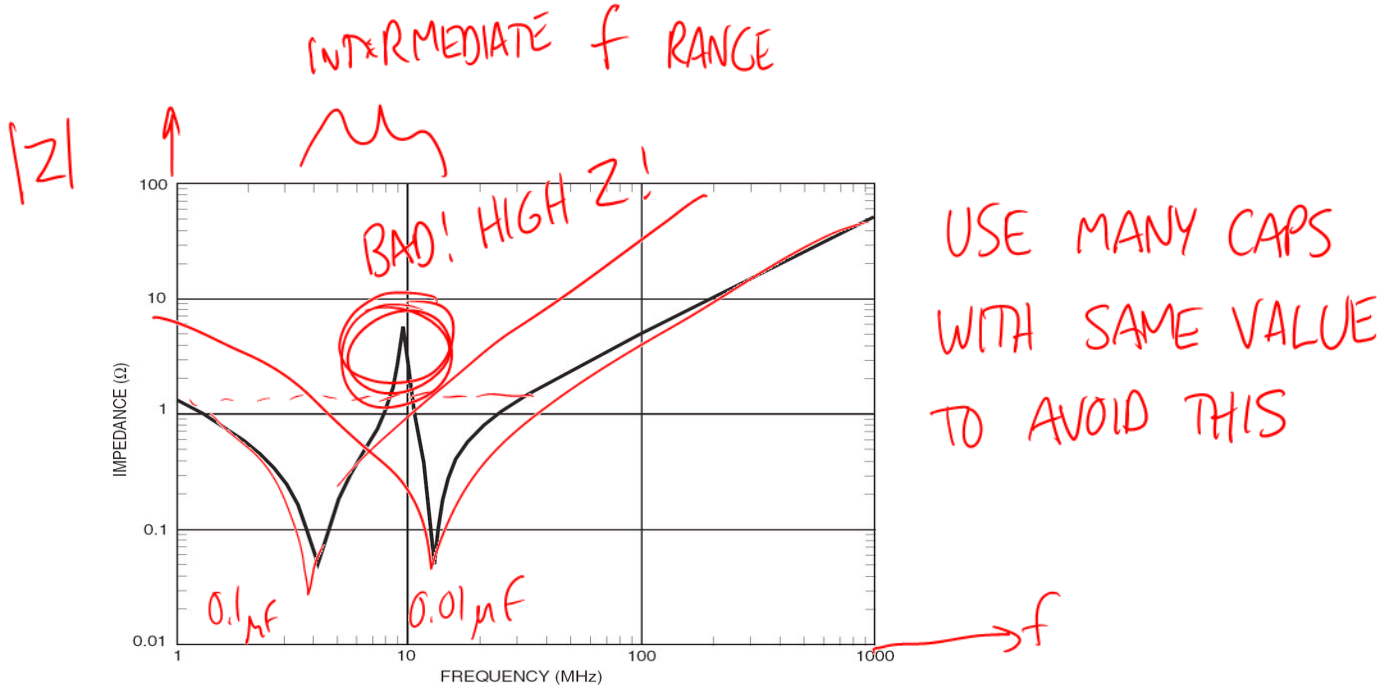


Figure 11-14: Impedance versus frequency for a decoupling network consisting of a 0.1 and a 0.01-μF capacitor, both in series with 15 nH of inductance

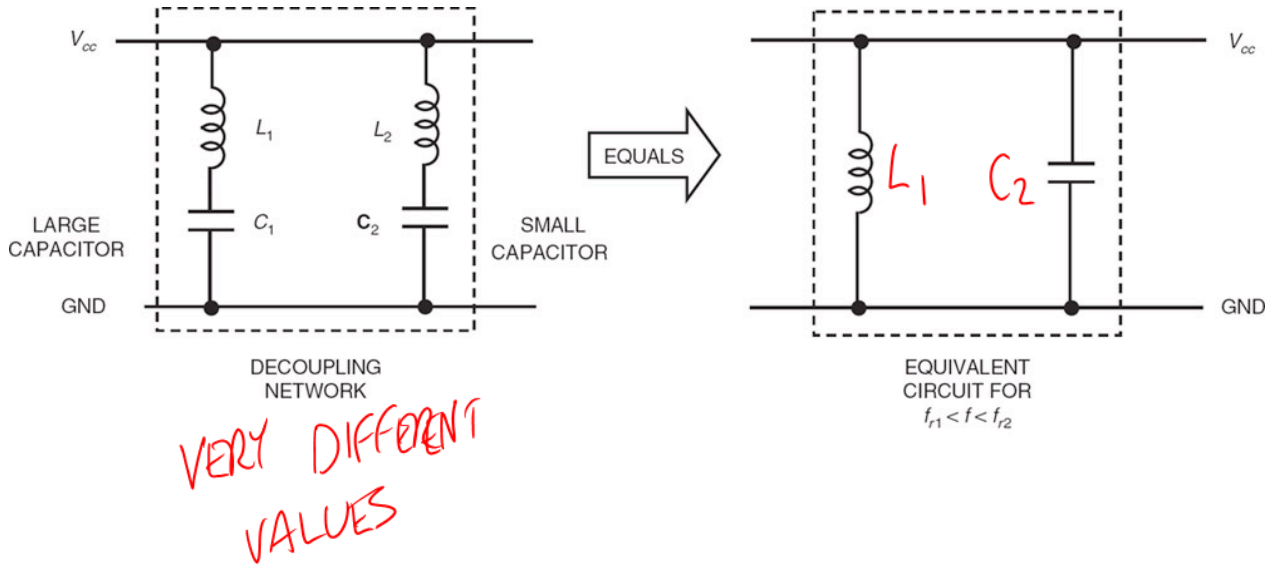
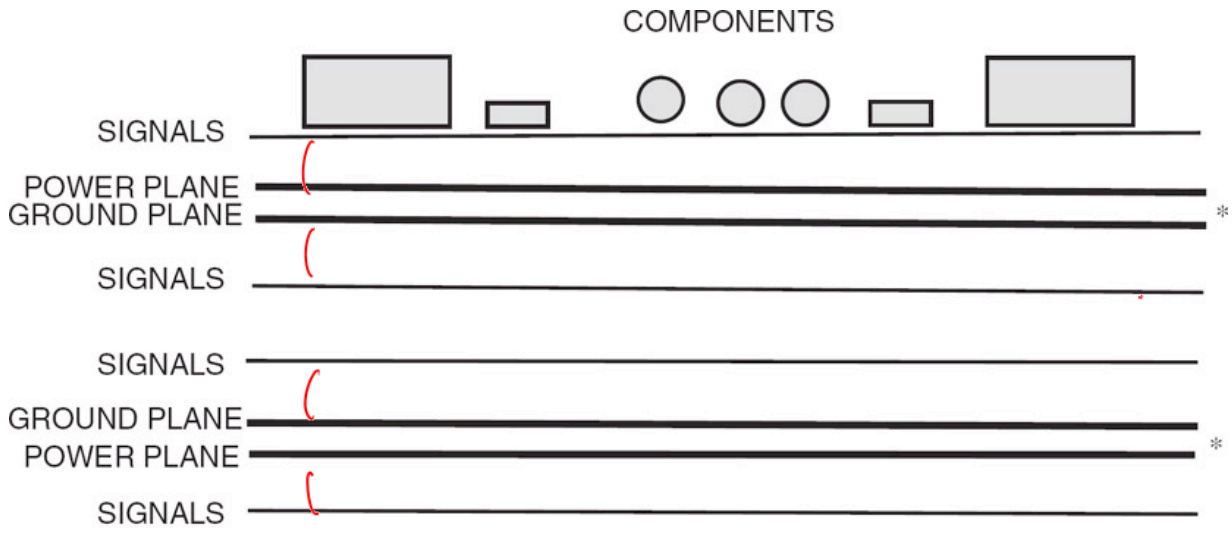


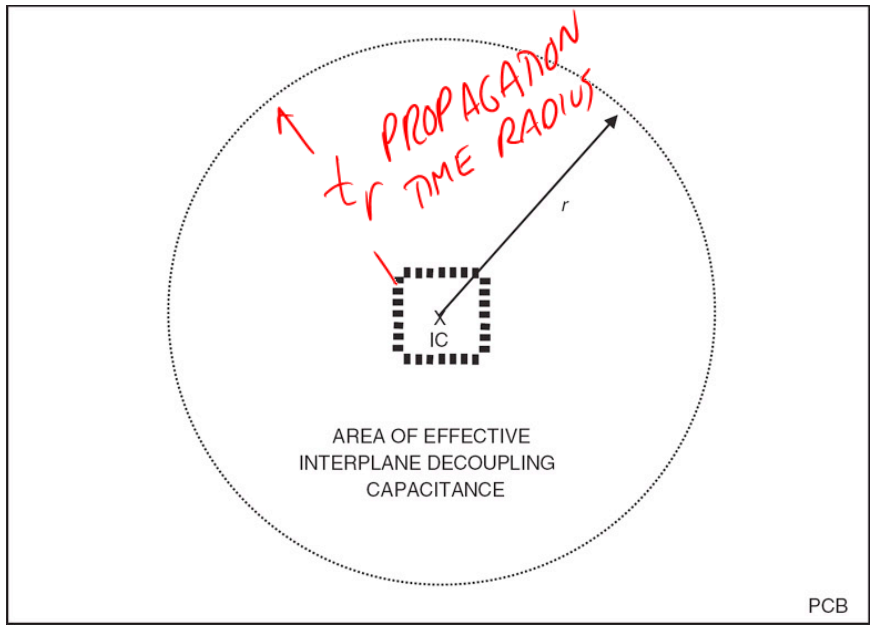
Figure 11-15: (*A*) Decoupling network with two different value capacitors, and (*B*) the equivalent circuit of *A* for a frequency *f* where $f_{r1} < f < f_{r2}$

Figure 11-19: Stackup of a typical embedded capacitance printed circuit board



DISTRIBUTED CAPACITANCE INHERENTLY LOW ESL, ESR

ANOTHER NICE FEATURE: EVERY SIGNAL PLANE HAS A REFERENCE PLANE (GND OR PWR) ADJACENT



The velocity of propagation of electromagnetic energy in a dielectric was given in Eq. 5-14 and is repeated here:

$$v = \frac{c}{\sqrt{\varepsilon_r}}, \qquad (11\text{-}9)$$

where c is the speed of light (12 in/ns) and ε_r is the relative dielectric constant of the material.

The radius of the effective capacitance area is equal to

$$r = vt = \frac{12t}{\sqrt{\varepsilon_r}}, \qquad (11\text{-}10)$$

where r is the radius in inches, t is the time required to move the charge in nanoseconds, and ε_r is the relative dielectric constant of the material. If we want to move charge on an FR-4 epoxy-glass PCB ($\varepsilon_r = 4.5$) in 0.5 ns, then r would be equal to approximately 3 in.

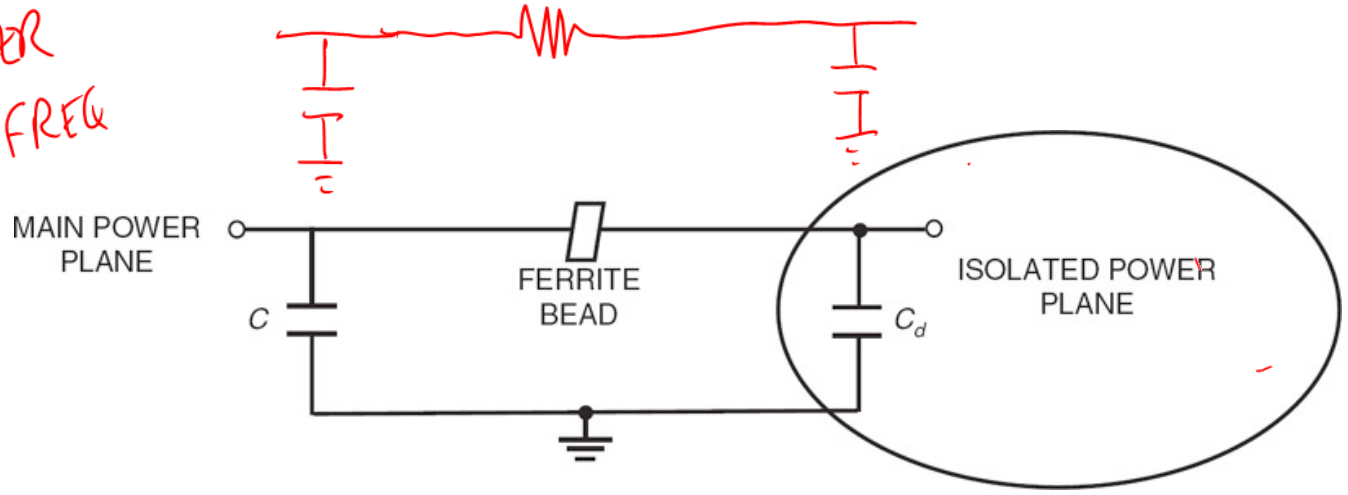


Figure 11-21: Filter used to feed power to an isolated power plane

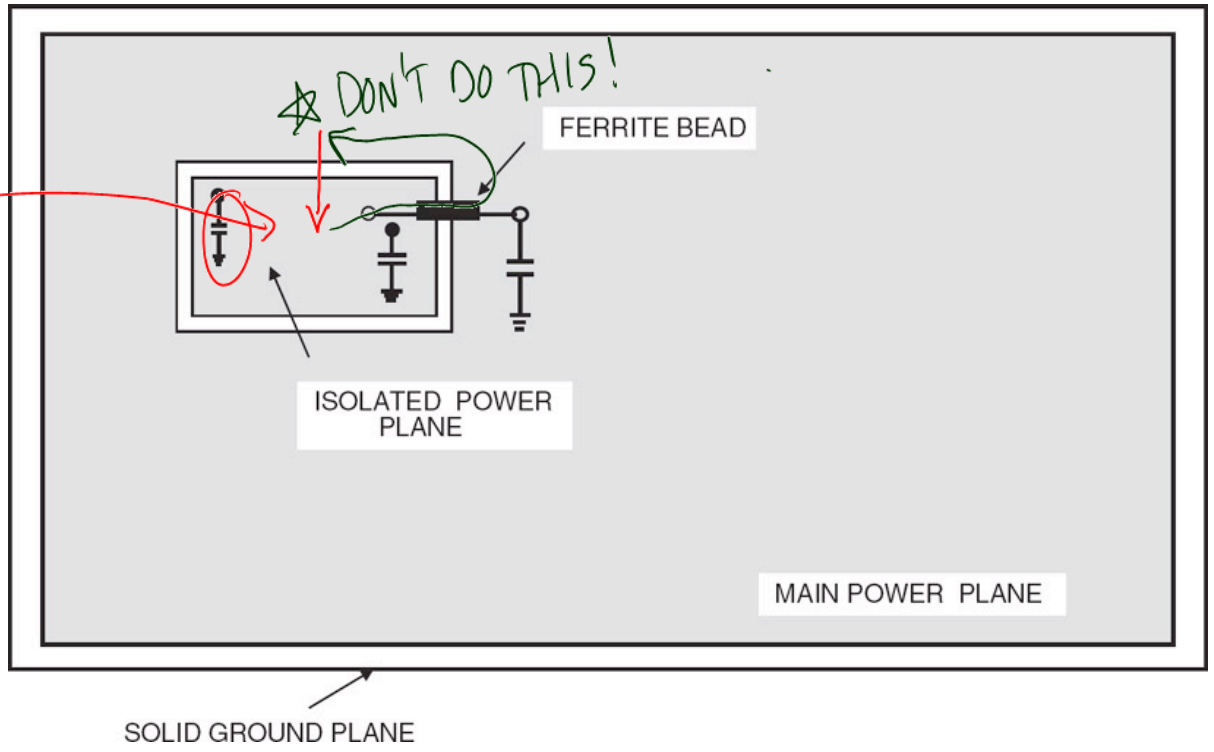


Figure 11-22: Example of an isolated power plane

Effect of decoupling on Radiated Emissions

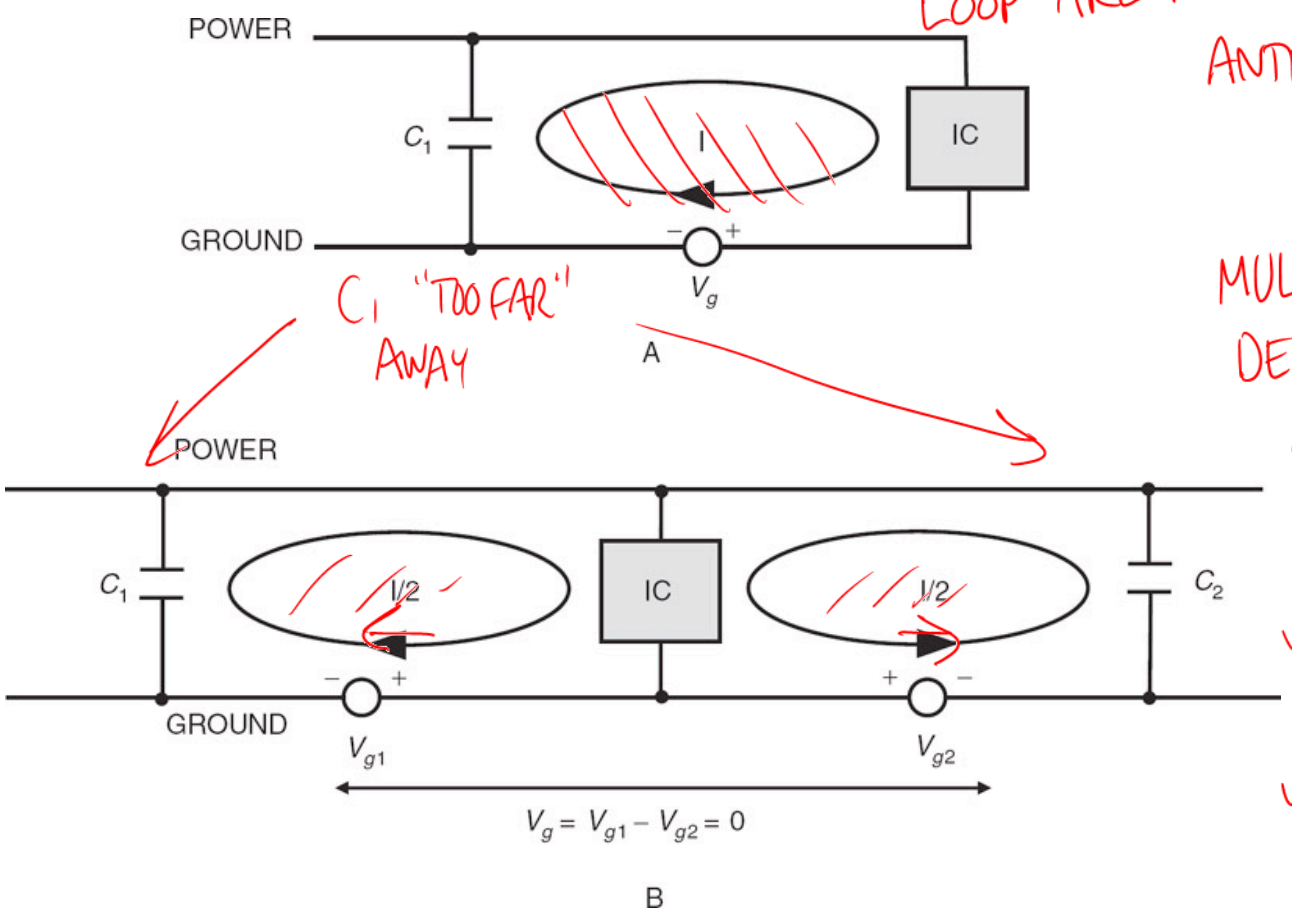


Figure 11-24: Current in the IC to decoupling capacitor loop, for the case of (A) one decoupling capacitor, and (B) two identical decoupling capacitors

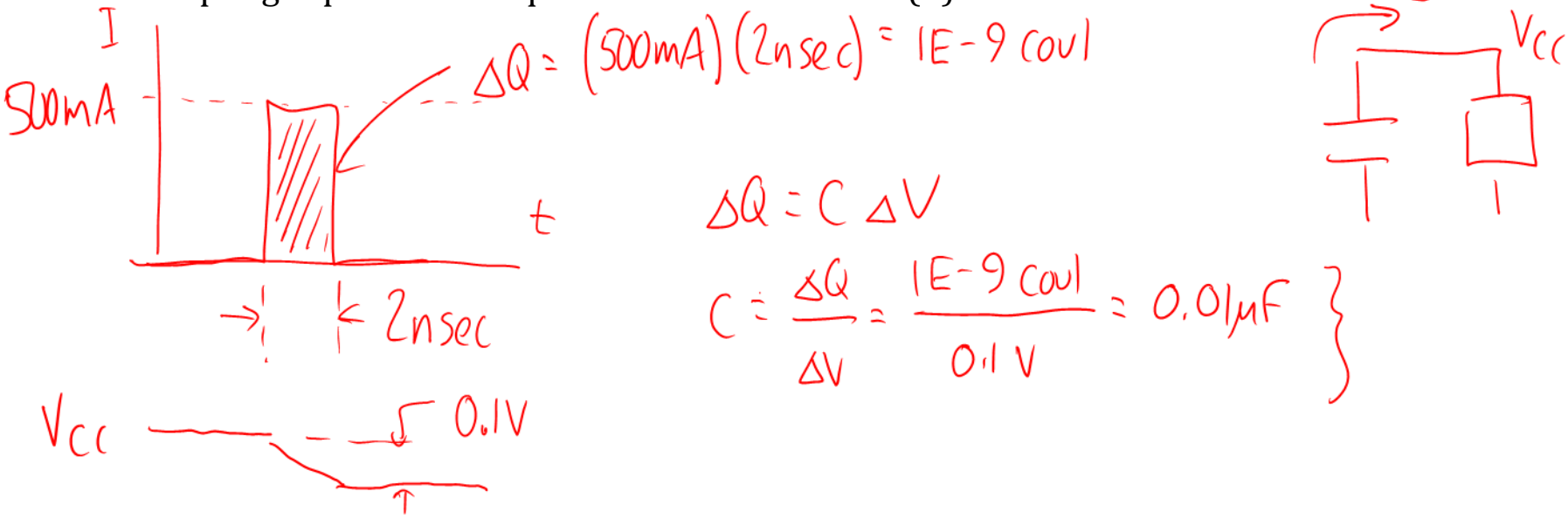
Decoupling Capacitor Value

For effective decoupling at low frequencies (below the decoupling network resonance), the total decoupling capacitance must satisfy the following two requirements:

(1) the total capacitance must be large enough to have an impedance below the target impedance at the lowest frequency of interest (see Section 11.4.5) and

(2) the total capacitance must be large enough to supply the transient current required by the IC when it switches, while keeping the supply voltage within the required tolerance. (SLIDE 1-148)

One Minute Quiz:
An IC requires a transient current of 500 mA for 2 ns. For proper operation it is necessary to limit the power supply voltage transient to less than 0.1 V. What is the total value of decoupling capacitance required to meet criterion (2)?



Decoupling Capacitor Type

Low-frequency effectiveness: value of capacitance
High-frequency performance: determined solely by how low the inductance can be driven.

Inductance is determined by how many capacitors are used and the inductance in series with each.

The internal inductance of a multilayer SMT capacitor is primarily determined by its package size.

A 1206 capacitor will have an inductance of about 1.2 nH, whereas an 0603 capacitor will have an inductance of about 0.6 nH.

Use the smallest package size practical for the application, and then use the largest value capacitor readily available in that package size. Choosing a smaller value capacitor provides no improvement in the high-frequency performance, but it will degrade the low-frequency effectiveness.

Decoupling Capacitor Placement

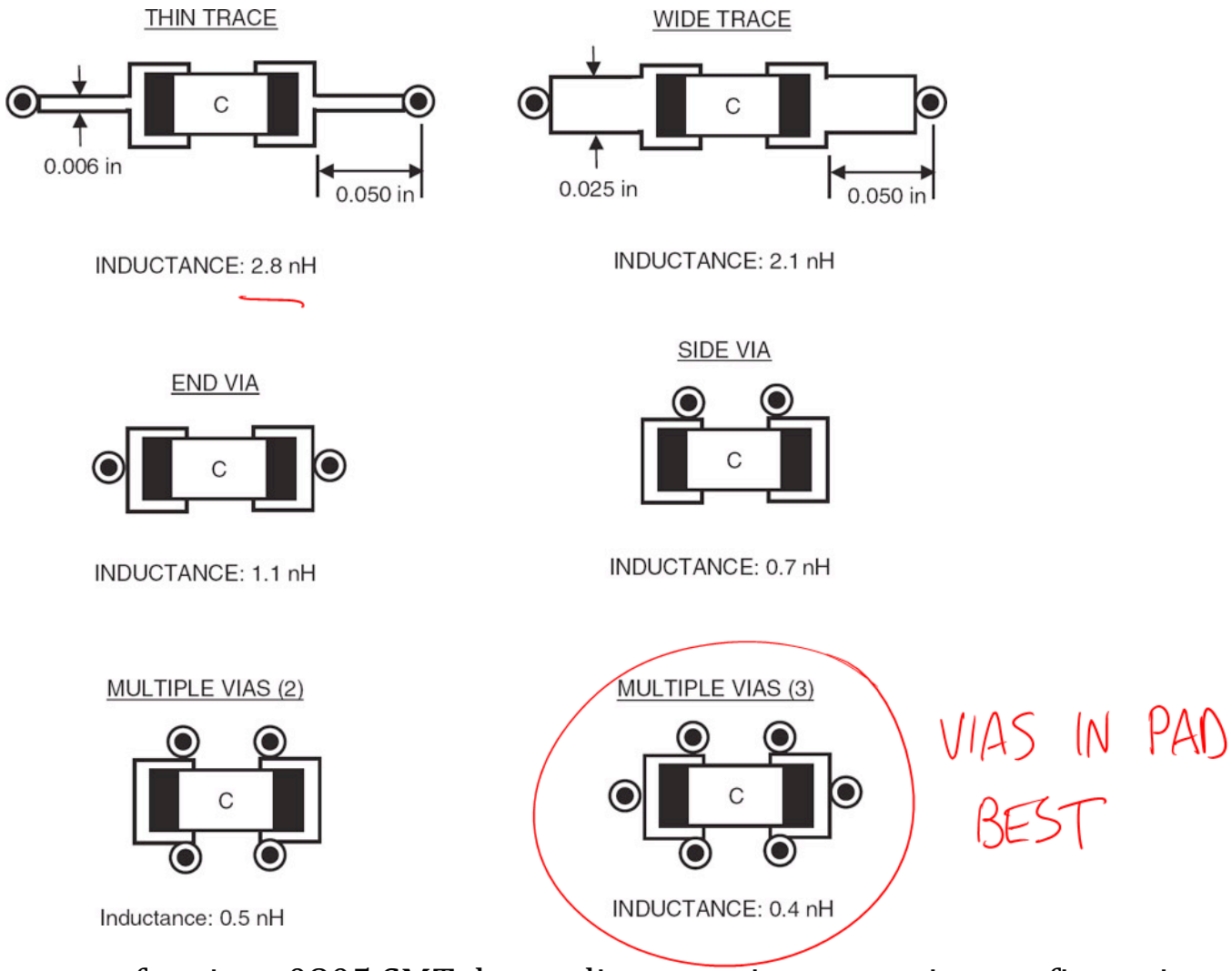


Figure 11-25: Inductance of various 0805 SMT decoupling capacitor mounting configurations

Bulk Decoupling Capacitors

The value of the bulk capacitor is not critical, but it should be greater than the sum of all the values of the IC decoupling capacitors that it serves.
One bulk decoupling capacitor should be located where power comes onto the board. Other bulk capacitors should be located strategically around the board.
It is better to err on the side of too much bulk decoupling capacitance than on the side of too little.

The bulk decoupling capacitors will typically have values in the 5- to 100-μF range (10 μF being a typical value) and should have a small equivalent series inductance.
Multilayer ceramic capacitors are becoming more common in this application.
In the past, tantalum electrolytic capacitors were common.
Aluminum electrolytic capacitors have inductances an order of magnitude or more higher than tantalum and should not be used.

Power Entry Filters

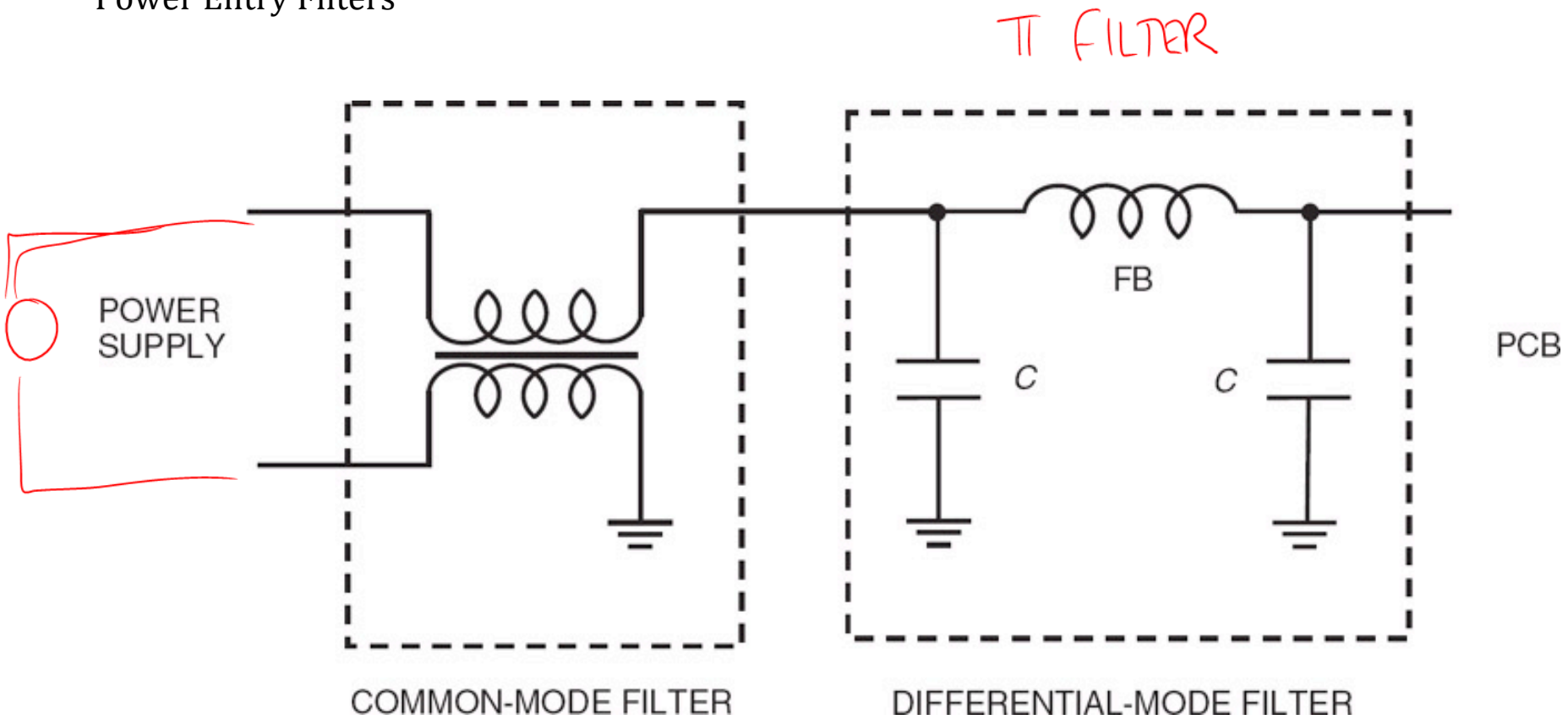


Figure 11-26: A typical power entry filter

Typical values for the filter elements are 0.1 to 0.01 μF for the capacitors and a ferrite bead whose impedance is between 50 and 100 Ω across the frequency range of interest. In this application, it is important to avoid saturation of the ferrite bead by the dc current. If an inductor is used, then typical values would be from 0.5 to 5 μH.

Summary: Digital Power Distribution

- Decoupling capacitors are needed to supply, through a low-inductance path, some or all of the transient power supply current required when an IC logic gate switches.
- Decoupling capacitors are needed to short out, or at least reduce, the noise injected back into the power ground system.
- Decoupling is not the process of placing a capacitor adjacent to an IC to supply the transient switching current; rather it is the process of placing an *L–C* network adjacent to the IC to supply the transient switching current.
- The value of the decoupling capacitor(s) is important for the low-frequency decoupling effectiveness.
- The value of the decoupling capacitor(s) is not important at high frequencies. At high frequencies, the most important criteria is to reduce the inductance in series with the decoupling capacitors.
- Effective high-frequency decoupling requires the use of a large number of capacitors.
- In most cases, the use of single value decoupling capacitors perform better than when multiple value capacitors are used.
- For *optimum* high-frequency decoupling, discrete capacitors should not be used at all; rather, a distributed capacitor PCB structure should be used.
- The number one rule of decoupling is to have the current flow through the smallest loop possible.

Summary: Day 1 Grounding and Power

- Ground and power are the among first things you should think about when designing a high speed or high current or high accuracy system
- There are many techniques available to reduce interference to an acceptable level, and the earlier you think about them in the design process the more options are available and the lower will be the cost of implementation
- Noise and interference can be understood in terms of basic system concepts such as the source – channel transfer function – receptor model and use of circuit elements (capacitance and inductance) to represent electric field and magnetic field coupling
- "Ground" means different things to different people. Be clear on the use of ground for safety, voltage reference, current return, shielding, etc. in different applications
- Current has to flow in a loop and wants to return by the lowest impedance path. Always give the current the smallest loop area return path possible and watch out for common impedance coupling so that high current return paths do not affect low level signal voltage reference ground paths

$V_g = I_g Z_g$

- Power supply distribution and decoupling needs to be intentionally designed
- Passive elements used in distribution and decoupling are nonideal, and often it is the parasitic nonidealities that end up setting critical performance limitations
- Even digital is analog and often digital traces on a PCB need to be designed as analog transmission lines to maintain acceptable digital signal integrity