To avoid device damage, engineers must minimize backdrive currents and the length of time a circuit must endure them.

The BACKSTORY on BACKDRIVING

BY TONY SUTO, TERADYNE, AND JOHN MCNEILL, WORCESTER POLYTECHNIC INSTITUTE

Since the introduction of in-circuit test (ICT) more than three decades ago, manufacturers of printed circuit boards (PCBs) have debated whether overdriving devices during test can damage them. Research on the subject surfaced out of Bell Laboratories in the early 1980s (Ref. 1). Its conclusions were uncertain, at best.

The Bell research involved CMOS parts featuring the large geometries, thick oxides, and 5-V power supplies of that era's state of the art. Since then, the battle to reduce heat dissipation and power consumption in a world of ever-higher speeds and shrinking circuit features has forced voltage levels dramatically lower, until today's V_{CC} barely tops 1 V.

Achieving higher device performance at lower supply voltages has required manufacturers to reduce gate-oxide thickness, yet thinner oxide makes a circuit more vulnerable to damage from electrical overstress (EOS).

Backdriving during in-circuit testing causes particular concern. Some circuits suffer damage from ESD when diodes are subjected to current levels that exceed manufacturers' specifications. More robust devices can guard against this damage, but they typically exhibit a higher shunt capacitance and therefore cannot achieve the switching speeds necessary for many applications.

Damage can take several forms. Reverse-biased junctions that are subjected to ESD can avalanche and fail. More often, forward-biased diodes fail because the high current leads to high temperatures that cause damage. Metallization layers that connect to the protection circuits can also succumb to Joule heating.

Devices may not malfunction immediately. Instead, parts with latent defects may pass all normal

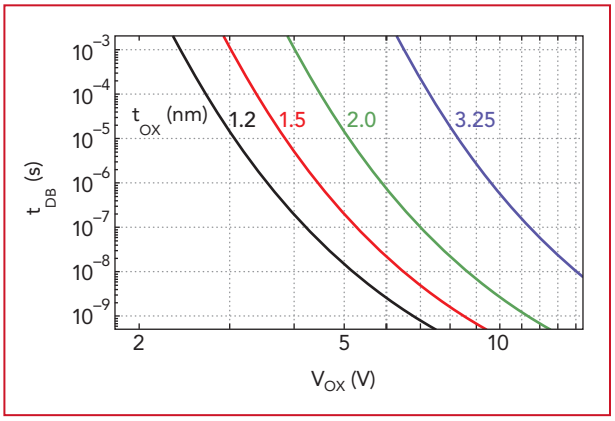

FIGURE 1. This graph shows mean time to dielectric breakdown (t_{DB}) as a function of voltage stress (V_{OX}) across the gate oxide for various gate oxide thicknesses (t_{OX}).

production tests, only to deteriorate over time and fail at the worst possible moment—in the hands of the customer. To assure such failures don't occur, you need to understand the relevant failure mechanisms and how you can safely apply in-circuit test techniques.

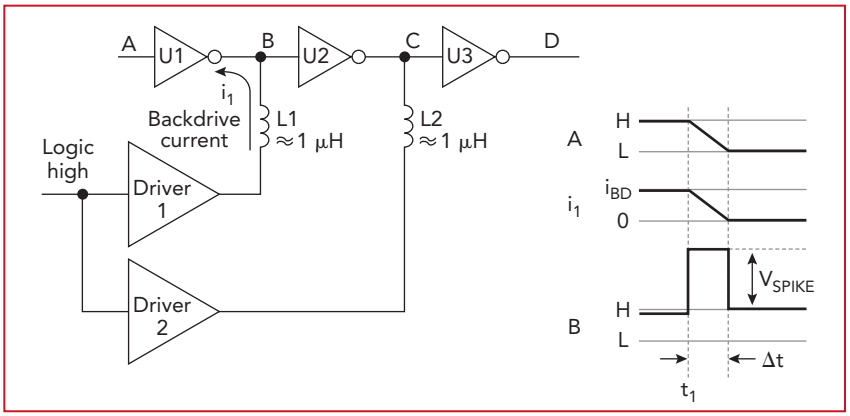

FIGURE 2. This example shows the backdriving of device U1 necessary to test device U3.

CMOS latchup and TDDB

CMOS latchup occurs when I/O voltages exceed the power-supply voltage or go below the nominal IC ground by more than about 700 mV. Such conditions can turn on the parasitic bipolar transistors Q_{npn} and Q_{pnp} in CMOS processes, heating up the bond wires as well as the rest of the die to temperatures that can exceed 200°C. More common on 12-V CMOS devices made two decades ago, this type of damage still presents a significant problem in submicron-geometry devices.

Time-dependent dielectric breakdown (TDDB) begins with an overvoltage condition that exhibits either a large amplitude for a short duration or a smaller amplitude for a longer duration. Resulting hot carriers accelerate to velocities high enough to enter the gate-oxide layer and create electron-hole pairs. The pairs, in turn, trap charges in the transistor's dielectric layer. These traps attract other trap sites and accumulate to form a silicon filament that eventually shorts a gate to a channel. As with diode damage caused by ESD, latent versions of these defects can escape all electrical tests during production only to fail later on.

Researchers have proposed two models for predicting gate-oxide reliability as a function of electric field E. For high values of E, an anode-hole injection, or "1/E" model agrees fairly well with experimental results. A thermochemical—or "E"—model works better at low field levels.

The 1/E model predicts a mean time to breakdown of

$$t_{BD} = C_1 \exp(C_2/E_{OX})$$

In this equation, C_1 is a technology-dependent empirical time parameter that represents a best fit with available data. Its value in this case is 5.6×10^{-13} s. C_2—the field-acceleration parameter—equals $4.3 \times 10^{+8}$ V/cm. E_{OX} represents the electric field in the oxide, determined by

$$E_{OX} = V_{OX}/T_{OX}$$

where V_{OX} represents the voltage drop across the gate oxide caused by the applied voltage, and T_{OX} is the oxide thickness in centimeters. **Figure 1** graphs these parameters for various oxide thicknesses.

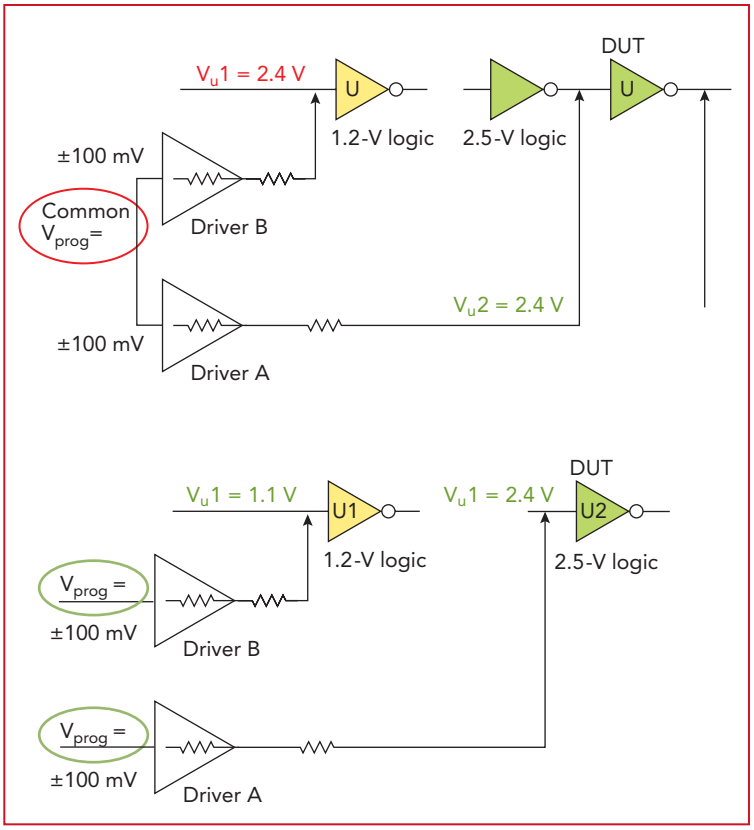

FIGURE 3. (a) A tester with a single voltage level for both Driver A and Driver B may not provide a safe environment for both devices. (b) In this tester design the two drivers can be programmed independently to minimize stress to the lower-voltage part.

Enter the in-circuit tester

An in-circuit tester must often force inputs to a logic state opposite to their "natural" states. This "backdriving" can induce currents of several hundred milliamps as well as overvoltage transients.

In **Figure 2**, U3 is the device under test. Its input at node C is forced by pin driver Driver 2. To ensure that Driver 2 sees a constant load and that the device produces a stable output, the tester prevents the U2 output from changing state during the test. To achieve this isolation, Driver 1

forces node B high. Since U1 remains free, Driver 1 does not see a constant load.

The current level (i_1) required to maintain the desired state at node B depends on the node A logic level. If node A is high, U1 tries to drive node B low. To maintain the high, Driver 1 must supply a substantial backdrive current (i_{BD})—from 50 mA to 500 mA, depending on the device architecture. If node A is low, then node B is already high, and Driver 1 needs to supply little or no current during the test.

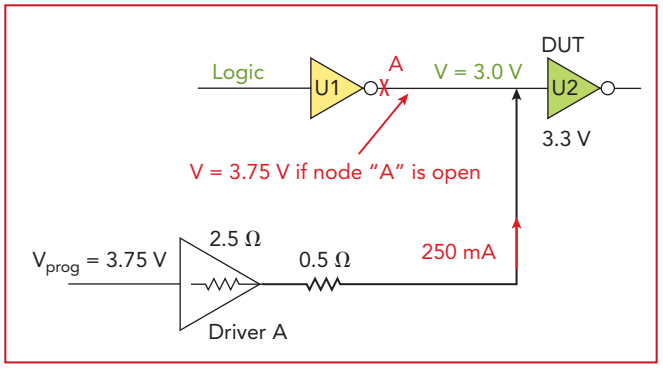

FIGURE 4. This test configuration exhibits an IR drop of 750 mV due to a 250-mA backdrive current through a 2.5-Ω driver output resistance and 0.5-Ω fixture and board resistance. Driver accuracy is ±100 mV, enabling V_{PROG} to rise as high as 3.85 V.

If node A transitions from high to low during the test because of activity elsewhere on the board, the necessary backdrive current changes from i_{BD} to 0 over a very short time period (Δt). The sudden change in current and the inherent inductance between the driver and node B—typically 1 to 10 µH—causes a voltage spike at node B that can be severe enough to damage devices connected to that node.

Consider a backdrive current of 100 mA, a Δt of 10 ns, and an inductance (L) of 1 µH. The transition produces a voltage spike:

$$V_{SPIKE} = 1\ \mu H\ (100\ mA/10\ ns) = 10\ V$$

For faster logic families, the problem is even more severe. Their lower output impedance requires higher backdrive currents and lower transition time.

Certain characteristics of in-circuit tester architecture will aggravate a device's susceptibility to overvoltage failure. **Figure 3a** shows conventional in-circuit shared logic-level assignments that input a single voltage level input to both Driver A and Driver B. In this case, Driver A has been programmed to an input voltage of 2.4 V, the level necessary to drive device U2 to a logic high. Because Driver B is slaved to that same voltage, it will subject U1's 1.2-V logic to overvoltage.

Testers designed specifically to serve low-voltage technologies, as in the schematic in **Figure 3b**, permit engineers to program the logic level independently for each pin. Each driver has its own programmable voltage for both high and low logic levels. Driver A delivers 2.4 V, while Driver B is programmed to apply only 1.1 V.

Inaccurate high-impedance tester drivers can also subject devices to overvoltage stress. The test configuration in **Figure 4** applies 250 mA of backdrive current to force the output of U1 to a logic high. This driver has an output impedance at 2.5 Ω and a path impedance of another 0.5 Ω, producing an IR drop in the test circuit of 750 mV. In addition, the driver has an accuracy specification of ±100 mV.

To accommodate the IR drop and to achieve an input voltage of 3.0 V at U2, you would need to program the input to Driver A above U2's 3.3-V nominal level to 3.75 V. With a driver accuracy of 100 mV, the programmed voltage could be as high as 3.85 V. If the output of U1 is open, the backdrive current is no longer required, and the tester drives the input of U2 to 3.85 V—an overvoltage condition.

If you replaced the high-impedance driver with a driver with an output resistance of only 0.05 Ω and an accuracy of ±15 mV, the tester will still push 250 mA of backdrive current, but the IR drop would be only 138 mV. Providing a 3.0-V input at U2 in this case would require you to program a voltage of 3.125 V. The driver error means that the actual voltage may be as high as 3.14 V. Therefore, even if the output of U1 is open, the voltage at U2 does not exceed safe levels.

Excessive current can also compromise device quality. In a worst-case scenario, the tester has to backdrive multiple outputs on the same device. In that circumstance, the ground bond wires or the power bond wires inside the chip have to carry backdrive currents from all backdriven digital outputs at the same time.

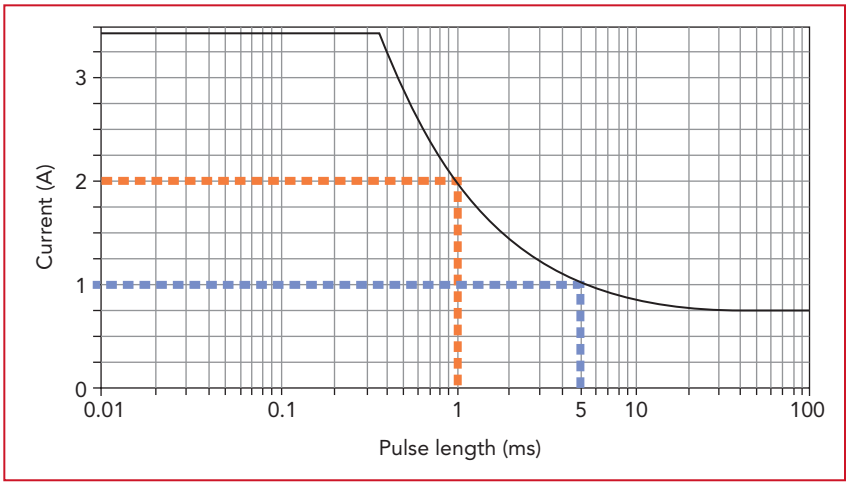

FIGURE 5. The curve represents what the UK Ministry of Defence has found to be safe backdrive current levels and pulse durations that will limit the temperature of a 1-mil-diameter aluminum bond wire to 210°C. A device with one ground bond carrying 2 A allows a pulse lasting only 1 ms (yellow dashed line). Adding a second ground bond to share the current permits a 5-ms pulse (blue dashed line). The values assume a 25°C ambient temperature and a 39-ms cooling-off period between pulses.

The 74AC244 bus driver, for example, features eight outputs, each requiring about 250 mA to backdrive, as well as a single power pin and a single ground pin. If there is only one bond wire between the ground pin and the die, then as much as 2 A could be flowing through that wire. If instead the pin and die were double-bonded—two bonded ground wires in parallel—then 1 A of current would flow along each of those paths.

Figure 5 illustrates what the UK Ministry of Defence (Ref. 2) has found to be safe operating parameters for backdriving on a 1-mil-diameter aluminum bond wire. According to the graph, with all eight outputs backdriven on a 74AC244 along a single bond wire carrying 2 A, a backdrive pulse longer than 1 ms would risk damaging that bond wire. A part from another vendor that featured two parallel bond wires could endure a backdrive pulse of 5 ms before experiencing the same level of stress.

```
DEVICE LABEL: U33_B1: (NAND tree Test)
DEVICE NAME: U33
DEVICE TYPE: 82801 (I/O Controller Hub-3V)

PIN    NODE            NAIL      BACKDRIVE
A3     PICH_HLCOMP      106       79.06 mA
G1     LAN_RXD1         640       73.79 mA
R21    RSMRST_           90      131.76 mA
W11    PCLK_ICH         105       84.33 mA
Y20    OVCUR_1          147      469.08 mA
R22    FERR             614       76.42 mA
C12    CPUINIT_         743      450.64 mA
D11    SB_A20M_         575      563.95 mA
Y17    SUS_STAT         531       73.79 mA
       GGNT_             61      171.29 mA
       RBF_              67      237.18 mA
       SBA0             122      176.56 mA
```

FIGURE 6. New debug software can show real-time backdrive information to help programmers identify harmful conditions.

How much backdrive?

We analyzed one manufacturer's test-related backdrive on a PC motherboard. Our analysis showed the following:

- 17 out of 17 digital bursts included backdriving conditions;
- 217 backdrive events exceeded 50 mA;
- the test exposed 96 nets on the board to backdrive conditions, 28 of them more than once;
- the mean backdrive current was 131 mA with a median of 87 mA;
- the maximum current was 543 mA; and
- the longest backdrive pulse width was 258 ms.

The manufacturer's staff claimed that by using design-for-manufacturing and design-for-test methods, they had diligently optimized the test program. They said they had not subjected the board to backdriving conditions and were quite surprised when we showed them our results.

Uncontrolled backdriving can be caused by a number of factors. For example, the test program may inadequately isolate devices from transients during the test, and incorrectly programmed drive levels can exceed input compliance limits, accidentally turning on ESD structures. At one point in our analysis of the PC motherboard, the test program applied 2.5 V to a 1.2V device. A test program may also connect bidirectional output bus drivers to pin drivers before switching the chips to input mode.

In some board topologies, the program may accidentally backdrive not the gates themselves but discrete small-value resistors connected between a long run of two digital devices communicating with one another. These resistors, typically with values of 22 Ω or 33 Ω and generally four to a pack, reside in the circuit to minimize transmission-line effects. They don't have a very high power rating, so backdriving can damage them when pins on either side are forced to different logic levels.

Last, it is not uncommon to see incorrect code loaded onto programmable devices. That type of error could, for example, backdrive an output that is supposed to be an input. *(continued)*

Figure 6 shows a screen from a debug environment that features real-time backdrive information to help programmers identify potentially harmful conditions. This type of information allows you to go back to the program and to the board schematic to identify alternate test steps that prevent such dangerous conditions.

Backdrive measurement circuitry can also save manufacturers money during production. Here, the debug tool can reveal incorrect device programs, open or faulty enable pins, and incorrect isolation vectors. The tool looks for backdrive durations of 1 ms to 25 ms and currents of 50 mA to 500 mA—parameters that users can set depending on the specific situation.

Thus, to avoid device damage, you must minimize backdrive currents and the length of time a circuit must endure them. By invoking all available tools—including new software debug tools—you can reduce test-vector execution times and ensure that logic devices do not accidentally change state during backdrive conditions. T&MW

REFERENCES

1. Hsue, C.W., and C.D.Hechtman, "Transient responses of an exponential transmission line and its applications to high-speed backdriving in in-circuit test," *IEEE Transactions on Microwave Theory and Techniques,* Volume 42, Issue 3, March 1994, pp. 458–462. www.ieeexplore.ieee.org/iel1/22/6852/00277440.pdf?arnumber=277440.

2. UK Ministry of Defence, Defence Standard 00-53/Issue 2, "Safe Operating Limits for Backdriving, July 2, 1999. www.dstan.mod.uk/data/00/053/00000200.pdf.

FOR FURTHER READING

Technical papers that provide a discussion of backdriving can be found at www.teradyne.com/atd/resource/type/technical_papers.html.

ACKNOWLEDGMENTS

The authors would like to recognize Alan Albee and Ken Maclean of Teradyne for their technical support and editorial contribution.

Tony Suto *is chief scientist at Teradyne (North Reading, MA), and* **John McNeill** *is associate professor at the Electrical and Computer Engineering Department at Worcester Polytechnic Institute (Worcester, MA).*