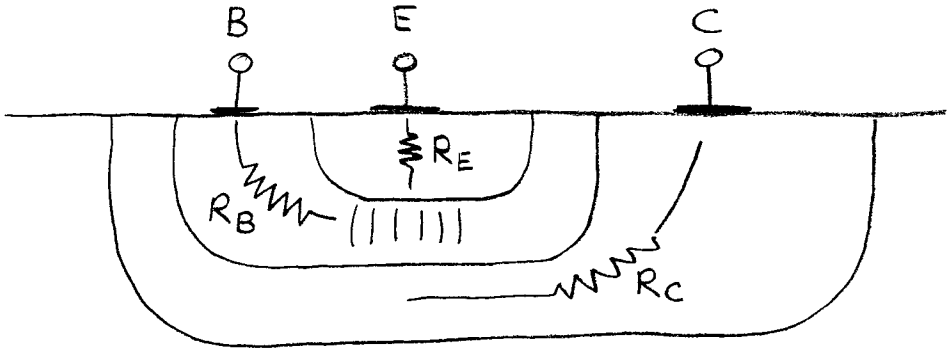
BJT "REAL WORLD" PARASITIC R



EMITTER R_E

USUALLY ~1Ω (E HEAVILY DOPED), NOT A PROBLEM
CAUTION: POWER APPLICATIONS!
SOLUTION: LARGER EMITTER AREA LOWERS R_E

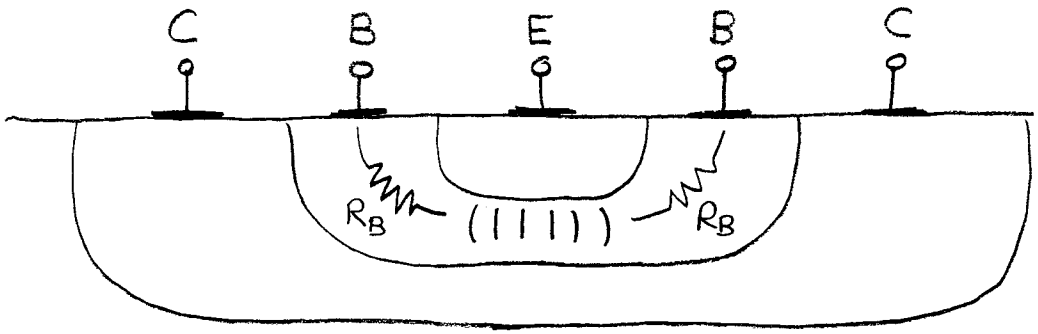
COLLECTOR R_C

HIGH (C LIGHTLY DOPED) ~1kΩ
BUT: IN SERIES WITH CURRENT SOURCE (NOISE OK)
CAUTION: QUASISATURATION ($I_C R_C$ DROP FORWARD BIAS ON INTERNAL B-C JUNCTION)
SOLUTION: LOWER R_C WITH BURIED LAYER

BASE R_B

MODERATE: ~100Ω TO 1kΩ
USUALLY MAJOR NOISE OFFENDER AT INPUT; SEES FULL GAIN

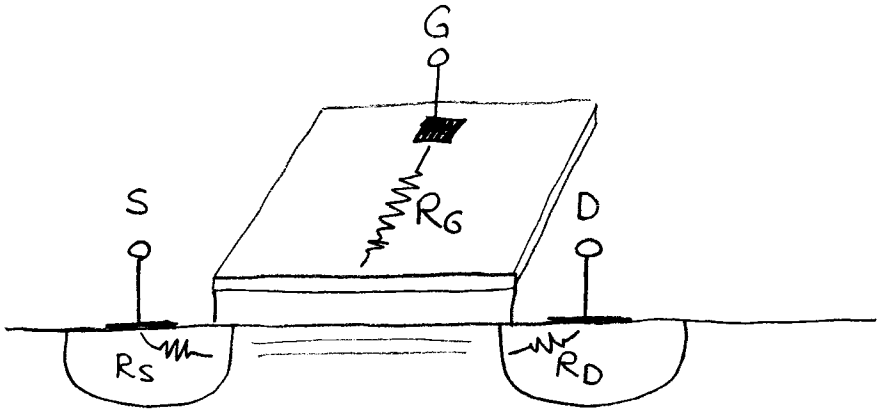
R_B SOLUTION "DOUBLE BASE"



PARALLEL COMBINATION $R_B/2$

BUT: C_{JC} (B-C) INCREASED (LARGER JCT AREA)

MOSFET "REAL WORLD" PARASITIC R



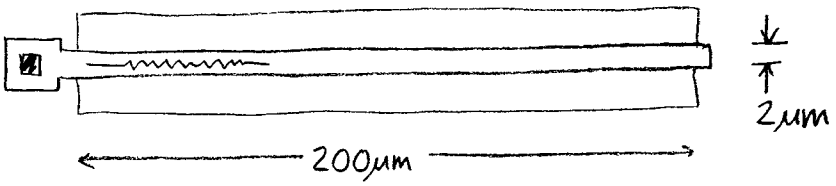
R_S, R_D

USUALLY ~ 10 TO 100Ω (S, D HEAVILY DOPED)
PLUS CONTACT RESISTANCE
CAUTION: POWER APPLICATIONS!
SOLUTION: LOTS OF CONTACTS

R_G GATE POLY RESISTANCE

CAN BE MODERATE TO HIGH (GATE GEOMETRY)
USUALLY MAJOR NOISE OFFENDER

EXAMPLE: W/L = 200/2 IN 20Ω/□ POLY



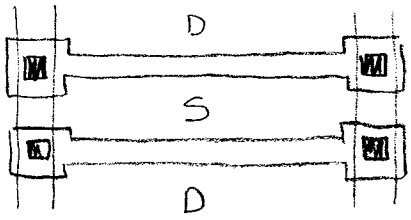
TO CENTER (AVERAGE)

$$R_G = \left(\frac{100\mu m}{2\mu m}\right)(20\Omega/\square) = 1\,k\Omega$$

SOLUTIONS

PROCESS: SILICIDE GATE
LOWERS SHEET R BY ~ 10X

LAYOUT: FINGERS; DOUBLE CONTACT



WIN BY N^2 FOR N FINGERS: $\frac{R_G}{N}$; N IN PARALLEL