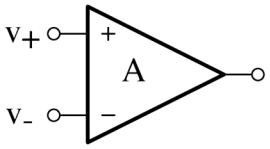
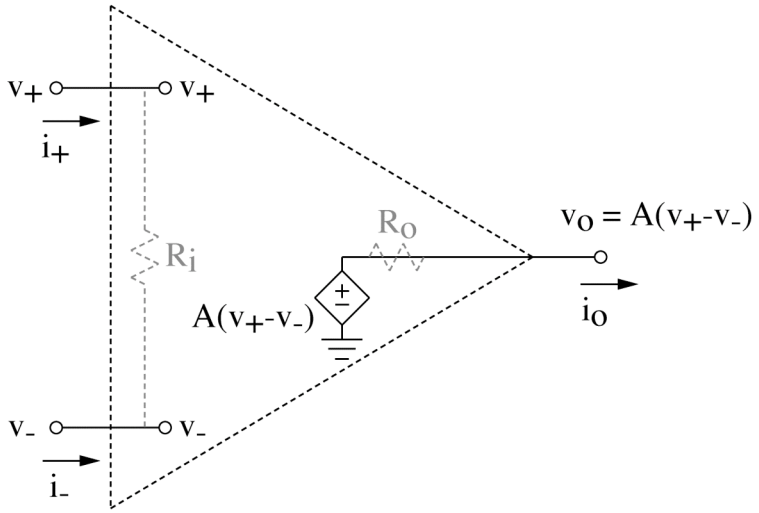
ECE3204 IDEAL OP-AMP SUMMARY





PROPERTY	INPUT RESISTANCE	OPEN LOOP GAIN	BANDWIDTH	OUTPUT RESISTANCE
IDEALIZATION	$R_i = \infty$	$A = \infty$	$BW = \infty$	$R_o = 0$
MEANING	Input currents = 0	Any v_o can be "supported" by infinitesimally small differential input ($v_+ - v_-$)	Signal of any frequency is OK	Output "looks like" ideal voltage source. Can drive any current required by load resistance
CONSEQUENCE	KCL at -, + terminals simplified. Always known that $i_- = 0$ and $i_+ = 0$	When negative feedback is present, $v_- = v_+$		Output current i_o determined by load