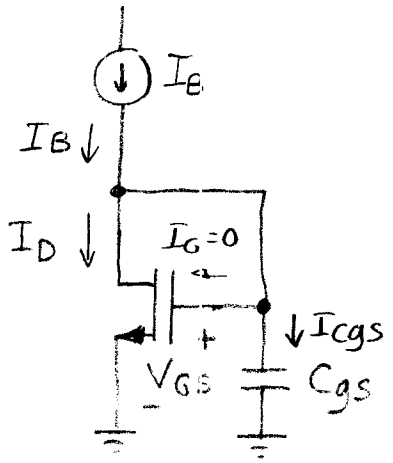
WHY DOES DIODE CONNECTED MOSFET HAVE TO CARRY $I_D = I_B$?



SUPPOSE $I_D \neq I_B$

SAY V_{GS} IS TOO SMALL SO $I_D < I_B$

KCL AT GATE NODE

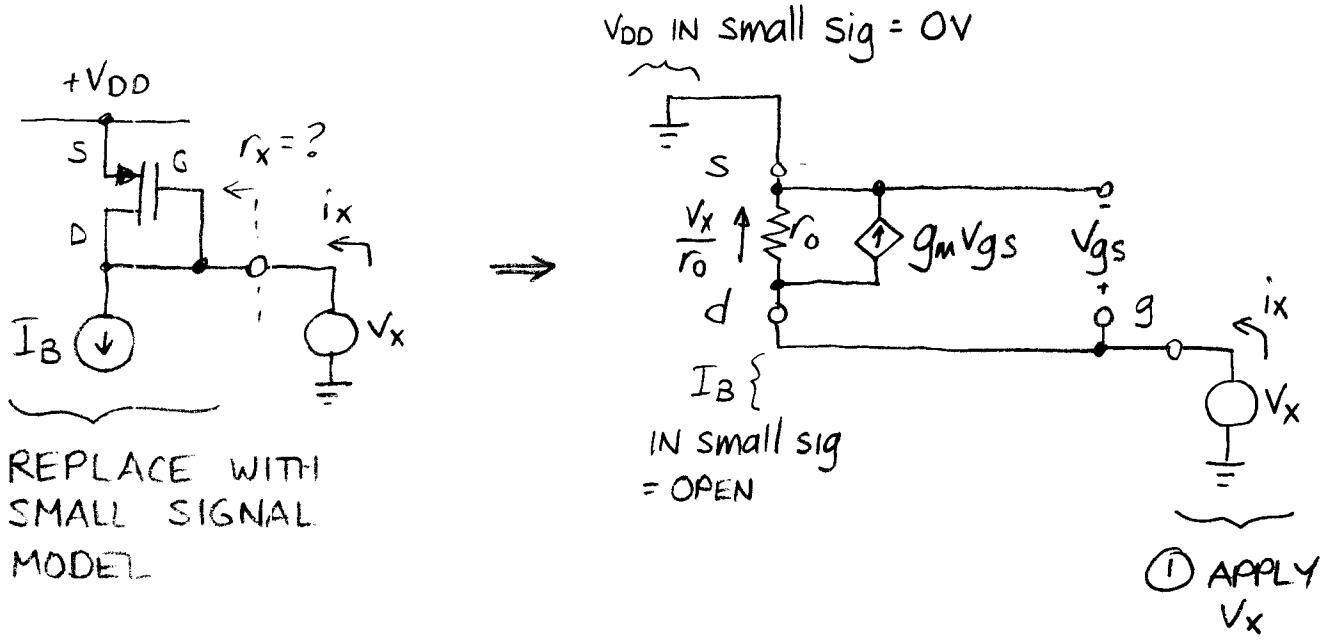
$$I_B = I_D + \underbrace{I_G}_{0} + I_{cgs}$$

IF $I_D < I_B$, THEN I_{cgs} WILL BE POSITIVE
$\Rightarrow$ CHARGING UP C_{gs} $\Rightarrow$ INCREASING I_D
$\Rightarrow$ MOVES I_D CLOSER TO I_B

SIMILARLY, IF $I_D > I_B$, V_{GS} WILL DECREASE

EQUILIBRIUM WHEN $\frac{dV_{GS}}{dt} = 0 \Rightarrow I_{cgs} = 0 \Rightarrow \boxed{I_B = I_D}$

SMALL SIGNAL RESISTANCE OF DIODE CONNECTED MOSFET



"IMPEDANCE AT A NODE" PROCEDURE

① APPLY V_x ② CALCULATE i_x ③ $r_x = \frac{V_x}{i_x}$

② KCL AT GATE

$$i_x = g_m V_{gs} + \frac{V_x}{r_o} \qquad i_x = g_m V_x + \frac{V_x}{r_o} = V_x\left(g_m + \frac{1}{r_o}\right)$$

KVL AROUND GATE: $V_{gs} = V_x$

③ $r_x = V_x / i_x$

$$\frac{V_x}{i_x} = \frac{1}{g_m + \frac{1}{r_o}} = \frac{1}{g_m} \parallel r_o \qquad \text{USUALLY } r_o \gg \frac{1}{g_m}$$

$$\boxed{r_x \approx \frac{1}{g_m}}$$

SMALL SIGNAL MODEL FOR DIODE CONNECTED MOSFET (NMOS OR PMOS) IS $1/g_m$: