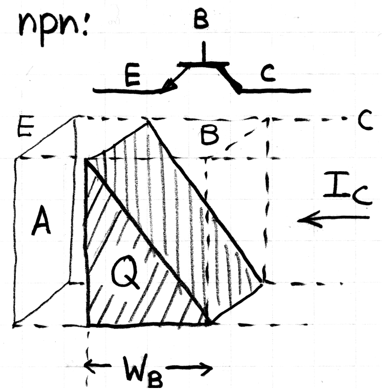
<table>
<tr><td>



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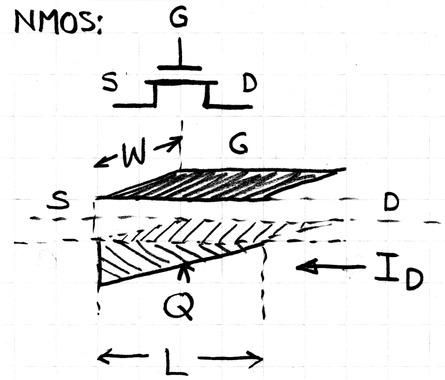

</td></tr>
<tr><td rowspan="2">Current in collector terminal:
$$I_C = \underbrace{\frac{qAD_n n_i^2}{2W_B N_A}}_{I_S} e^{(V_{BE}/V_T)}$$</td><td colspan="2">Current in drain terminal (active region):</td></tr>
<tr><td>Long channel (L >> 1 μm):
$$I_D = \frac{\overline{\mu} C_{OX}}{2} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2$$</td><td>Short channel (L << 1 μm):
$$I_D = C_{OX} W v_{SAT} \left(V_{GS} - V_{TH}\right)$$</td></tr>
<tr><td colspan="3">Representing current in form of I = Q/ΔT</td></tr>
<tr><td>Charge in base:
$$Q = \frac{qAW_B n_i^2}{2N_A} e^{(V_{BE}/V_T)}$$</td><td>Charge in channel:
$$Q = \frac{C_{OX} WL}{2} \left(V_{GS} - V_{TH}\right)$$</td><td>Charge in channel:
$$Q = C_{OX} WL \left(V_{GS} - V_{TH}\right)$$</td></tr>
<tr><td>Transit time through base:
$$\Delta T = \frac{W_B{}^2}{2\mu V_T}$$</td><td>Transit time through channel:
$$\Delta T = \frac{L^2}{2\overline{\mu}\left(V_{GS} - V_{TH}\right)}$$</td><td>Transit time through channel:
$$\Delta T = \frac{L}{v_{SAT}}$$</td></tr>
<tr><td colspan="3">Applied voltage:</td></tr>
<tr><td>V_{BE}: Applied across base-emitter junction</td><td colspan="2">V_{GS}: Applied from gate to source</td></tr>
<tr><td colspan="3">Geometry under designer control, subject to process (mask lithography) minimum:</td></tr>
<tr><td>A: Base-emitter junction area</td><td colspan="2">W: Width of channel under gate
L: Length of channel under gate</td></tr>
<tr><td colspan="3">Process parameters:</td></tr>
<tr><td>W_B: Width of base region (determined by diffusion of dopant atoms for base, emitter regions)
N_A: Dopant density of p-type atoms in base</td><td colspan="2">C_{OX}: Gate oxide capacitance per unit area (determined by thickness, dielectric constant of gate oxide)
V_{TH}: Threshold voltage (determined by lots of things; see Razavi ch. 16)</td></tr>
<tr><td colspan="3">Physical parameters:</td></tr>
<tr><td>μ: **Bulk** mobility of carriers in base
D_n: Diffusion constant of electrons in base
n_i: Intrinsic carrier concentration (strongly temperature dependent
q: Electron charge
V_T: thermal voltage = kT/q ~ 26mV @ T=300K</td><td>$\overline{\mu}$: **Surface** mobility of carriers in channel</td><td>v_{SAT}: Saturation velocity (maximum due to high field; ≈ 1E+7 cm/s.</td></tr>
</table>

ECE4902 MOS BJT Comparison

Notes:

<u>Speed</u>

W_B, L are critical dimensions for improving speed performance

Note exponent of 2 in ΔT equation indicates that improvement goes as factor squared; meaning there are two reasons speed improves:

1) Shorter distance for carrier to travel
2) More "push" (steeper diffusion gradient for BJT, higher E field for MOSFET in long channel limit)

<u>Factors in MOS - BJT speed performance:</u>

1) Bulk mobility (BJT) always better than surface mobility (MOSFET)
2) Reducing critical dimension involves different process considerations
3) Trying to increase MOSFET speed by increasing V_{GS}-V_{TH} has two problems:
   - reduces transconductance efficiency
   - carrier velocity doesn't increase as much as expected due to velocity saturation (Razavi ch. 16)

Small signal transconductance g_m:	
$g_m = \dfrac{I_C}{V_T}$	$g_m = \dfrac{I_D}{(V_{GS} - V_{TH})/2}$

<u>Why BJT transconductance will always be better for roughly similar bias currents:</u>

Thermal voltage V_T is less than (V_{GS}-V_t); trying to reduce V_{GS}-V_t below ~ 150mV causes MOSFET to enter subthreshold (weak inversion) region of operation

<u>Advantages of MOS:</u>

Near ∞ input resistance looking into gate vs. base current for BJT (better buffer on input side)
Better analog switch; truly ohmic at origin of V_{DS}-I_D plot (sample & hold)
Compatible with digital CMOS (process cost advantage)
Comes out of non-active operating region more quickly (BJT slow out of saturation)
More robust current sources (gentler "crash" than BJT into saturation)

<u>Advantages of BJT</u>

More speed, transconductance per amount of bias current
Higher intrinsic gain for actively loaded stage (better Early voltage)
Lower output resistance at emitter vs. source of MOSFET (better buffer on output side)
"Closer" to fundamental physics (e.g. bandgap voltage reference)
Follows exponential model over 5 - 8 orders of magnitude (analog computation; multipliers)
Higher output resistance current sources