MOSIS WAFER ACCEPTANCE TESTS

RUN: T6BF VENDOR: AMIS
TECHNOLOGY: SCN15 RUN TYPE: SKD FEATURE SIZE: 1.6 microns

Each wafer fabrication run has its own code; this run is designated "T6BF"

FEATURE SIZE is the minimum gate length; 1.6μm for this process

TECHNOLOGY and RUN TYPE are more specific; these codes indicate added features in the process (for example, linear capacitors and BJTs)

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: SCNA16_AMIS

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	4.0/1.6			
Vth		0.57	-0.97	volts
SHORT	20.0/1.6			
Idss		183	-72	uA/um
Vth		0.55	-0.93	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/1.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.58	-0.88	volts
Vjbkd		16.6	-14.5	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.62	0.47	V^0.5
K' (Uo*Cox/2)		35.7	-12.0	uA/V^2
Low-field Mobility		632.73	212.68	cm^2/V*s

Vth is the threshold voltage; MINIMUM refers to the smallest geometry devices allowed by the process design rules. For logic applications, often only minimum size devices are used.

Idss is the current per unit width with maximum voltage (in the case of this process, 5V) applied for V_{GS}. Expressing current this way allows the designer to rapidly determine required device size for a given current. For example, if 2mA of drive current is required for a P-channel MOSFET when the gate is fully turned on, the width should be
2mA / (86μA/μm) = 23.3μm
Note also that the threshold voltage Vth for the SHORT device is different than the MINIMUM case -- a second-order effect that SPICE needs to keep track of.
Vpt is the punch-through voltage, beyond which the device will be damaged.

This is the leakage current per unit width when V_{GS}=0. An important parameter for analog switch design, especially in sample-and-hold circuits when the hold capacitor can be partially discharged by the leakage current of a MOSFET which should be "off".

Again, note that the threshold voltage is affected by device geometry.
Vjbkd is the breakdown voltage of the active-substrate pn junction;
Ijlk is the reverse bias leakage current of the junction.
Gamma is the body-effect parameter, which expresses how the threshold voltage is affected by the source-substrate reverse bias voltage.

K' is the transconductance parameter used in some expressions of the square law

$$I_D = \underbrace{\frac{\mu C_{OX}}{2}}_{K'} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2$$

Low-field mobility is the value of μ for E fields below the velocity saturation limited region.

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)
SCN (lambda=0.8)	0.00

"Poly bias" allows the software which writes the mask specification file to make the mask dimension larger or smaller than what is drawn in the layout software. This can account for the over- or under-etching of the polysilicon.
Here "lambda" refers to the unit spatial dimension of the layout software used to design the masks (not the channel length modulation λ).
See Razavi ch. 17 and Johns & Martin sec. 2.3 for more information.

POLY2 TRANSISTORS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	4.8/3.2			
Vth		0.86	-1.14	volts
SHORT	9.6/3.2			
Vth		0.86	-1.09	volts
LARGE	28.8/28.			
Vth		0.87	-1.08	volts
K' (Uo*Cox/2)		21.5	-6.8	uA/V^2

In this technology, transistors can also be fabricated using a second polysilicon layer for the gate. The transistor parameters are different (and not quite as good) since the resulting MOSFETs have a thicker gate oxide.

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

This is for a MOSFET which uses the field oxide as the gate oxide. We don't want this to function as a MOSFET (if it did, unrelated active areas could be shorted together). In this case, the field implant worked, because the threshold voltage is ~15V. Since this process is intended for 5V systems, the FOX transistor will never be on.

BIPOLAR PARAMETERS		NPN	UNITS
2X1	2X1		
Beta		129	
V_early		43.7	volts
Vce,sat		---	volts
2X2	2X2		
Beta		131	
V_early		43.7	volts
Vce,sat		---	volts
2X4	2X4		
Beta		131	
V_early		43.4	volts
Vce,sat		---	volts
2X8	2X8		
Beta		130	
V_early		43.2	volts
Vce,sat		---	volts
BVceo		18.9	volts
BVcbo		30.2	volts
BVebo		8.0	volts

This process technology includes layers that allow fabrication of NPN bipolar transistors. It turns out that these BJTs have reasonably good DC performance, but not very good high frequency performance. Usually these devices would be used in a circuit such as the bandgap voltage reference which makes use of the exponential voltage-current behavior of the BJT in developing a temperature-stable DC reference voltage.

PROCESS PARAMETERS	N+	P+	POLY	POLY2	PBASE	M1	M2	UNITS
Sheet Resistance	52.2	75.6	25.0	22.3	2257.5	0.05	0.03	ohms/sq
Contact Resistance	54.5	41.1	25.4	17.0			0.05	ohms
Gate Oxide Thickness	306							angstrom

PROCESS PARAMETERS	N_W	UNITS
Sheet Resistance	1714	ohms/sq
Contact Resistance		ohms

Sheet resistance: *These are the numbers to use when determining the physical dimensions of a resistor to achieve a certain value of resistance. The layers are:*

- *N+* — *Heavily doped region of N-type diffusion used for source, drain of N-channel MOSFETs*
- *P+* — *Heavily doped region of P-type diffusion used for source, drain of P-channel MOSFETs*
- *POLY* — *Polysilicon metal used for gates of MOSFETs*
- *POLY2* — *A second layer of polysilicon which can also be used for MOSFET gates (Also, POLY and POLY2 can be used with thin oxide between to make a linear capacitor (See capacitance parameters below)*
- *PBASE* — *A moderately doped region of P-type diffusion used as the base for NPN bipolar transistors*
- *M1* — *First layer of aluminum metallization; much lower sheet resistance than polysilicon or diffusion*
- *M2* — *Second layer of metallization; lowest sheet resistance since thickness of M2 is greater than thickness of M1*
- *N_W* — *Lightly doped region of N-type diffusion used as a well (sort of a "local substrate") used for P-channel MOSFETs*

Contact resistance: *This is the resistance of one contact between METAL1 and the layer indicated. For example, one contact between the heavily doped N-type source or drain region of a MOSFET (N+) and the first layer of metal (M1) has a resistance of 54.5 Ω - not negligible! When it is necessary to lower resistance, many contacts are made in parallel to give a lower total resistance.*

Gate Oxide Thickness: *This is the oxide thickness tox used to determine the gate capacitance per unit area. Check by comparing to the gate oxide capacitance per unit area:*

$$\frac{\varepsilon_{OX}}{t_{OX}} = \frac{K_{OX}\varepsilon_O}{t_{OX}} = \frac{3.9(8.85E-12\ F/m)}{306E-10\ m} = 1.13E-3\ F/m^2$$

Which agrees pretty well with the 1128aF/um² for POLY-to-N+ shown below

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	N_W	UNITS
Area (substrate)	291	302	36	37	21	13	129	aF/um^2
Area (N+active)			1128	730	50	26		aF/um^2
Area (P+active)			1110	723				aF/um^2
Area (poly)				592	46	23		aF/um^2
Area (poly2)					46	23		aF/um^2
Area (metal1)						38		aF/um^2
Fringe (substrate)	79	160			31	27		aF/um
Fringe (poly)					58	44		aF/um
Fringe (metal1)						55		aF/um
Overlap (N+active)			173					aF/um
Overlap (P+active)			231					aF/um

These are parallel-plate capacitance (per unit area) between the layers indicated. For example, a capacitor using M1 and M2 as the plates will have a capacitance of 38aF/µm² (atto is 1E-18) per micron squared. A capacitor 100µm x 100µm has an area of 1E+4µm², so the capacitance would be 380E-15 F, or 0.38pF.

Fringe and overlap capacitances are edge effects, and therefore are given per unit length. The 100um x 100um capacitor mentioned in the example above would have a perimeter of 400um. The fringe capacitance from M1 to M2 is 55aF/µm. Thus the capacitance due to the fringing field would be (400µm)(55aF/µm)=22 E-15 F = 22fF. Total for the 100um x 100um capacitor will be the sum of contributions from parallel plate + fringing: 0.38pF + 22fF = 0.402pF.

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	1.80	volts
Vinv	1.5	2.11	volts
Vol (100 uA)	2.0	0.44	volts
Voh (100 uA)	2.0	4.33	volts
Vinv	2.0	2.31	volts
Gain	2.0	-15.06	

This data describes performance of CMOS logic inverters. "K" is the size ratio between the P-channel and N-channel MOSFETs in the CMOS inverter. For example, for the case K=1.5, the PMOS device in the inverter has a width 1.5X the NMOS width.
Vinv is the logic threshold of the inverter.
Vol and Voh are the output voltages the inverter output can maintain while sourcing (Voh) or sinking (Vol) the indicated current of 100µA.
Gain is the slope of the Vout vs. Vin transfer characteristic of the inverter at its switching threshold. Although it might seem irrelevant to worry about an "analog" concept like gain in a digital system, it is actually very important that the gain magnitude be greater than unity: if the gain is less than one, logic swings become smaller and smaller as a logic signal propagates through a sequence of gates, until the logic swing is too small to switch a gate at all.

Ring Oscillator Freq.		
DIV64 (31-stg,5.0V)	37.70	MHz
Ring Oscillator Power		
DIV64 (31-stg,5.0V)	1.60	uW/MHz/gate

A ring oscillator is made up of a chain of inverters with a net signal inversion from input to output (enforced in this case by using an odd number of inverters). When the output of the chain is tied back to the input, this completes a ring, and a signal edge will propagate around the ring, forming an oscillator. The oscillation frequency is

$$f_{OSC} = \frac{1}{2 \cdot N \cdot t_{PD}}$$

where N is the number of stages in the ring and t_{PD} is the propagation delay of the inverter. Thus measuring the ring oscillator frequency is an easy way to determine the propagation delay of the logic inverter; in this case with an oscillator frequency of f_{OSC} = 37.7 MHz it is

$$t_{PD} = \frac{1}{2 \cdot N \cdot f_{OSC}} = \frac{1}{2 \cdot 31 \cdot (37.7E+6\ Hz)} = 428\ ps$$

The ring oscillator power measurement can be used to estimate the power consumed by a digital circuit given the number of gates and the switching frequency.

T6BF SPICE LEVEL3 parameters are available for classroom instructional purposes but not for actual IC design work.

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* DATE: Jan 12/07
* LOT: T6BF                  WAF: 6102
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                   LEVEL   = 3
+ TOX    = 3.06E-8          NSUB   = 9.34116E15       GAMMA   = 0.7671649
+ PHI    = 0.9554462        VTO    = 0.6111337        DELTA   = 0.7532645
+ UO     = 541.3782915      ETA    = 6.06068E-4       THETA   = 0.070589
+ KP     = 7.399509E-5      VMAX   = 2.102169E5       KAPPA   = 0.5
+ RSH    = 23.7230709       NFS    = 6.009445E11      TPG     = 1
+ XJ     = 3E-7             LD     = 8.616976E-15     WD      = 6.516763E-7
+ CGDO   = 1.73E-10         CGSO   = 1.73E-10         CGBO    = 1E-10
+ CJ     = 2.872743E-4      PB     = 0.838875         MJ      = 0.5
+ CJSW   = 1.238328E-10     MJSW   = 0.05             )
*
.MODEL CMOSP PMOS (                                   LEVEL   = 3
+ TOX    = 3.06E-8          NSUB   = 1E17             GAMMA   = 0.4950231
+ PHI    = 0.7              VTO    = -0.889286        DELTA   = 0.2719659
+ UO     = 100              ETA    = 9.990442E-5      THETA   = 0.1262713
+ KP     = 2.524773E-5      VMAX   = 1.930155E5       KAPPA   = 90
+ RSH    = 0.2004376        NFS    = 5.850358E11      TPG     = -1
+ XJ     = 2E-7             LD     = 1.001708E-14     WD      = 9.821909E-7
+ CGDO   = 2.31E-10         CGSO   = 2.31E-10         CGBO    = 1E-10
+ CJ     = 2.993018E-4      PB     = 0.8              MJ      = 0.4481429
+ CJSW   = 1.609243E-10     MJSW   = 0.1174914        )
*
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These are the SPICE parameters that would be used for simulating the MOSFET using the Level 3 model. Note that you are cautioned not to use these parameters for actual IC design work! The more accurate, but more complicated, Level 49 BSIM3 model parameters are given on the next two pages.

To simulate using the parameters you extract in the studio labs for the MC14007 MOSFET, you will use a (much simpler) set of model parameters based on the parameters extracted from your lab measurements.

T6BF SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

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* DATE: Jan 12/07
* LOT: T6BF                  WAF: 6102
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 3.06E-8
+XJ      = 3E-7           NCH     = 7.5E16         VTH0    = 0.5467907
+K1      = 0.9040053      K2      = -0.0667247     K3      = 3.2074393
+K3B     = -2.4863898     W0      = 1.726569E-6    NLX     = 2.003139E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.5616596      DVT1    = 0.5961287      DVT2    = -0.5
+U0      = 659.1539164    UA      = 1.571393E-9    UB      = 6.331182E-19
+UC      = 1.327941E-11   VSAT    = 9.85294E4      A0      = 0.5995609
+AGS     = 0.1306233      B0      = 2.470264E-6    B1      = 5E-6
+KETA    = -0.0107507     A1      = 0              A2      = 1
+RDSW    = 3E3            PRWG    = -0.0293948     PRWB    = -0.0296004
+WR      = 1              WINT    = 6.909849E-7    LINT    = 2.918303E-7
+XL      = 0              XW      = 0              DWG     = -1.088946E-8
+DWB     = 2.842396E-8    VOFF    = -0.0700562     NFACTOR = 0.4708962
+CIT     = 0              CDSC    = 8.279564E-8    CDSCD   = 1.482736E-6
+CDSCB   = 3.869072E-5    ETA0    = 0.0110351      ETAB    = 0.0262778
+DSUB    = 0.2442264      PCLM    = 0.2186109      PDIBLC1 = 0.0110461
+PDIBLC2 = 3.644817E-3    PDIBLCB = -0.1           DROUT   = 0.0795384
+PSCBE1  = 2.153596E9     PSCBE2  = 5.005E-10      PVAG    = 0.2222499
+DELTA   = 0.01           RSH     = 52.2           MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 1.73E-10       CGSO    = 1.73E-10       CGBO    = 2E-9
+CJ      = 2.767682E-4    PB      = 0.99           MJ      = 0.5559833
+CJSW    = 1.417238E-10   PBSW    = 0.9889456      MJSW    = 0.1
+CJSWG   = 6.4E-11        PBSWG   = 0.9889456      MJSWG   = 0.1
+CF      = 0               )
*
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.MODEL CMOSP PMOS (                             LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 3.06E-8
+XJ      = 3E-7         NCH     = 2.4E16        VTH0    = -0.8476404
+K1      = 0.4513608    K2      = 2.379699E-5   K3      = 13.3278347
+K3B     = -2.2238332   W0      = 9.577236E-7   NLX     = 4.909017E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.7546343    DVT1    = 0.4613224     DVT2    = -0.179467
+U0      = 236.8923827  UA      = 3.833306E-9   UB      = 1.487688E-21
+UC      = -1.08562E-10 VSAT    = 1.842738E5    A0      = 0.3536635
+AGS     = 0.2659996    B0      = 1.980132E-6   B1      = 5E-6
+KETA    = 0.0303949    A1      = 0             A2      = 0.364
+RDSW    = 3E3          PRWG    = 0.0725853     PRWB    = -0.1860065
+WR      = 1            WINT    = 7.565065E-7   LINT    = 1.422522E-7
+XL      = 0            XW      = 0             DWG     = -2.13917E-8
+DWB     = 3.857544E-8  VOFF    = -0.0877184    NFACTOR = 0.2508342
+CIT     = 0            CDSC    = 2.924806E-5   CDSCD   = 1.497572E-4
+CDSCB   = 1.091488E-4  ETA0    = 0.20103       ETAB    = -0.0129682
+DSUB    = 0.2873       PCLM    = 6.403032E-10  PDIBLC1 = 7.477411E-4
+PDIBLC2 = 3.271335E-3  PDIBLCB = -1E-3         DROUT   = 1E-3
+PSCBE1  = 3.515038E9   PSCBE2  = 5.273648E-10  PVAG    = 14.985
+DELTA   = 0.01         RSH     = 75.6          MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.31E-10     CGSO    = 2.31E-10      CGBO    = 2E-9
+CJ      = 2.995053E-4  PB      = 0.8           MJ      = 0.4487006
+CJSW    = 1.586304E-10 PBSW    = 0.8971831     MJSW    = 0.1136092
+CJSWG   = 3.9E-11      PBSWG   = 0.8971831     MJSWG   = 0.1136092
+CF      = 0             )
*
```