MOSIS PARAMETRIC TEST RESULTS

RUN: N88Z VENDOR: AMI
TECHNOLOGY: SCN12 FEATURE SIZE: 1.2 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. 1.2 micron ABN.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	1.8/1.2			
Vth		0.69	-1.03	Volts

* Vth is the threshold voltage; MINIMUM refers to the smallest geometry
* devices allowed by the process design rules. For logic applications,
* often only minimum size devices are used

SHORT	10.8/1.2			
Idss		193	-86	uA/um
Vth		0.57	-0.89	Volts
Vpt		10.0	-14.8	Volts

* Idss is the current per unit width with maximum voltage (in the case of
* this process, 5V) applied for VGS. Expressing current this way allows
* the designer to rapidly determine required device size for a given
* current. For example, if 1mA of drive current is required for a P-channel
* MOSFET when the gate is fully turned on, the width should be
* 2mA / (86uA/um) = 23.3um
* Note also that the threshold voltage Vth is different than the MINIMUM case --
* a second-order effect that SPICE needs to keep track of
* Vpt is the punch-through voltage, beyond which the device will be damaged.

WIDE	30/1.2			
Ids0		0.8	-0.5	pA/um

* This is the leakage current per unit width when VGS=0. An important
* parameter for analog switch design, especially in sample-and-holds
* when leakage current discharges the hold capacitor.

LARGE	10.8/10.8			
Vth		0.61	-0.87	Volts
Vjbkd		16.9	-15.7	Volts
Ijlk		-26.7	3.8	pA
Gamma		0.64	0.83	V^0.5

* Again, note that the threshold voltage is affected by device geometry.
* Vjbkd is the breakdown voltage of the active-substrate pn junction;
* Ijlk is the reverse bias leakage current of the junction.
* Gamma is the body-effect parameter, which expresses how the threshold
* voltage is affected by the source-substrate reverse bias voltage.

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

* This is for a MOSFET which uses the field oxide as the gate oxide.
* We don't want this to function as a MOSFET (if it did, unrelated
* active areas could be shorted together). In this case, the field
* implant worked, because the threshold voltage is ~15V. Since this
* process is intended for 5V systems, the FOX transistor will never be on.

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PROCESS PARAMETERS   N+ACTV  P+ACTV  POLY  POLY2  MTL1   MTL2   N_WELL  UNITS
 Sheet Resistance     53.7    76.2   26.1  25.2   0.05   0.03   1524    ohms/sq
* These are the numbers to use when determining the physical dimensions
* of a resistor to achieve a certain value of resistance.  The layers are
* N+ACTV  Heavily doped N-type region used for source, drain of N-channel MOSFETs
* P+ACTV  Heavily doped P-type region used for source, drain of P-channel MOSFETs
* POLY    Polysilicon metal used for gates of MOSFETs
* POLY2   A second layer of polysilicon which can also be used for MOSFET gates
*         Also, POLY and POLY2 can be used with thin oxide between to make a
*         linear capacitor (See capacitance parameters below)
* MTL1    First layer of aluminum metalization; much lower sheet resistance
* MTL2    Second layer of metalization; lowest sheet resistance since thickness
*         of MTL2 is greater than thickness of MTL1
* N_WELL  Lightly doped N-type region used as a well (sort of a "local
*         substrate") used for P-channel MOSFETs

PROCESS PARAMETERS    N+ACTV  P+ACTV  POLY  POLY2  MTL1   MTL2   N_WELL  UNITS
 Width Variation       -0.62  -0.85  -0.12  0.27   0.35   -0.06          microns
  (measured - drawn)
* This describes the difference between the drawn dimensions (on the mask) and
* actual dimensions after fabrication.  The difference is due to nonidealities
* of the chemical process such as overetching or sideways diffusion

PROCESS PARAMETERS    N+ACTV P+ACTV  POLY POLY2 MTL1   MTL2   N_WELL  UNITS
 Contact Resistance    65.8   36.3  25.7  20.2           0.06          ohms
* This is the resistance of one contact between METAL1 and the layer
* indicated.  For example, one contact between N+Active and METAL1 has
* a resistance of 65.8 Ohms - not negligible!  To lower resistance,
* many contacts are made in parallel to give a lower total resistance

 Gate Oxide Thickness 304                                                angstroms
* This is the oxide thickness tox used to determine the gate capacitance per
* unit area.  Check: eox/tox=(3.9)(8.85E-12F/m)/(3.04E-8m)=1.14E-3F/m^2
* Which agrees pretty well with the 1135aF/um^2 for poly-to-N+active shown below

CAPACITANCE PARAMETERS N+ACTV P+ACTV   POLY  POLY2  MTL1  MTL2  N_WELL  UNITS
 Area (substrate)      287    296       36           20    13     28    aF/um^2
 Area (N+active)                     1135   706     49    25           aF/um^2
 Area (P+active)                     1117   697                        aF/um^2
 Area (poly)                               596     45    21           aF/um^2
 Area (poly2)                                      45                 aF/um^2
 Area (metal1)                                           38           aF/um^2
* These are parallel-plate capacitance (per unit area) between the layers
* indicated.  For example, a capacitor using METAL1 and METAL2 as the plates
* will have a capacitance of 38aF/um^2 (atto is 1E-18) per micron squared.
* A capacitor 100um x 100um has an area of 1E+4um^2, so the capacitance
* would be 380femtofarads, or 0.38pF.

 Fringe (substrate)     99    148                    44    35           aF/um
 Fringe (poly)                                       55    39           aF/um
 Fringe (metal1)                                           48           aF/um
 Overlap (N+active)                   170                               aF/um
 Overlap (P+active)                   193                               aF/um
* Fringe and overlap capacitances are edge effects, and therefore are given
* per unit length.  The 100um x 100um capacitor mentioned in the example
* above would have a perimeter of 400um.  The fringe capacitance from METAL1
* to METAL2 is 48aF/um.  Thus the capacitance due to the fringing field
* would be (400um)(48aF/um)=19.2 femtofarad.
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N88Z SPICE LEVEL3 PARAMETERS

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* These are the SPICE parameters used for simulating the MOSFET.  To simulate
* using the parameters you extract in the studio labs for the CD4007 MOSFET, you
* will use a (much simpler) set of model parameters based on the parameters
* extracted from your lab measurements.

.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.0400E-08 XJ=0.200000U TPG=1
+ VTO=0.6081 DELTA=1.3700E+00 LD=9.0910E-10 KP=7.4209E-05
+ UO=653.3 THETA=9.5780E-02 RSH=5.1480E+01 GAMMA=0.6166
+ NSUB=1.4780E+16 NFS=5.9090E+11 VMAX=1.8150E+05 ETA=7.7500E-02
+ KAPPA=2.4680E-01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.4138E-10 CJ=2.8065E-04 MJ=5.3057E-01 CJSW=1.4649E-10
+ MJSW=1.0000E-01 PB=9.7858E-01

.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.0400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8311 DELTA=3.1900E+00 LD=9.0910E-10 KP=1.9344E-05
+ UO=170.3 THETA=1.0050E-01 RSH=3.3060E+01 GAMMA=0.3046
+ NSUB=3.6060E+15 NFS=5.9090E+11 VMAX=1.6930E+05 ETA=8.5870E-02
+ KAPPA=9.9940E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.2737E-10 CJ=2.9597E-04 MJ=4.4146E-01 CJSW=1.4645E-10
+ MJSW=1.0000E-01 PB=7.4913E-01
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