The Effect of Channel Width on Jitter in CMOS Ring Oscillators

by

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Abstract

Oscillators are a critical component in many electronic systems and improving their jitter performance is an ongoing process.

Harmonic oscillators offer very good jitter performance but typically require the use of either an off-chip inductor, which will defeat the goal of integration, or the use of an on-chip inductor, which will deliver poorer jitter performance at the cost of die area.

The ring oscillator is easy-to-design and easily integrated. Without the need for inductors, the ring oscillator occupies far less die area than a harmonic oscillator. Unfortunately, the jitter performance of the ring oscillator falls short of the jitter performance of harmonic oscillators.

Despite its shortcomings the ring oscillator satisfies a niche where moderate jitter performance, high levels of integration with low die real estate, and a wide tuning range are required.

This thesis investigates the relationship between MOSFET channel width and the jitter in ring oscillators with the goal of finding out if wider devices will produce lower jitter. A test chip with four VCOs was realized in silicon on a TSMC 0.35μm CMOS process.

The results indicate that increasing transistor width improves jitter in a manner consistent with the theoretical predictions.

Acknowledgements

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Chapter 1 Introduction

1.1 Goals and Motivation

Precise timing is essential in modern electronics. Digital communication systems and microprocessors depend on timing signals to synchronize and regulate their operations. Imprecise timing can result in bit errors or cause the failure of a system. Electronic systems have typically derived their timing from externally generated clock sources but faster clock speeds and the quest for greater levels of integration has led to the placement of the oscillator on the same die as the electronics that use them. The cost of greater integration where oscillators are concerned is a decrease in the purity of the clock signals. This decrease in purity is the result of noise and is manifested in the form of jitter. When the periods of an oscillator's output vary about their mean that phenomenon is known as jitter.

One of the popular methods of generating good quality clock signals has been the LC oscillator, which consists of a well-matched inductor and capacitor pair that is designed to resonate at a particular frequency. Integrating the LC oscillator has been achieved but doing so requires the use of integrated inductors and capacitors, both of which consume

large amounts of die area. The integration of these resonant components brings with it increased resistances that reduce the quality of the periodic output of these oscillators.

Ring oscillators are oscillators that are built around the inherent instability of inverters connected back-to-back in a ring. This instability causes oscillation to occur. While ring oscillators exhibit high levels of integration and can be tuned over a very wide frequency range, the quality of their output falls short of the LC oscillator's.

While the conventional LC oscillator's jitter performance is good, integrated LC oscillators show a degredation in their jitter performance. If researchers search for alternatives to integrated LC oscillators, the ring oscillator could find its place in applications where moderate jitter performance, high levels of integration with low die real estate, and a wide tuning range are required.

To that end, this thesis sets out to examine the physical parameters that affect the jitter in ring oscillators. Specific parameters that affect jitter will be identified and these will be incorporated into an experimental chip that will verify experimentally the relationship between theory and practice.

1.2 Organization

This paper is divided into six chapters. This chapter describes the goals and motivation of this thesis.

Chapter 2 introduces voltage-controlled oscillators (VCOs) and describes the differences between different types of oscillators, along with their relative advantages and disadvantages.

Chapter 3 will discuss the concepts of jitter and phase noise. It will explain the differences between jitter and phase noise, and discuss how they are measured and quantified. The figures of merit K and N_1 which are used as measures of jitter and phase noise will be introduced as well.

Chapter 4 begins by developing a timing model for the inverter delay stage in the ring oscillator and from there develops a relationship between the time-domain figure-of-merit K and the physical parameters of the transistors in the ring. Out of this analysis a plan will be developed that will verify through experiment how well the theoretical noise model holds true.

Chapter 5 will describe the silicon implementation of the experiment followed by a discussion of the methods used to measure the jitter of the VCOs. The results of the experiment are presented and discussed.

Chapter 6 is the conclusion and it presents future research directions that can be developed on the basis of the results of this work.

Chapter 2 Voltage-Controlled Oscillators

2.1 Voltage Controlled Oscillators

Voltage-controlled oscillators (VCOs) are a means for the generation of periodic signals in circuits. Changing an applied control voltage varies the frequency output of a VCO. There are a few different types of circuits that make up the family of voltage-controlled oscillators. These can be broadly classified into harmonic oscillators, relaxation or multivibrator oscillators, and ring oscillators.

2.1.1 Harmonic Oscillators

Harmonic oscillators are characterized by an equivalence to two energy storage elements operating in resonance to produce a periodic output signal. The resonant element is typically either a LC tank or a quartz crystal. These types of oscillators are known to have excellent jitter performance [10]. The drawback that these oscillators suffer from is the fact that the LC tank and crystals have to be off-chip. This defeats the purpose of trying to develop integrated VCOs. Nowadays, integrated inductors are commonly used in designs but they consume large amounts of die real estate. Even then, these inductors

typically suffer from low Q values due to resistive losses. This has the effect of degrading the jitter performance of these oscillators.

The oscillation frequency of LC oscillators is dependent upon the inductance and capacitance of the resonant elements according to Equation (2.1).

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

Integrated LC oscillators are usually tuned using voltage-controlled MOSFET capacitors. These MOSFET capacitors have a limited capacitance range, typically controllable over a range of 2:1 [12]. A capacitance range of 2:1 means that integrated LC oscillators can only be tuned over a range of $\sqrt{2}$:1. This narrow tunable range is a disadvantage to using these LC oscillators.

2.1.2 Relaxation Oscillators

Relaxation oscillators, also known as multivibrators, are characterized by a single energy storage element together with circuitry that senses the state of the element and controls its excitation to give a periodic output signal [10]. The jitter performance of this type of oscillator is not as good as that of the harmonic oscillator but design techniques are available for improving the jitter [10]. This type of oscillator has been fully integrated in some clock recovery applications [10].

2.1.3 Ring Oscillators

The ring oscillator is a fully integrable VCO that depends on a series of delay stages and an inversion in the signal path to produce the desired periodic output signal. Ring oscillators come in both single-ended and differential flavors. Differential ring oscillators require at least two delay stages and a wire inversion to function. Single-ended ring oscillators require an odd number of stages in the ring to oscillate. While ring oscillators suffer from poor jitter performance relative to the harmonic and relaxation oscillators, their prime advantages are their full integrability into a die and their wide operating frequency range.

Table 1 below summarizes the relative merits of each of the oscillators presented.

	Harmonic (with integrated L)	**Relaxation**	**Single-ended Ring**
Die Area	High	Fair	Lowest
Jitter Performance	Excellent	Good	Fair
Supply Rejection	Good	Good	Poor
Tuning Range	Narrow	Narrow	Very Wide
Integrability	Poor	Fair	Good

Table 1. Summary of oscillator performance.

2.2 Choosing a VCO for this Work

The choice of VCO used for this work was the single-ended ring oscillator. The LC oscillator has received a great deal of attention because of its good jitter performance. Not much research has been performed into determining how the jitter performance of the ring oscillator could be improved upon. Despite the moderate jitter performance of this type of oscillator, it exhibits great potential in certain applications where the full integrability and wide tuning range is more important than moderate jitter performance. In addition, the single-ended ring oscillator's jitter is independent of the number of stages in the ring [4, 8, 9, 10]. Choosing to work with the single-ended ring oscillator provides fertile ground for this work and any work that might follow it.

2.2.1 The Single-Ended CMOS Ring Oscillator

The type of oscillator used in this work is a single-ended ring oscillator of the type shown in Figure 2.1.

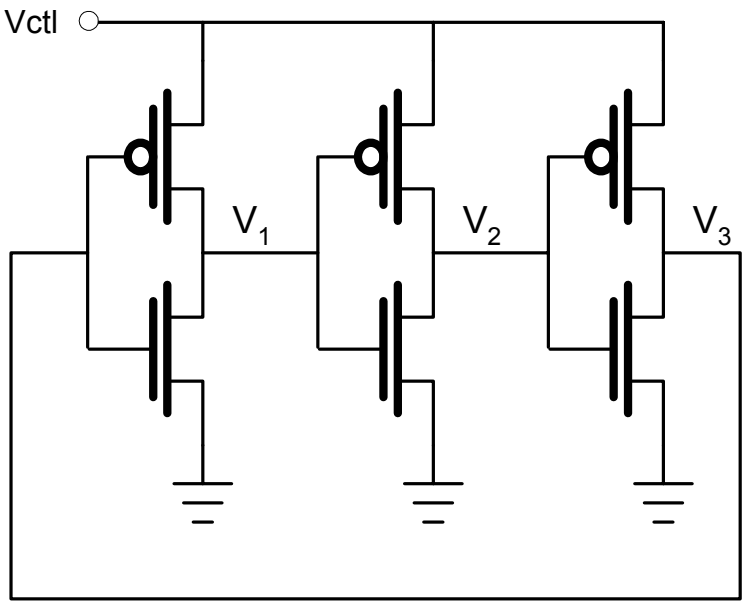

Figure 2.1. Schematic of a 3-stage single-ended ring oscillator.

This type of inverter requires the use of an odd number of delay cells, with a minimum number of three. The circuit has only one stable state (where all the outputs are at $V_{CTL}/2$) but that is not achievable in real implementations because thermal noise in the transistors is enough to tip the balance such that the outputs are driven out of that stable state and into an oscillatory state.

The timing diagram of the waveforms in a 3-stage ring oscillator is shown in Figure 2.2.

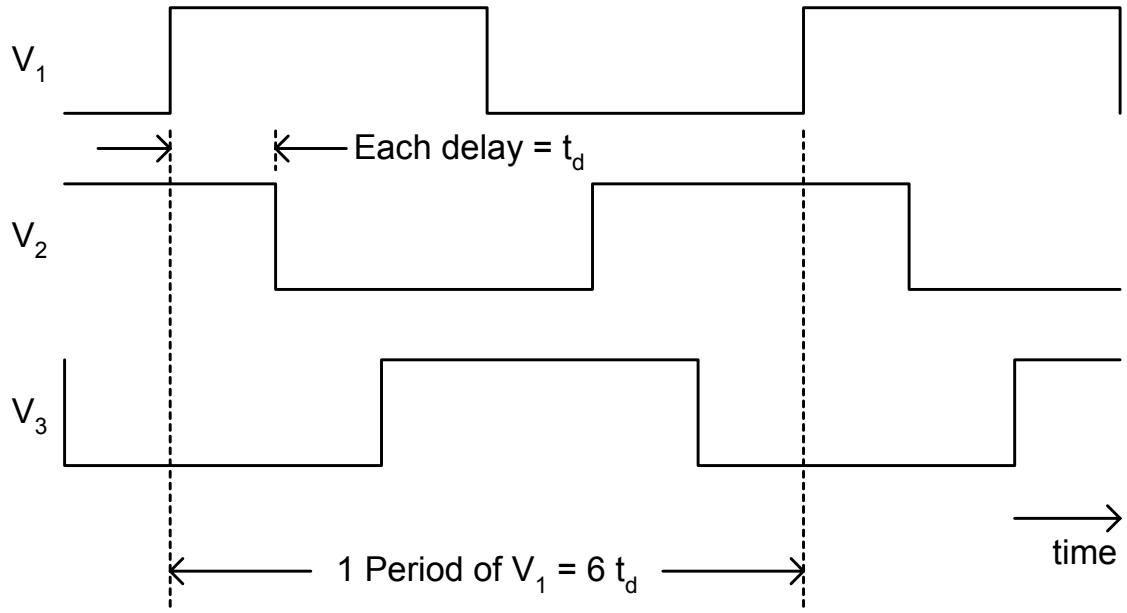

Figure 2.2. Timing diagram of a 3-stage ring oscillator.

The oscillation frequency of this type of ring oscillator can be generalized in terms of the number of stages N and propagation delay t_d according to Equation (2.2).

$$f = \frac{1}{T} = \frac{1}{2 \cdot N \cdot t_d} \tag{2.2}$$

To ensure the equal rise and fall times necessary to make all delays equal to t_d, Equation (2.3) must be satisfied [14].

$$\mu_p \cdot C_{ox} \cdot \frac{W_p}{L_p} = \mu_n \cdot C_{ox} \cdot \frac{W_n}{L_n} \tag{2.3}$$

μ_n and μ_p are the mobility of the n and p material while C_{ox} is the oxide capacitance per square. W and L with the appropriate subscripts denote the widths and lengths of the n and p transistors in each inverter.

2.3 Conclusion

In this chapter, various VCOs have been introduced and their relative merits discussed. Based on its research potential, the choice of which type of VCO to use was narrowed down to the single-ended ring oscillator. The next chapter will discuss the concept of jitter and explain how it is quantified and measured.

Chapter 3 Jitter and Phase Noise

3.1 Jitter versus Phase Noise

The terms jitter and phase noise are often used loosely and interchangeably. This is somewhat acceptable as both describe the same phenomenon. The difference is that jitter is used when referring to the phenomenon in the time-domain while phase noise is used to describe it in the frequency-domain. In this chapter, jitter and phase noise will be defined in the time and frequency-domains respectively.

3.2 Jitter

All timing devices suffer from a phenomenon known as jitter. Jitter is the word used to describe the variation of an oscillator's period from its ideal. An ideal oscillator will have periods that are exactly the same for every cycle. This is shown in the left half of Figure 3.1.

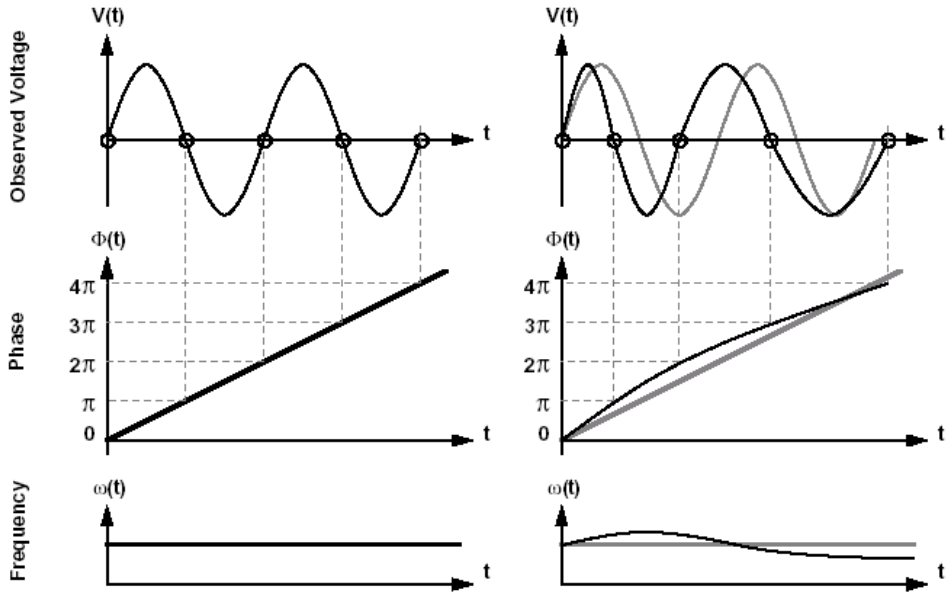

Figure 3.1. Time-Domain Representation of Jitter

Notice that the phase increases with a constant slope. Note also that because frequency is the derivative of phase, the frequency is constant. The right half of Figure 3.1 shows an oscillator that has a jittery output. The oscillator's periods vary from cycle to cycle, with some periods longer and some periods shorter than the ideal period. Notice that the phase changes and wanders above and below the ideal slope of the perfect oscillator. This translates to a modulation of the frequency around the fundamental as shown in the bottom of Figure 3.1.

3.2.1 Measuring Jitter

Jitter, being a time-domain characteristic, should be measured in the time-domain. Consider the circuit shown in Figure 3.2 where the noise is dominated by a white noise source at the input of the open loop VCO.

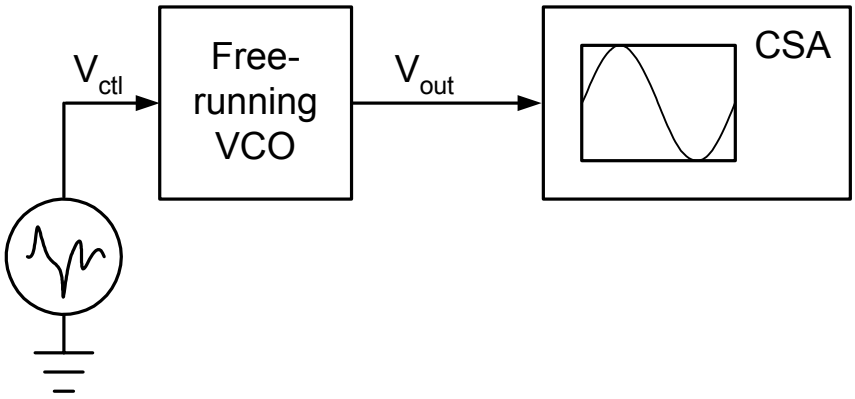

Figure 3.2. Test setup for measuring jitter in the time-domain.

In this setup, the output of the white noise-dominated free-running VCO is fed into a communications signal analyzer. The CSA has the ability to trigger off an edge and then wait for a given period of time ΔT_n before sampling the zero crossing occurring at that time. The longer the time delay between the triggered edge and the sample, the greater the standard deviation in the zero crossing times. This is illustrated in Figure 3.3.

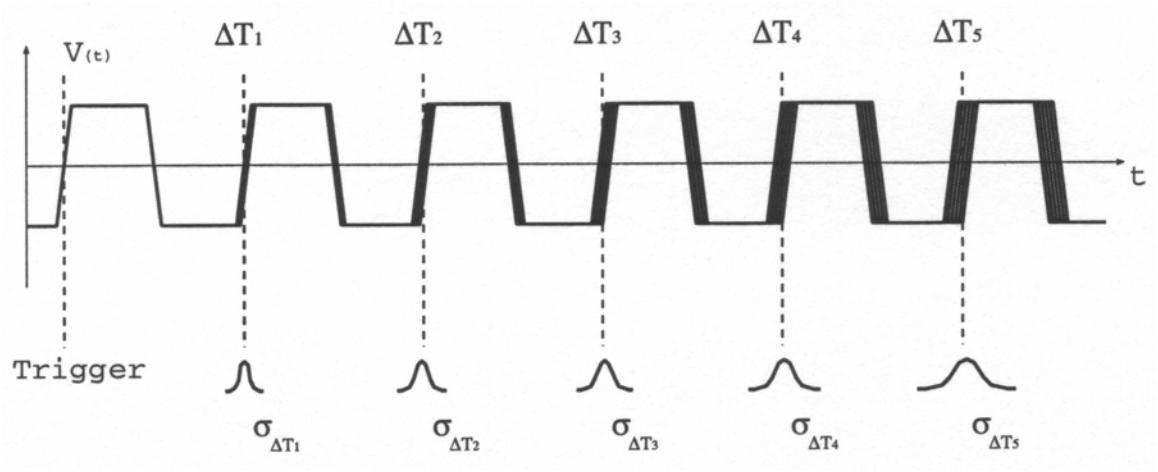

Figure 3.3. Zero crossing uncertainty with increasing time delays.

This increase in the standard deviation is because in the open loop VCO, timing errors are not corrected and persist for an infinite amount of time. This is known as jitter accumulation. Figure 3.4 illustrates what a plot of the standard deviation versus delay time would look like [10]. The axes shown in Figure 3.4 are on a logarithmic scale.

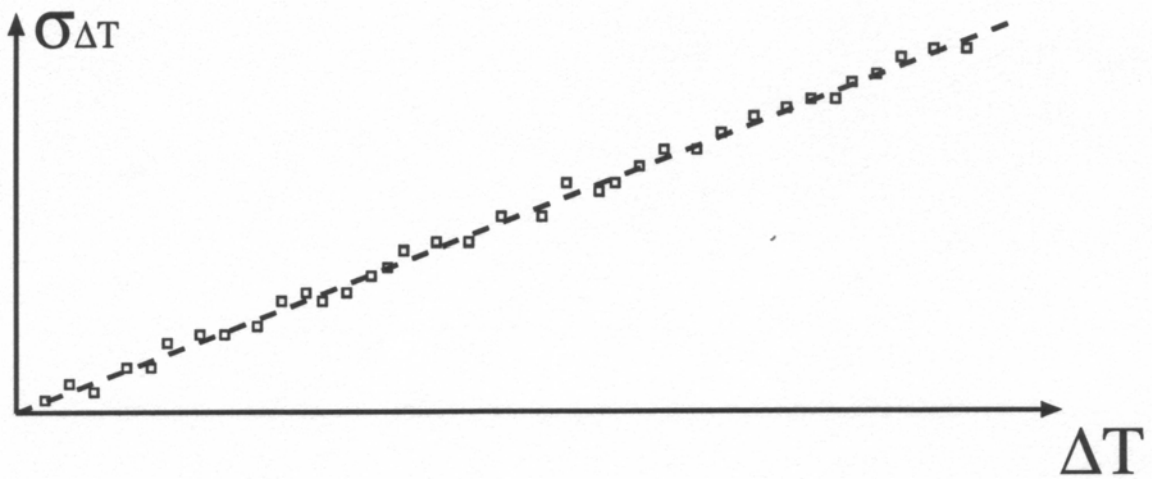

Figure 3.4. Plot of zero crossing standard deviation versus delay.

It has been shown that the standard deviation and delay are related by Equation (3.1) [3, 10].

$$\sigma_{\Delta T}(\Delta T) \approx \kappa\sqrt{\Delta T} \tag{3.1}$$

The slope of the plot in Figure 3.4 is therefore 1/2. A larger value of K would shift the line up along the vertical axis and represent a larger degree of uncertainty in the zero crossing times for a given time delay.

The reason why the standard deviation increases with the root of the time delay is because the uncertainty introduced with each clock edge is an independent event. These uncorrelated errors therefore add in a root sum squared fashion.

3.2.2 K As A Time Domain Figure Of Merit For Describing Jitter.

If we consider an oscillator to be dominated by uncorrelated white noise, then K can be used as a time-domain figure-of-merit for describing the jitter in an oscillator.

3.3 Phase Noise

Having described jitter in the time-domain, we shall look at phase noise. In the frequency-domain, a perfect oscillator will manifest itself as an impulse at the fundamental frequency as shown in the left-most spectrum in Figure 3.5.

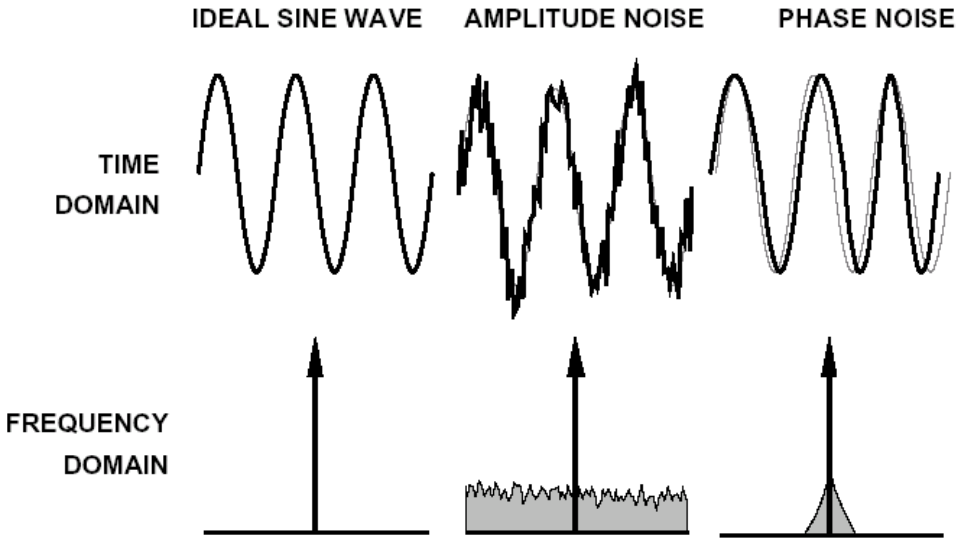

Figure 3.5. Frequency-Domain Representation of Jitter

If a perfect oscillator is acted upon by broadband amplitude noise, the time-domain signal will be a noisy sinusoid as shown in the middle of Figure 3.5. In the frequency-domain this translates to a raising of the noise floor around the impulse. In the time-domain, the most natural way to remove the broadband noise would be to use a bandpass filter. This would clean up most of the amplitude noise at frequencies above and below the fundamental but the bandpass filter will not be able to remove the residual zero crossing errors caused by the noise which reside at frequencies close to the fundamental. These zero crossing errors give rise to jitter. In the frequency-domain this translates to a residual phase noise skirt that remains around the base of the fundamental.

3.3.1 Phase Noise is Akin to Modulation in the Frequency Domain

The question that arises is often one of how the phase noise skirt comes about. To answer that question, think of phase noise as modulation in the frequency-domain. Figure 3.6 shows how a phase-modulated waveform is actually composed of a perfect sine wave in-phase (I) and an amplitude modulated quadrature (Q) signal.

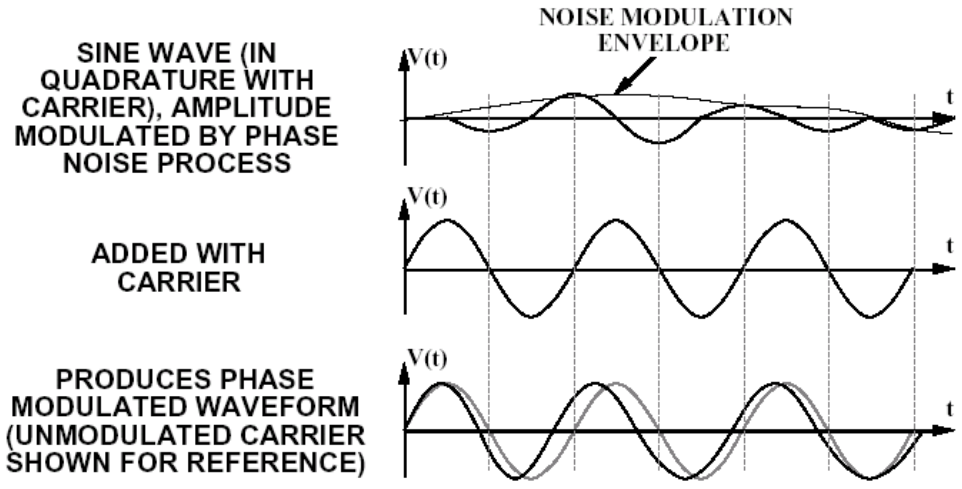

Figure 3.6. Decomposition of Phase-Modulated Waveform into In-phase Quadrature Components.

The envelope of the Q signal is representative of the phase error and when the Fourier transform of the phase error $\Phi(t)$ is taken it will have a spectrum centered around zero in the frequency-domain. This is shown at the bottom in Figure 3.7. The spectrum of the phase-modulated carrier is the sum of the impulse at the fundamental frequency f_c and the

baseband modulating signal's spectrum centered around f_c. The simple addition of the power spectral densities is possible because the I and Q signals are uncorrelated.

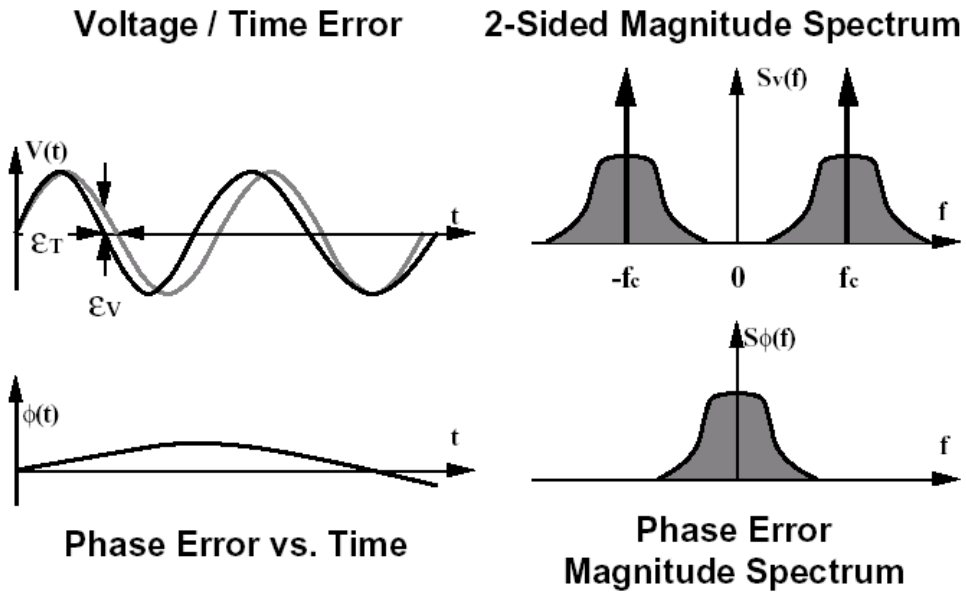

Figure 3.7. Phase Noise as Modulation in the Frequency Domain.

This is a useful finding because it means that the power spectral density of the phase error directly translates to the shape of the phase noise skirt. Thus, we can extract information about the phase error directly from the shape of the phase noise skirt around the fundamental.

3.3.2 Measuring Phase Noise

If it is assumed that the noise in an oscillator is white noise dominated and if all the various noise sources are referred to the control voltage input of the VCO as shown in Figure 3.8, then the power spectral density of the phase noise will exhibit a $1/f^2$ behavior [3]. This $1/f^2$ behavior is illustrated in Figure 3.9.

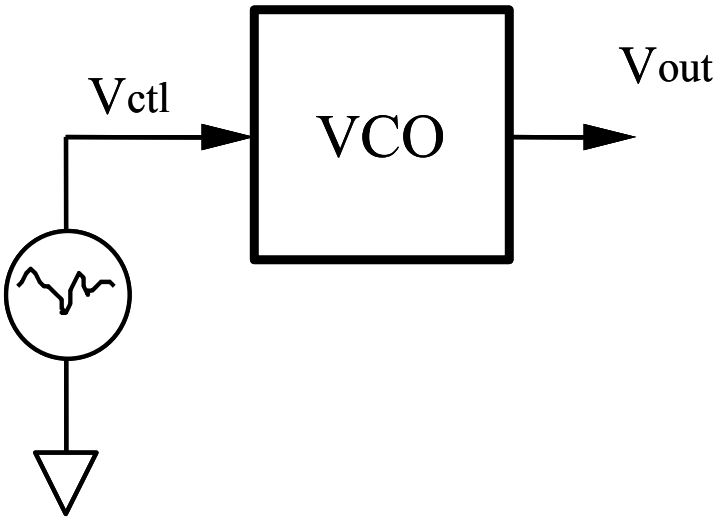

Figure 3.8. Open loop VCO with input referred white noise.

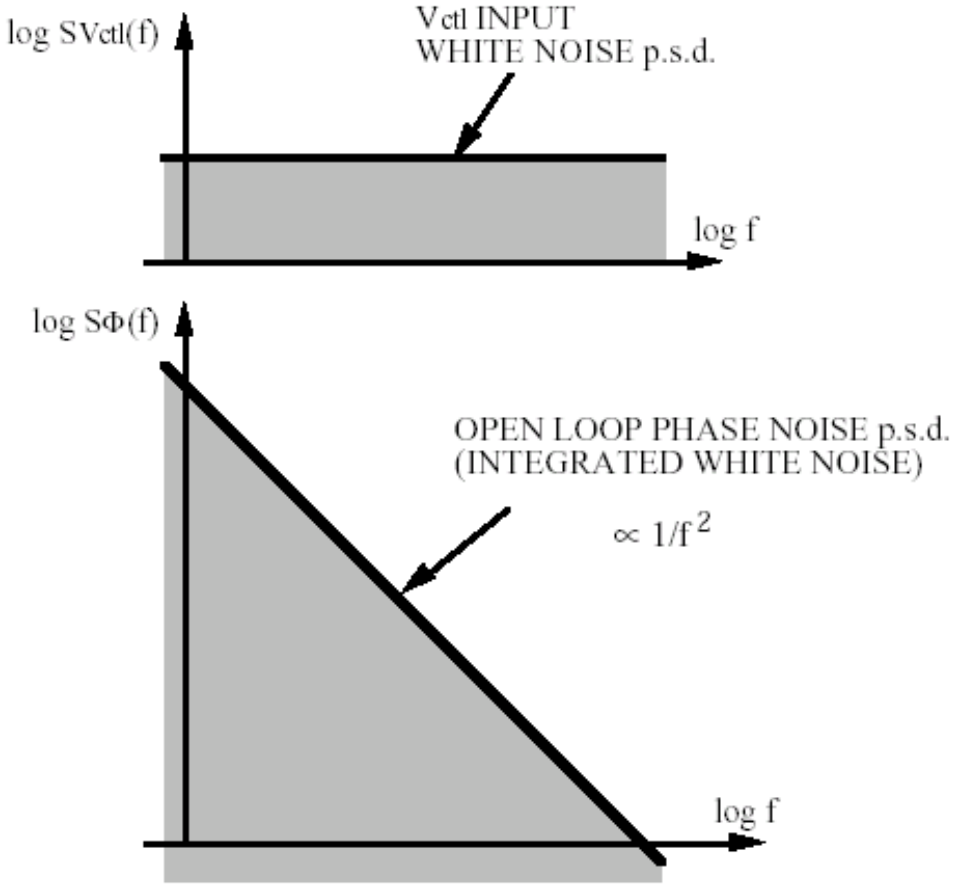

Figure 3.9. Phase noise PSD with white noise at VCO input [9].

A plot of the frequency spectrum of an oscillator output is shown in Figure 3.10. Notice that it is not very easy to detect the $1/f^2$ region. This is because of the linear horizontal scale that is used in this plot. Figure 3.11 shows an example of the phase noise plot versus the offset frequency from the carrier. In this case, the horizontal axis shows the offset frequency on a logarithmic scale. With this scale, the region of $1/f^2$ behavior becomes obvious and is highlighted.

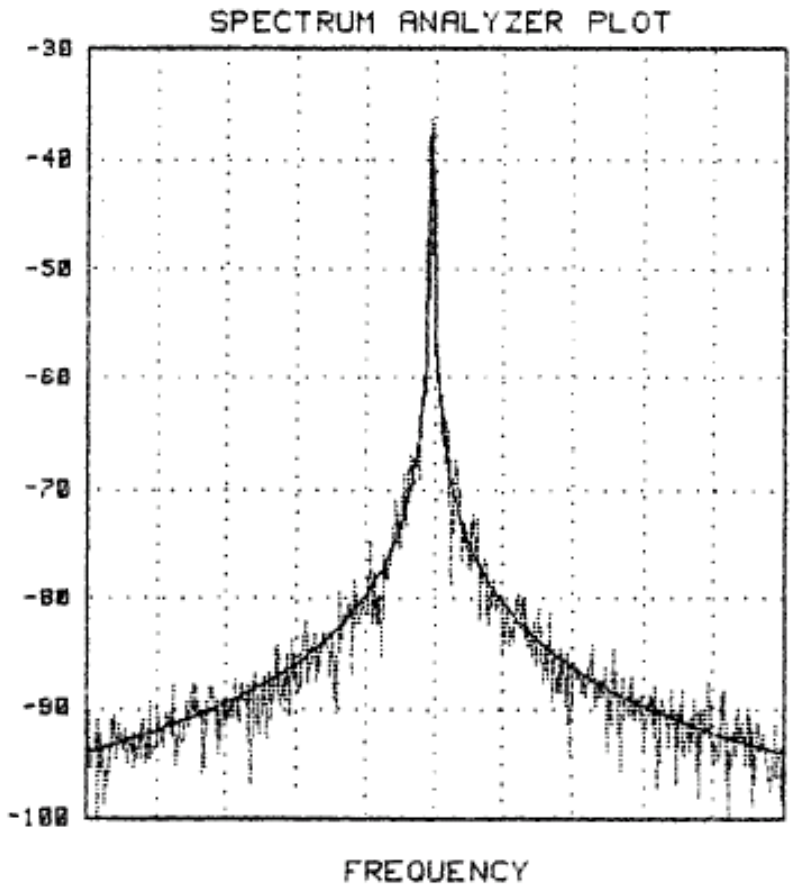

Figure 3.10. Spectrum analyzer plot of VCO output. Note linear horizontal scale.

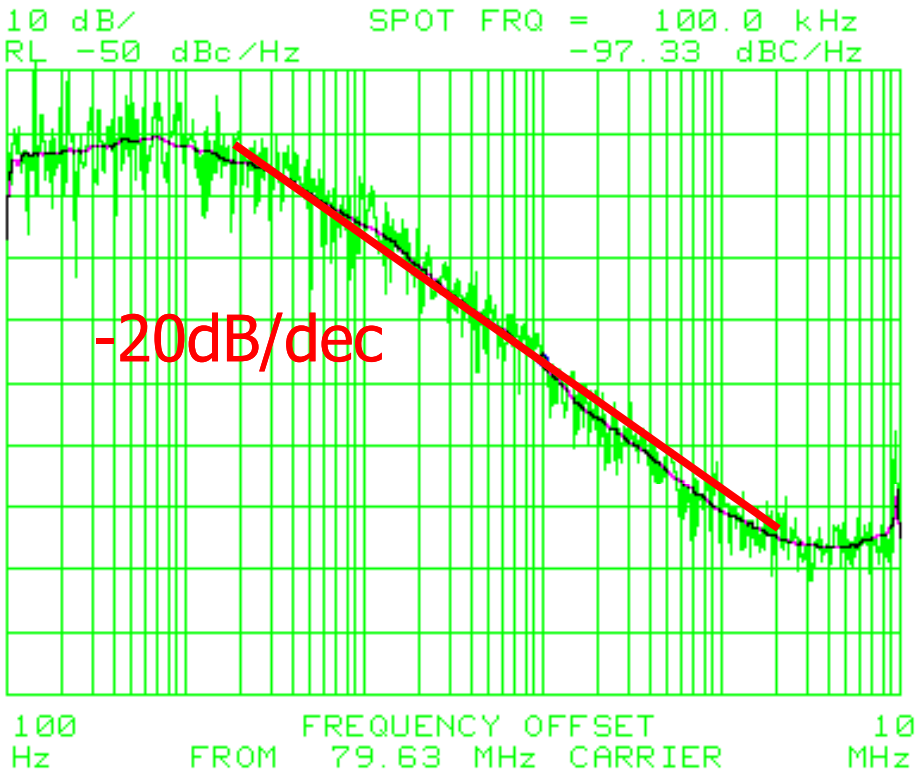

Figure 3.11. Spectrum analyzer plot of VCO phase noise versus offset frequency from carrier. Note logarithmic horizontal scale.

Within this region of $1/f^2$ behavior, the following relationship is true [3, 10].

$$S_{\phi OL}(f) \approx \frac{N_1}{f^2} \tag{3.2}$$

Just like K, N1 can be used as a figure-of-merit that describes the quality of an oscillator. Like K, the higher the value of N1 the noisier the oscillator is.

3.4 Relating K and N1

K and N1 are related through Equation (3.3) where f_o is the frequency of oscillation [3, 9, 10].

$$\kappa = \frac{\sqrt{N_1}}{f_o} \tag{3.3}$$

This result will allow us to move between the time and frequency-domains easily when making measurements. This gives the freedom to make measurements in the domain that is easiest and most convenient.

3.5 Sine Waves and Square Waves

So far the discussion has centered on sinusoidal signals. If the signals of interest are square in nature, the same rules apply. The left of Figure 3.12 shows the spectrum of a single sinusoid. It is an impulse at the fundamental frequency. If the sinusoid on the left is fed through a limiter and made square, the spectrum is composed of the fundamental and the odd harmonics of the fundamental.

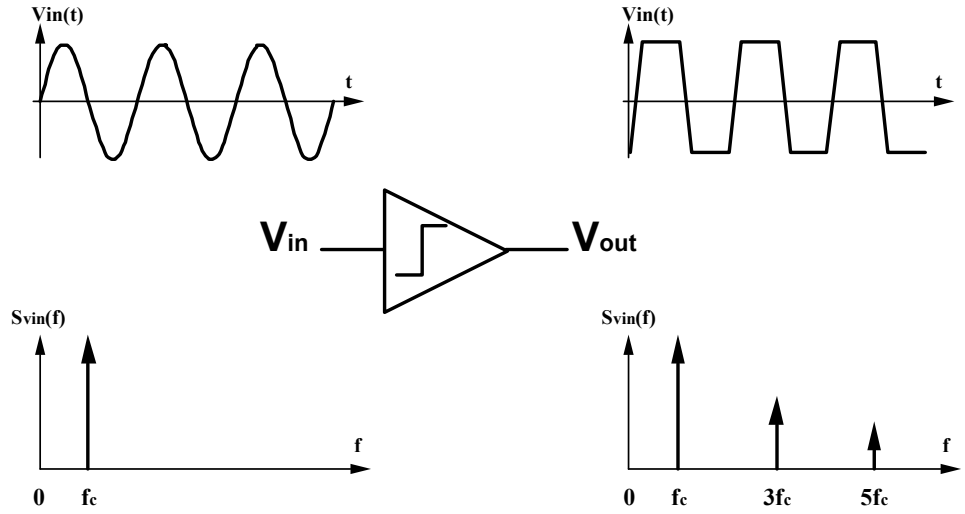

Figure 3.12. Spectral Composition of Sine and Square Waves.

Figure 3.13 shows that when a phase modulated sine wave is amplified such that it becomes a square (rectangular) wave, the phase error information is retained in the zero crossing times of the transitions. The frequency spectrum of the phase modulated square wave is simply the regular square wave spectrum with the phase noise skirt added to each impulse in the spectrum.

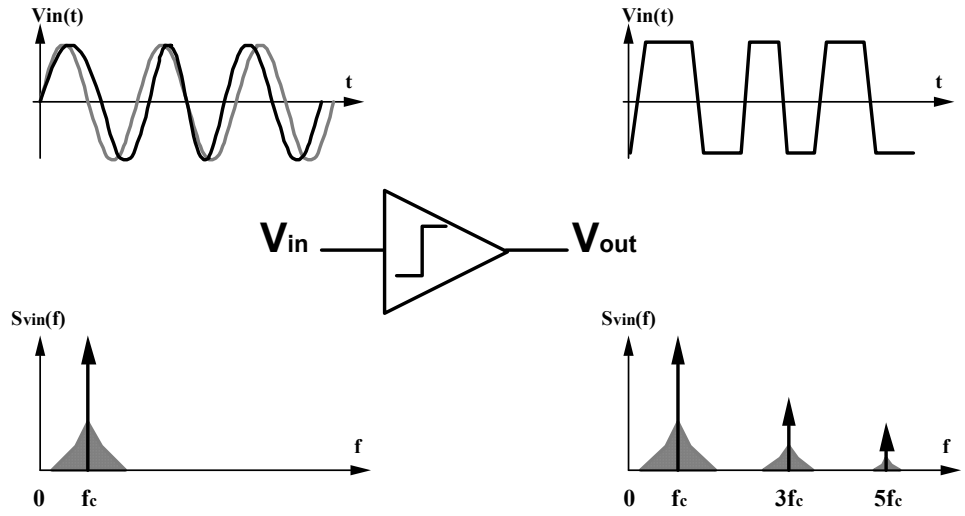

Figure 3.13. Phase noise skirts around fundamental of sine and square waves showing no change.

Thus, when analyzing the jitter of waveforms, whether sinusoidal or square, one only needs to look at the fundamental frequency to measure the phase noise.

3.6 Conclusion

In this chapter, the concepts of jitter and phase noise have been presented. The methods of identifying and measuring jitter and phase noise in a white noise-dominated environment have also been shown. In the next chapter, the jitter figure-of-merit K will be described as a function of MOSFET device parameters to see if the jitter in a ring oscillator can be reduced.

Chapter 4 Lowering the Jitter of Single-Ended Ring Oscillators

With an understanding of jitter and phase noise and how to quantify these parameters using the figures of merit K and N_1, the next task is to examine the equations that govern the noise in single-ended ring oscillators and to see if there are any parameters that can be modified to reduce the jitter in the oscillator.

4.1 Assumptions

The first step in the process is to define the assumptions that will be made in the analysis. It will be assumed that:

- the conducting MOSFET will be considered to be in saturation;
- the gate capacitance of next stage dominates load capacitance of previous stage;
- the square-law model will be used to describe MOSFET behavior;
- thermal noise in the conducting channel dominates the noise process; and
- the device threshold voltage Vt for all MOSFETs will be 0V.

4.2 Gate Delay: A Simple Model

There are many different models that describe the delay of a MOSFET inverter [2, 13] but in this work, the gate delay model will be simplified with the help of the assumptions that have been laid out. Figure 4.1 illustrates the model that will be used to describe the delay of each inverter stage.

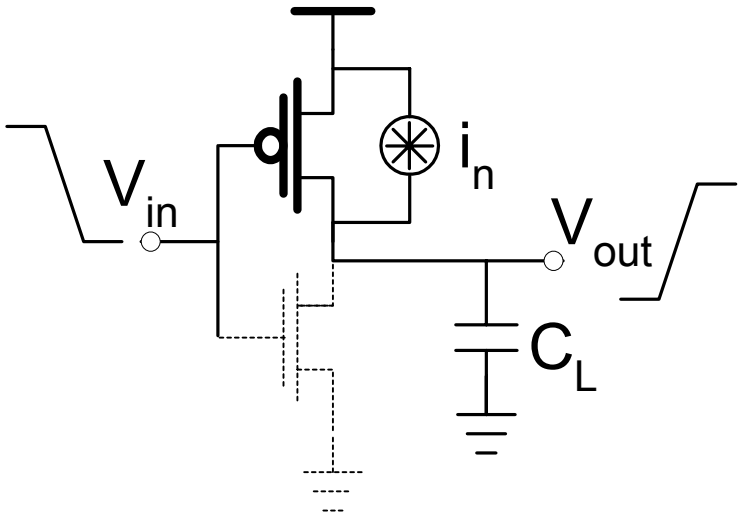

Figure 4.1. Simplified model illustrating inverter delay.

In this example, the input is falling from high to low, which will turn the PMOS transistor on. The first assumption allows us to treat the PMOS transistor as a constant current source, which allows us to model the output Vout as a linearly rising voltage with respect to time. This is shown in Figure 4.2.

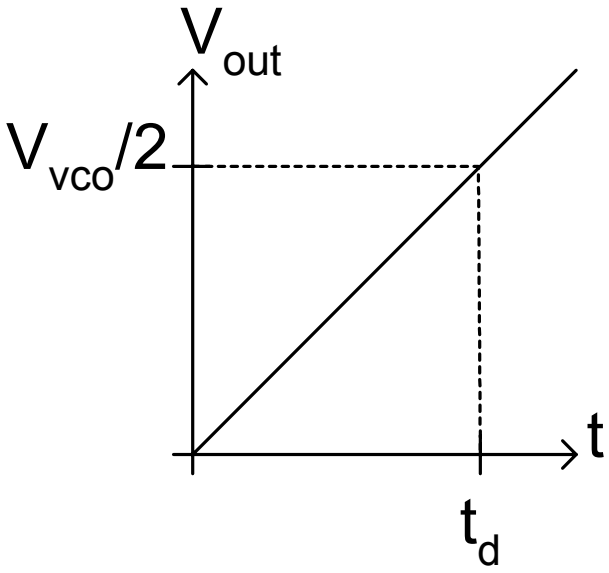

Figure 4.2. Rise-time of inverter delay stage.

We shall now develop an expression for the delay in terms of MOSFET device parameters. The current charging a capacitor can be described by Equation (4.1).

$$I = C \cdot \frac{dV}{dt} = C \cdot \frac{V_{VCO}}{2} \cdot \frac{1}{t_d} \tag{4.1}$$

From this the propagation delay of the inverter can be expressed as:

$$t_d = \frac{C \cdot V_{VCO}}{2 \cdot I}. \tag{4.2}$$

From a previous chapter we found that the frequency of oscillation for a N-stage ring oscillator is

$$f = \frac{1}{T} = \frac{1}{2 \cdot N \cdot t_d} \tag{4.3}$$

The square-law model for the drain current in a MOSFET in saturation is given in Equation (4.4) [7].

$$I = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{VCO}{}^2 \tag{4.4}$$

Combining (4.2), (4.3) and (4.4) gives us a new expression for the frequency of oscillation. This is expressed in Equation (4.5)

$$f = \frac{\mu \cdot V_{VCO}}{L^2 \cdot N} \tag{4.5}$$

Process technologists are constantly striving to reduce the minimum feature size of transistors. Equation (4.5) shows clearly why that is so. The switching speed increases quadratically with a decrease in feature size. The equation also indicates that for a given power dissipation (V_{VCO}), the frequency of oscillation is inversely proportional to the number of stages in the ring. Note also that frequency is independent of device width.

4.3 Noise in the MOSFET

The work in [3] has shown that the assumption that thermal noise in the channel dominates is a valid one. [3] has also shown that

$$\kappa = \frac{i_n}{I} \cdot \frac{1}{\sqrt{2}} \tag{4.6}$$

where i_n is the current noise density of the thermal noise in the conducting channel as shown in Figure 4.1.

The current noise density of thermal noise in the conducting channel of a MOSFET is given by Equation (4.7)

$$i_n = \sqrt{\frac{8}{3} \cdot kT \cdot g_m} \tag{4.7}$$

and the transconductance g_m is given by Equation (4.8)

$$g_m = \frac{2I}{V_{VCO}} \tag{4.8}$$

Combining (4.7) and (4.8) produces a new expression for the current noise density. This is expressed in Equation (4.9).

$$i_n = \sqrt{\frac{8}{3} \cdot kT \cdot \frac{2I}{V_{VCO}}} \tag{4.9}$$

Combining Equations (4.6), (4.9) and (4.4) yields Equation (4.10) that indicates that if the power in a ring oscillator (given by the IV product) is increased K will decrease.

$$\kappa = \sqrt{\frac{8}{3} \cdot kT} \cdot \sqrt{\frac{1}{I \cdot V_{VCO}}} \tag{4.10}$$

This discovery is an important one because it indicates that the jitter in the oscillator can be improved upon simply by increasing the amount of power consumed. This agrees with the work in [4]. It also indicates that the noise energy in the oscillator is a constant at a given temperature through the kT term in the equation.

Replacing the current term I in Equation (4.10) with the square-law drain current expression in Equation (4.4) gives way to Equation (4.11).

$$\kappa = \sqrt{\frac{8}{3} \cdot kT} \cdot \sqrt{\frac{1}{\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{VCO}^{\ 3}}} \tag{4.11}$$

Equation (4.11) expresses K as a function of design parameters that can be used by designers to achieve lower jitter. Choosing a process that has higher mobility and gate oxide capacitance can reduce jitter while increasing the device width can also achieve that goal.

4.4 The Experiment

From Equation (4.11), it can be seen that there are only two parameters that can be changed once a process is chosen. These are transistor gate width and length. It was

decided that the gate length should be kept constant while the width is varied. The decision to keep the length to the minimum was driven by the desire to push the speed of the VCO to as high as the process would allow. To design the gate lengths longer would defeat the purpose of using an expensive 0.35μm process. Widening the widths is an acceptable direction to take in an effort to improve the jitter performance of the ring oscillator because recall from Equation (4.5) that frequency is independent of width. Thus, we will not be sacrificing speed for lower jitter. For each width that is fabricated, the corresponding K value would then be determined to see how well the relationship in Equation (4.11) holds true.

Chapter 5 Verification, Testing and Results

5.1 Test Platform

Having decided that the widths of the transistors would be varied, a test chip needed to be fabricated. This chip would allow us to verify experimentally the theoretical results that were found in the last chapter.

The process used was a TSMC 0.35μm 4-metal 1-poly CMOS process. Layout was performed using the Cadence suite of design and layout tools.

The chip was designed with four VCOs of different widths. The baseline NMOS VCO has a width of 12um while the rest are 2, 4 and 8 times that width. This gives rise to transistors with widths of 12, 24, 48 and 96μm. All transistor lengths are of the minimum feature size of 0.4μm.

5.1.1 Chip Micrograph

A micrograph of the chip is shown in Figure 5.1. The four VCOs are placed such that there is one on each side of the chip.

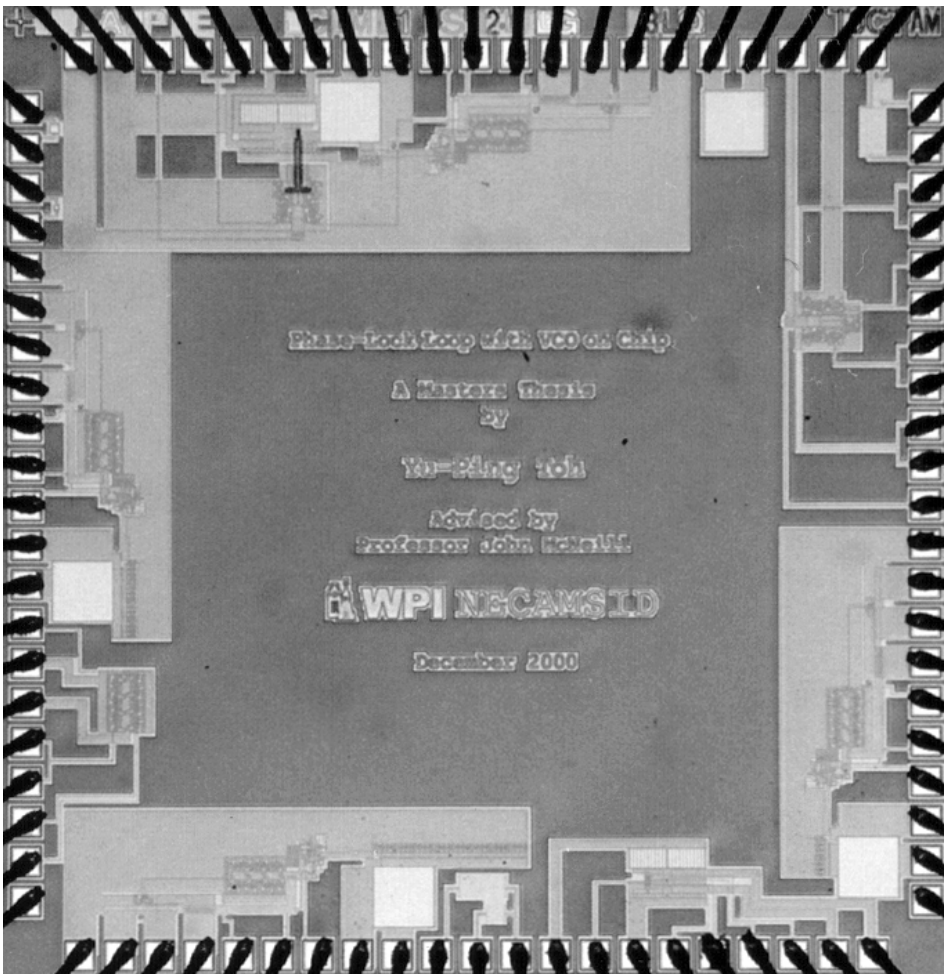

Figure 5.1. Chip micrograph.

5.2 Taking Measurements

It was found in Chapter 3 that the jitter performance of oscillators can be measured in both the time and frequency-domain. If K is obtained in the time-domain, it is easy to convert that value into the N_1 frequency-domain figure-of-merit. Which method to use is then dependent on the availability of equipment and the ease with which the measurements can be made. In this case, it was the availability of equipment that drove the decision to make the measurements in the frequency-domain

5.3 Defining the Test Parameters

Recall the relationship between K and the MOSFET device parameters. This is expressed in equation (5.1).

$$\kappa = \sqrt{\frac{8}{3} \cdot kT} \cdot \sqrt{\frac{1}{\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot {V_{VCO}}^3}} \tag{5.1}$$

For a given VCO voltage V_{VCO}, an oscillator with a wider transistor should exhibit lower jitter.

Unfortunately, it is not possible to probe the actual voltage across the VCO. This node is highly sensitive to any noise and to put a probe to it would upset the measurements. An

alternative method of determining the VCO voltage is to use the relationship between the oscillation frequency and V_{VCO}. This is shown in Equation (5.2).

$$f = \frac{\mu \cdot V_{VCO}}{L^2 \cdot N} \tag{5.2}$$

The tests will be redefined such that the jitter figure-of-merit K of each VCO will be measured against oscillation frequency. According to Equation (5.2) the oscillation frequency is proportional to V_{VCO}. Thus, the oscillation frequency can be used as an indicator of power.

A set of frequencies that exercises the useful range of frequencies of the VCO is developed and the jitter of each VCO will be measured at these frequencies.

5.4 Experimental Procedure

Determining K requires an understanding of the shape of the phase noise skirt. There is a region in which the phase noise skirt exhibits a $1/f^3$ trend (due to 1/f noise being upconverted around the carrier), followed by a $1/f^2$ region (due to white noise at the input), which then transitions into a flat region (noise floor of spectrum analyzer).

The measurement of K hinges on the relationships

$$S_\phi(f) = \frac{N_1}{f^2} \tag{5.3}$$

and

$$K = \frac{\sqrt{N_1}}{f_o} \tag{5.4}$$

These relationships hold true only over the $1/f^2$ region of the phase noise skirt. Within that range, for a given oscillator operating at a fixed oscillation frequency N_1 (and subsequently K) should be a constant. If S_ϕ does not fall off as $1/f^2$ then N_1 will not be constant.

Therefore, when determining K, N_1 must be measured over a wide range of offset frequencies and a region over which the value of N_1 is constant must be identified. Within that range, more values of N_1 can be taken and the average of these values will serve as the N_1 value for the given oscillator at a given oscillation frequency. From that value of N_1, K can be easily calculated using the known oscillation frequency and Equation (5.4).

5.5 Measurement Setup

To allow the spectrum analyzer to lock onto the fundamental oscillation frequency and prevent wander in the oscillation frequency, an external phase lock loop was used. The PLL used was the Analog Devices ADF4110. As long as the loop bandwidth of the PLL is kept low (below the $1/f^2$ region), the phase noise plot at offset frequencies above the loop bandwidth of the PLL will look no different from phase noise plot taken from an

open loop VCO [9, 10]. With the HP phase noise measurement utility, plots like those in Figure 5.2 are obtained.

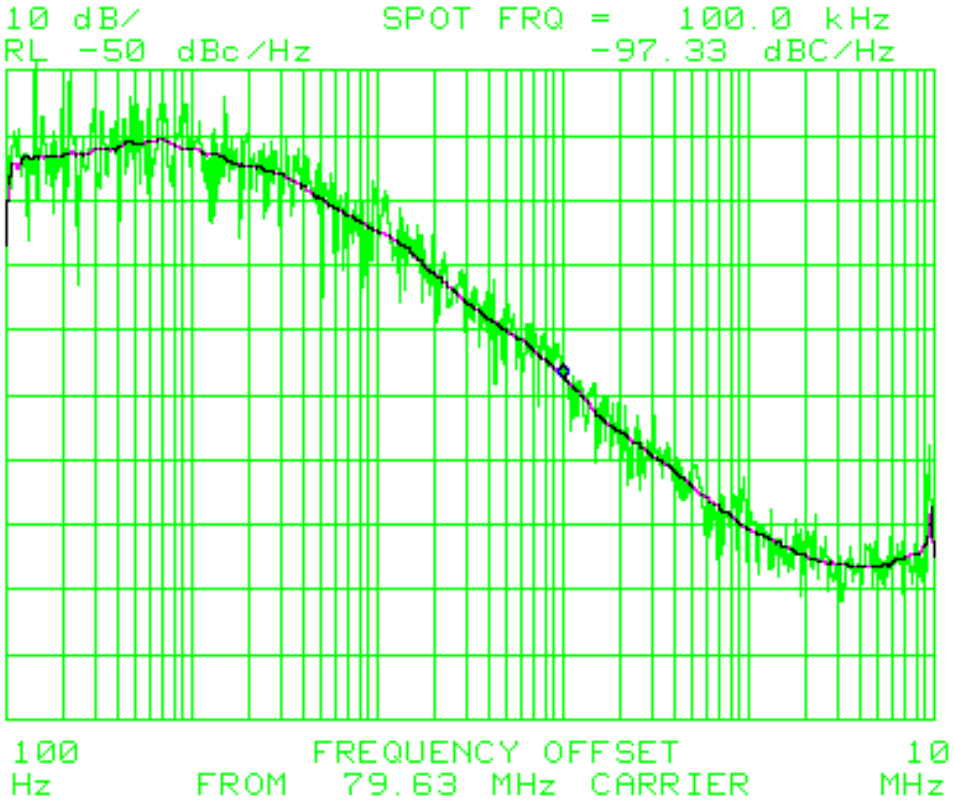

Figure 5.2. Example of phase noise plot from HP phase noise measurement utility.

Once a plot like the one in Figure 5.2 is obtained, there is a marker function that allows for the spot measurement of the phase noise. It is through the use of this function that data points for the plot in Figure 5.3 were obtained.

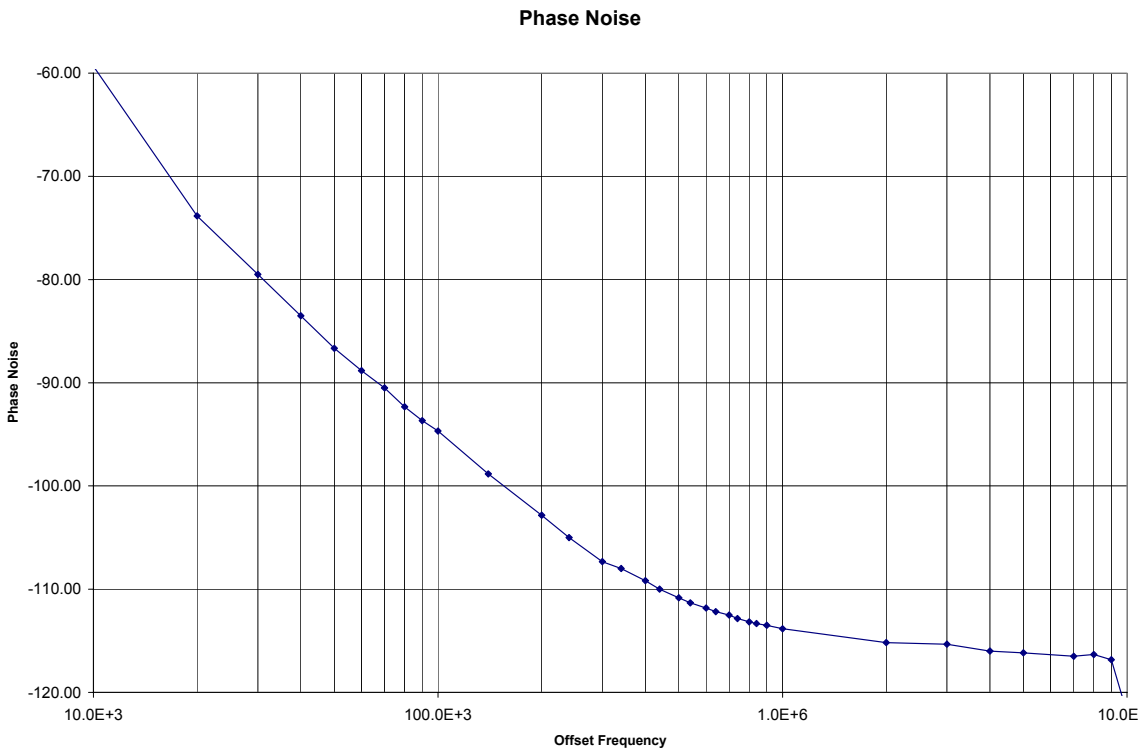

Figure 5.3. Phase noise plot for 1X VCO at 140MHz.

5.6 Measurement Example

The following example shows how the measurement was performed for the 1X VCO at an oscillation frequency of 140MHz.

Figure 5.3 shows the phase noise plot for the 1X VCO at 140MHz over a range of offset frequencies. The value of N_1 lies in the region where the phase noise rolls off with a –20dB/decade slope. This appears to happen roughly at a 400kHz offset. Obtaining an accurate measurement would be rather hard to discern visually so plots of N_1 and K are made and the corresponding values of N_1 and K are determined graphically.

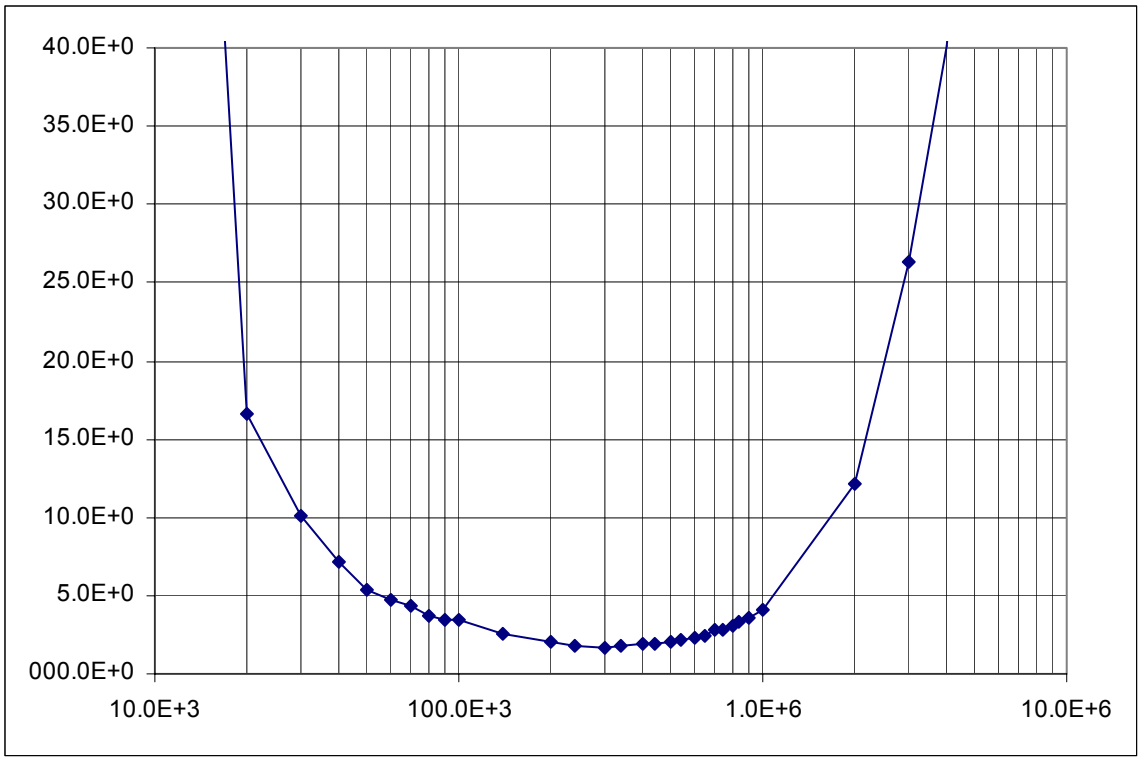

Figure 5.4. N_1 versus offset frequency from carrier.

It can be seen from the plot of N_1 that there is a region over which the value of N_1 is nearly constant. That is where the region over which the phase noise is exhibiting $1/f^2$

behavior. In this case the value of N_1 is 1.9. By relating N_1 and K through Equation (5.4), the corresponding value of K is found to be 9.97 n√sec. This occurs at an offset of about 400kHz.

This process was repeated for each VCO at each of the frequencies listed in Table 2 until the table was filled.

5.7 Results

Following the procedure outlined in the previous section, the table of K was filled and is shown below.

	1X VCO K	**2X VCO K**	**4X VCO K**	**8X VCO K**
VCO Frequency (MHz)	**12µm**	**24µm**	**48µm**	**96µm**
60	17.3E-9	11.9E-9	9.5E-9	7.0E-9
70	15.7E-9	10.5E-9	7.8E-9	6.9E-9
80	14.4E-9	8.9E-9	7.3E-9	6.2E-9
90	12.6E-9	8.1E-9	6.9E-9	5.4E-9

100	11.0E-9	7.8E-9	6.3E-9	5.0E-9
110	10.7E-9	7.5E-9	6.2E-9	4.8E-9

Table 2. Filled matrix of K values.

The data was then analyzed in two ways: K versus device width and K versus oscillation frequency (as an indicator of power).

5.7.1 K versus Device Width

The data in Table 2 was plotted in two ways. In the first plot, K is shown as a function of device width and this is shown in Figure 5.5. It can be seen that there is a definite decrease in K as device width increases.

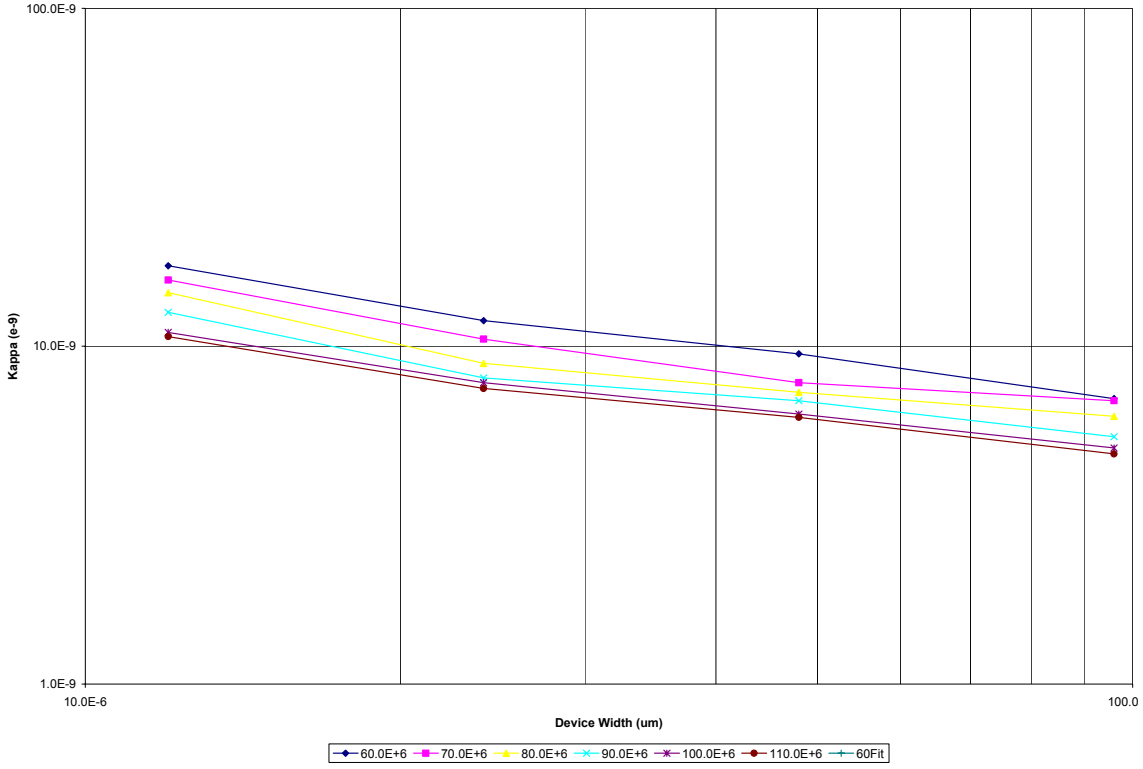

Figure 5.5. K versus device width.

The theory, as described in Equation (5.1) indicates that K should vary with device width according to Equation (5.5).

$$K \propto \frac{1}{\sqrt{W}} \tag{5.5}$$

Over the set of six frequencies, the slope of the K-W relationship was found to be between –0.37 and –0.42. This translates to an error of –15% to –25%. This shows reasonable correspondence with the theoretical predictions.

5.7.2 K versus Oscillation Frequency

In the case of K versus power, Equation (5.1) predicts the relationship shown in Equation (5.6).

$$K \propto V_{VCO}^{-3/2} \tag{5.6}$$

Combining Equation (5.6) with Equation (5.2) which states that V_{VCO} is directly related to frequency, yields the relationship in Equation (5.7).

$$K \propto f^{-3/2} \tag{5.7}$$

Plotting K versus f yields the plot shown in Figure 5.6. The predicted trend of decreasing K with increasing frequency is observed. Unfortunately the slopes of these trends stray far from the expected slopes of –1.5. The slopes extracted from the experiment range from –0.69 to –0.85. The most likely reason for this is the fact that we modeled the f-V_{VCO} relationship using the square-law model for the MOSFETs while the actual devices are short channel devices.

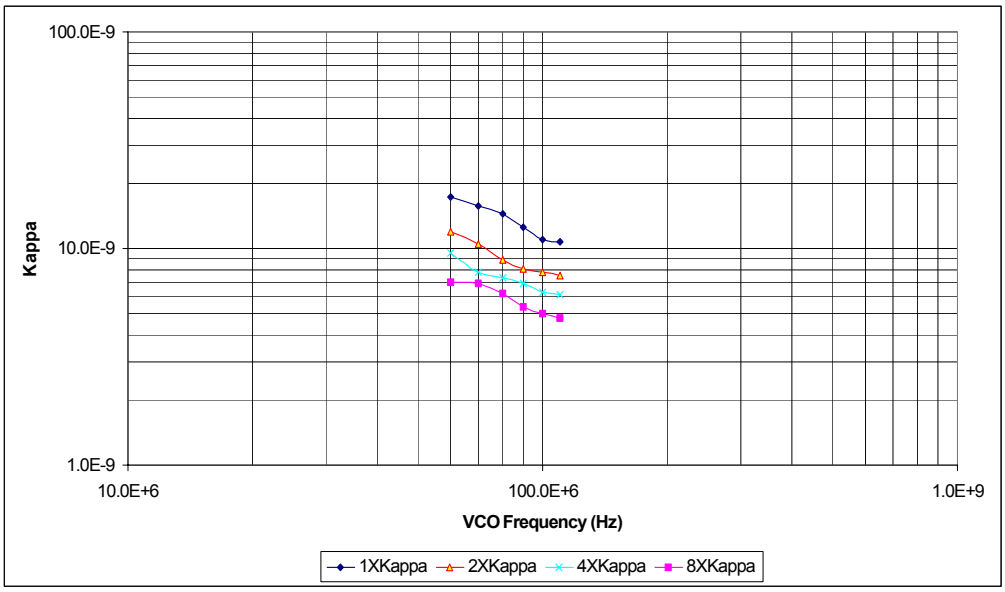

Figure 5.6. K versus VCO oscillation frequency.

5.8 Discussion of Results

The results of the K versus device width experiment give credence to the theoretical models that have been developed. This indicates that it is possible to improve on the jitter performance of the ring oscillator simply by increasing the width of the transistors.

Based on the K versus oscillation frequency experiments, it can be concluded that some refinement needs to be made in the models that describe the relationship between the VCO voltage and VCO oscillation frequency. It would be useful to be able to probe the actual VCO voltage but due to the highly sensitive nature of that node, that is not possible. One way to measure the voltage at that node would be to build buffers into the

VCOs so that the voltage at the V_{VCO} node can be probed without affecting the performance of the VCOs.

The results are encouraging and have spurred further research into the relationship between oscillator jitter and device geometry.

Chapter 6 Conclusions

This thesis has shown that there is a definite relationship between the gate widths of the transistors in a ring oscillator and the jitter in the ring.

It has been shown experimentally that jitter, quantified by the figure-of-merit K, is related to gate width in the following manner:

$$K \propto \frac{1}{\sqrt{W}}. \tag{6.1}$$

This is in agreement with the theoretical predictions.

The theoretical predictions state that jitter, quantified by the figure-of-merit K, is related to frequency in the following manner:

$$K \propto \frac{1}{\sqrt{f^3}}. \tag{6.2}$$

The experimental results do not agree with the predictions and the suspicion is that the use of the long channel square-law model for the MOSFET drain current in a short channel environment may be causing the discrepancy.

This has provided the starting point for more research in this area. At the time of writing, a new chip containing 24 VCOs of various widths has been fabricated under a TSMC 0.18μm CMOS process and is undergoing evaluation. The sizes of the VCOs on this chip

form a matrix of widths and lengths. The widths are 10, 20, 60, 100, 200, 600 while the lengths are 0.18, 0.6, 1.8, 6, with all dimensions in μm. This chip should yield more data over a wider range and should conclusively allow for the determination of the K-width relationship. Where the K to frequency relationship is concerned, the use of a range of gate lengths that extend into the long channel region should show whether or not the long channel model is true for long channel devices.

Ring oscillators have a place in areas where average jitter performance, high levels of integration with low die real estate, and a wide tuning range are required. The results of this work will give designers a better understanding of how device parameters affect the jitter performance of ring oscillators. With a definite understanding of how K is affected by device geometry, it is hoped that designers can take a set of jitter specifications and design to that specification with confidence.

The other significant contribution that this work has made is in the design of a novel single-ended to differential converter that interpolates the phases of a ring oscillator to generate a differential signal. This converter is briefly described in Appendix A. A paper about this converter has been accepted for publication in the IEEE Journal of Solid-State Circuits and is pending publication.

Appendix A Chip Design

This appendix provides details on the design of the chip that was used in this work.

A.1 Process and Design

A TSMC 0.35µm 4-metal 1-poly CMOS process was used and the design and layout was performed using the Cadence suite of design and layout tools.

A.2 Design Overview

The chip was designed with 4 VCOs of different widths. The baseline NMOS VCO has a width of 12µm while the rest are 2, 4 and 8 times that width. Transistor lengths are of the minimum feature size of 0.4µm. The baseline VCO of 12µm was built up as a functional phase lock loop. The rest of the VCOs were left to operate open loop. The die area and pins left unused by the 4 VCOs were filled with test sections of the functional blocks that make up the entire PLL. They were placed on the chip for troubleshooting purposes should any part fail to operate properly.

A.3 Functional Blocks

A.3.1 The VCOs

The VCOs in this work are simple 3-stage inverter chain VCOs. A schematic of such a VCO is shown in Figure A.1.

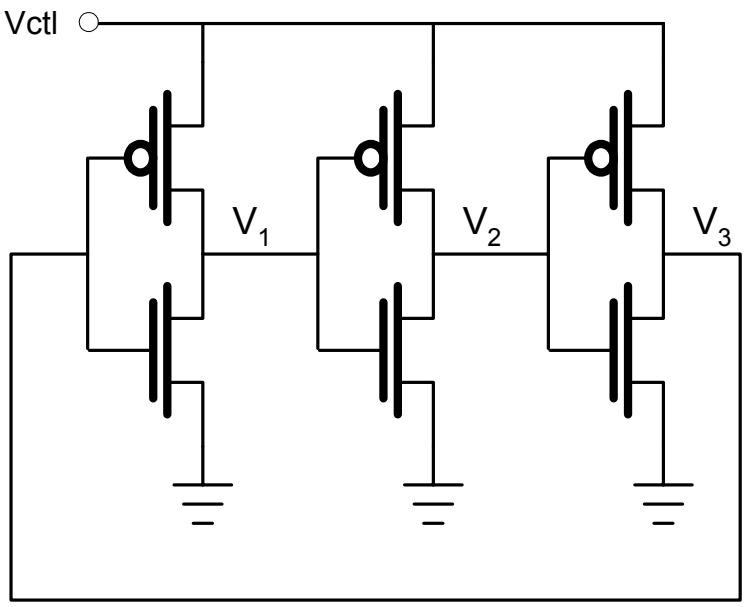

Figure A.1. Schematic of a 3-stage inverter chain VCO.

The NMOS transistors of the VCOs have W/L dimensions of 12um/0.4um, 24um/0.4um, 48um.0.4um, and 96um/0.4um. The P-type transistors are scaled accordingly to satisfy the relationship

$$\mu_p \cdot C_{ox} \cdot \frac{W_p}{L_p} = \mu_n \cdot C_{ox} \cdot \frac{W_n}{L_n} \quad \text{(A.3)}$$

For this process, the ratio μ_n/μ_p is approximately 2.83. For this work, $L_p=L_n$.

So far, the control voltage for the VCO has been described simply as the voltage applied between the sources of the PMOS and NMOS transistors in the ring. The control voltage is in reality applied through some other mechanism and the reasons for that will now be discussed.

A.3.2 Control Transistor for Input to the VCO

A.3.2.1 Direct Control

The voltage applied between the sources of the PMOS and NMOS transistors in the chain governs the oscillation frequency of the VCOs. Figure A.2 shows a method of connecting the VCO to the charge-pump and loop filter, with the control voltage V_{CTL} applied directly as the supply voltage of the inverter chain.

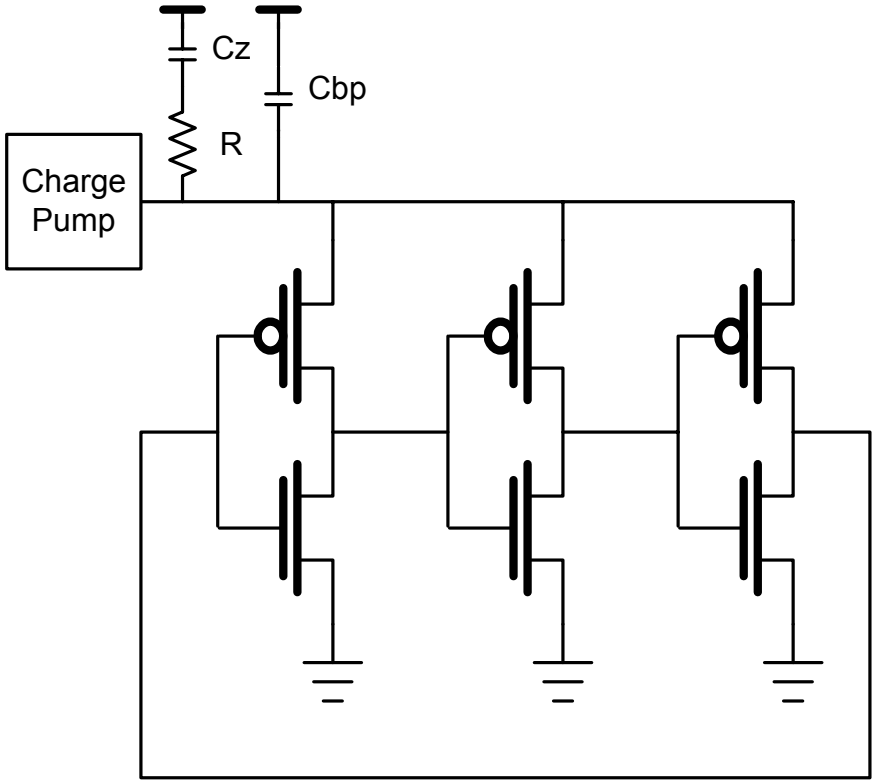

Figure A.2. Simple method of connecting V_{CTL}.

This configuration works as long as the source behind V_{CTL} can provide enough current to drive the VCO, which is typically in the mA range. In most applications though, the circuit in Figure A.2 will not work because the current drawn by the VCO will load down the loop filter node, causing the VCO to consistently run slow despite the phase-frequency detector continuously signaling UP.

A.3.2.2 PMOS Control Transistor

To overcome this problem a control transistor can be placed between the loop filter and the VCO. In order to maintain the charge in the loop filter capacitor, the loop filter output is fed into the gate of a MOSFET. This is illustrated in Figure A.3. This configuration provides the high impedance that is desired from the loop filter's point of view. This will ensure that the loop filter capacitor is not loaded down by the VCO. The source of the control transistor is connected to VDD. This ensures that as long as the control transistor is designed to be wide enough, there will be enough current available to drive the VCO.

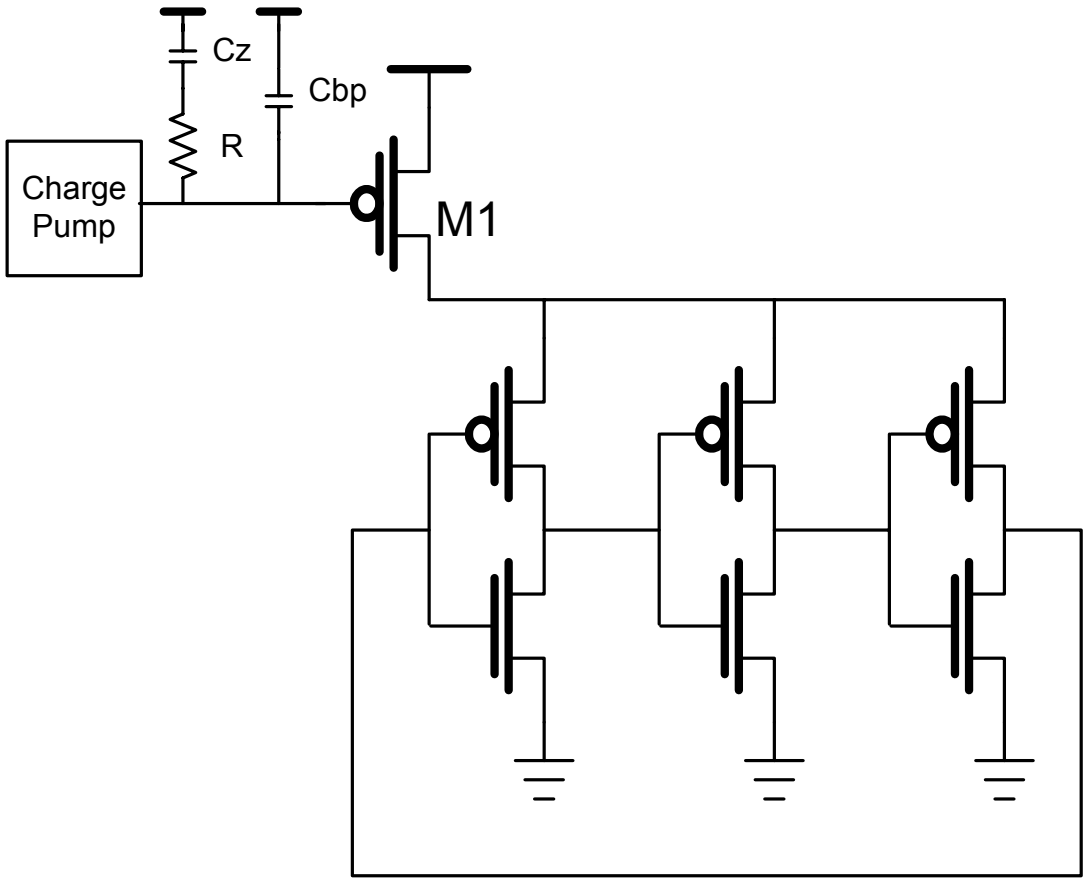

Figure A.3. Enhanced method of connecting V_{CTL} using a PMOS control transistor.

A.3.2.3 NMOS Control Transistor

It is worth mentioning that the solution shown in Figure A.3 is not the only control transistor configuration possible. An alternative configuration to this solution is presented in Figure A.4. In this configuration, an NMOS control transistor is used and its source is tied to the substrate.

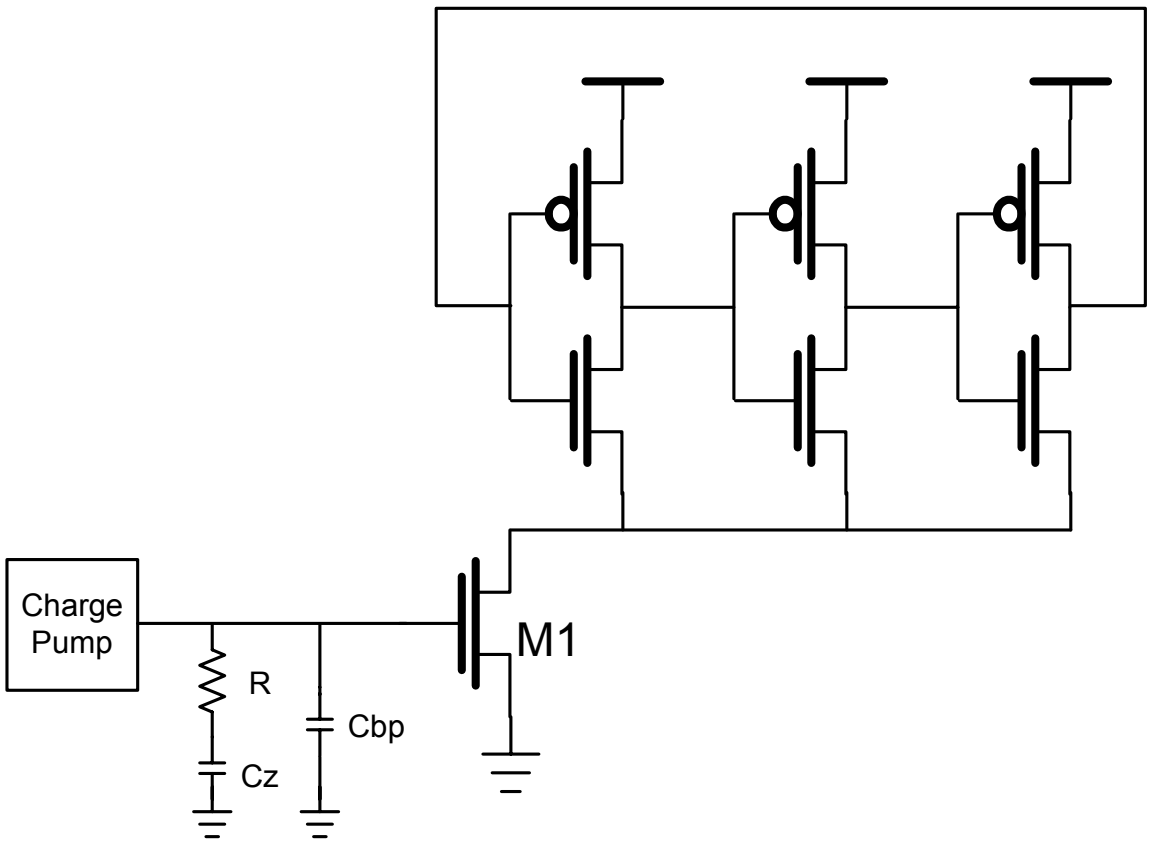

Figure A.4. Enhanced method of connecting V_{CTL} using a NMOS control transistor.

From the point of view of ensuring that the loop filter capacitor is not loaded down and that enough current is provided to run the VCO, either configuration will suffice. But it was found through simulation that the first configuration with the PMOS control transistor is a better solution. Both configurations were simulated with a sinusoidal modulation on the supply rail. The coupling of that simulated noise to the VCO output was measured by observing the variation in the VCO frequency. The PMOS control

transistor configuration was better able to isolate the VCO from variations in the supply voltage.

That and the fact that it placed all sources of the NMOS transistors in the ring at the same potential as the substrate (thus eliminating body effect in the ring) drove the choice of the PMOS control transistor over the NMOS version. With the PMOS control transistor the PMOS transistors in the ring do not suffer from body effect because they each reside in their own dedicated N-well that is tied to the source of the transistor that resides in it.

A.3.2.4 Sizing the Control Transistor

The control transistor was sized, through simulation, to provide enough current to drive the VCO, as well as to provide as much linearity over as wide a tuning range between the control transistor gate voltage and the frequency output of the VCO. Figure A.5 shows the transfer function of two control transistors.

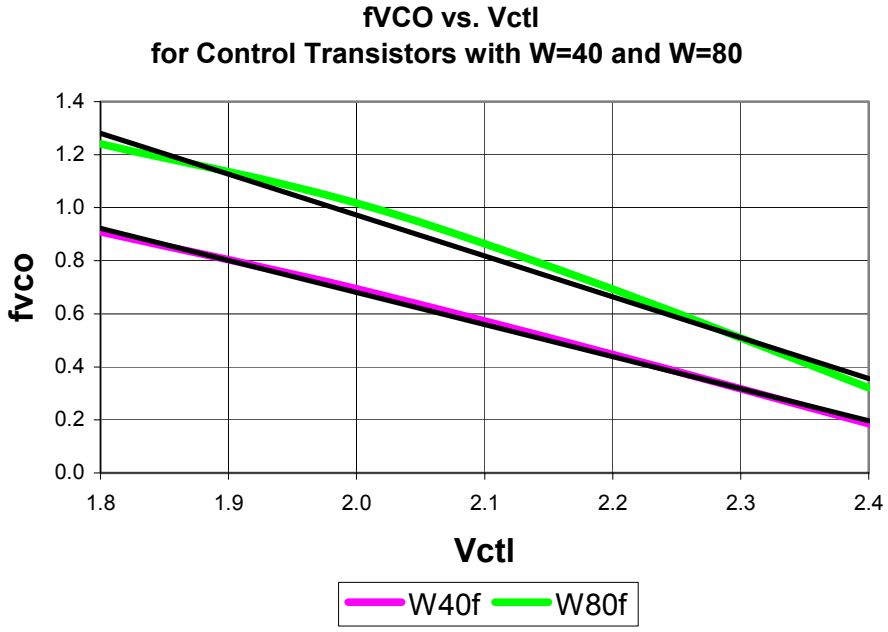

Figure A.5. Simulated f_{vco} versus V_{CTL} for control transistors of two different sizes.

While the 80µm control transistor exhibits a wider tuning range, the linearity of the 40µm control transistor is better. Based on simulation results, it was chosen to make the control transistor 40µm wide. It is important to realize that the control transistor has the effect of making K_{VCO} negative.

A.3.3 VCO Single-Ended to Differential Converter

The ring oscillator in this work is single-ended while the rest of the circuitry is differential. The conversion of the VCO output to a differential signal was done to take

advantage of the supply and substrate noise immunity that differential signaling offers. Achieving this single-ended to differential conversion posed several challenges.

A.3.3.1 Conventional Techniques

Figures A.6 and A.7 show two possible methods of performing single-ended to differential conversion of the output of a CMOS SRO.

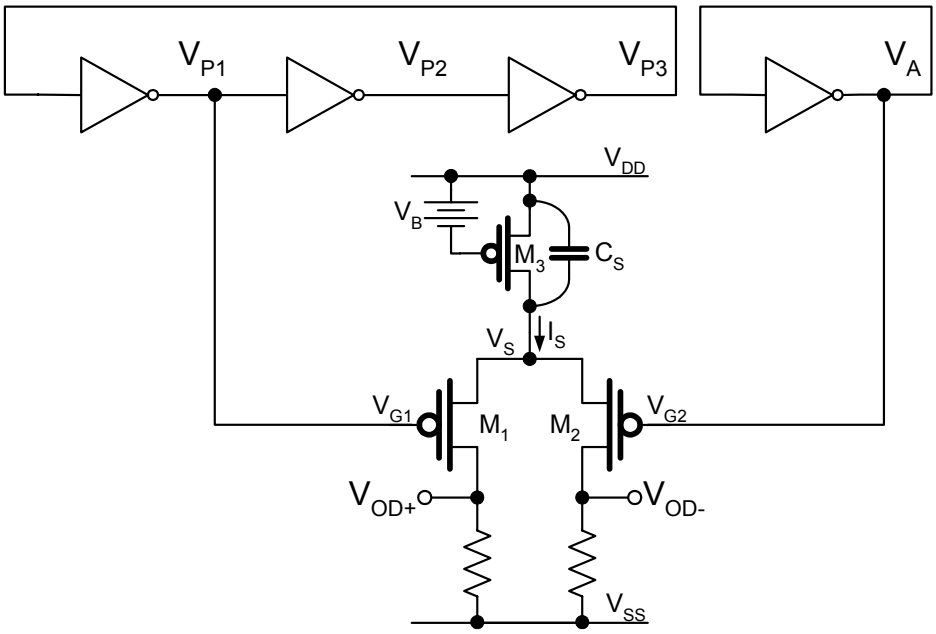

Figure A.6. Single-ended to differential conversion circuit using a single phase and DC average of the ring.

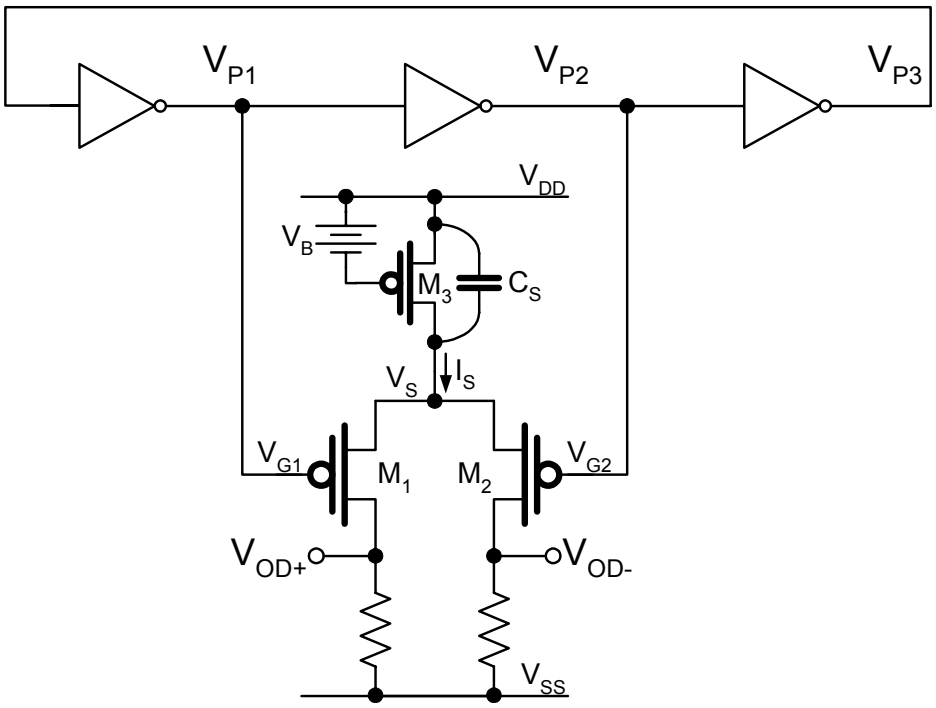

Figure A.7. Single-ended to differential conversion circuit using two phases of the ring.

In each case, a PMOS differential pair, formed by transistors M_1 and M_2, is used as a simple comparator to develop the desired output signals V_{OD+} and V_{OD-}, which are the differential representation of the single-ended ring signal. The differential pair is biased by current I_S, which is developed by current source M_3 with gate voltage V_B. C_S represents the sum of all parasitic capacitances at node V_S.

In the approach shown in Figure A.6, comparator input V_{G1} is obtained from one phase of the ring and input V_{G2} from a half-amplitude reference V_A developed by shorting the output and input of a replica ring stage.

In the approach shown in Figure A.7, the comparator inputs are obtained from two phases of the ring [3]. This approach eliminates the need to develop the half-amplitude reference required in the approach of Figure A.6.

Figures A.8 and A.9 show the waveforms associated with each approach.

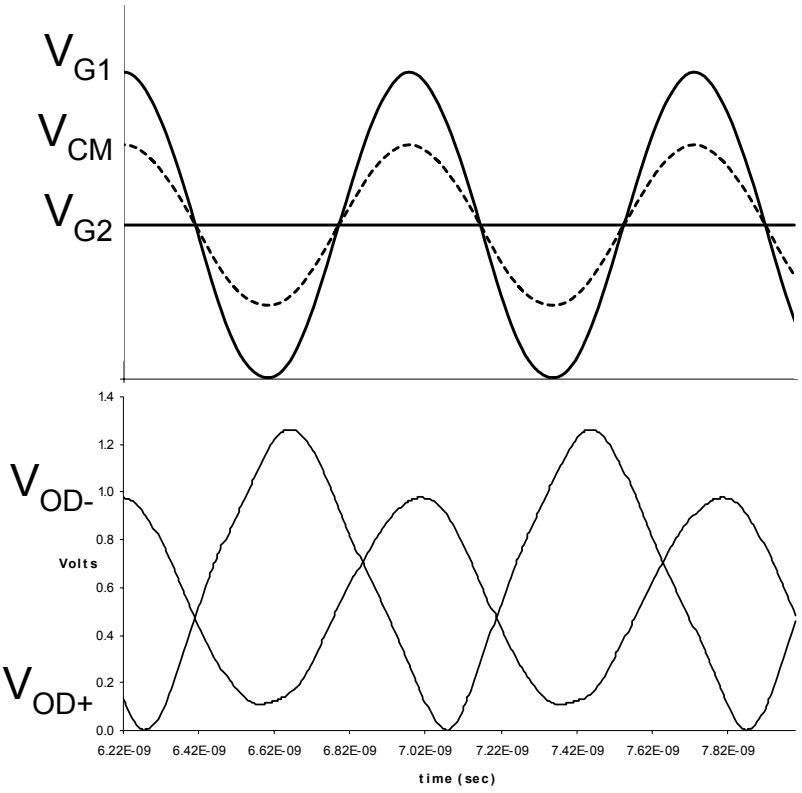

Figure A.8. Waveforms associated with Figure A.6.

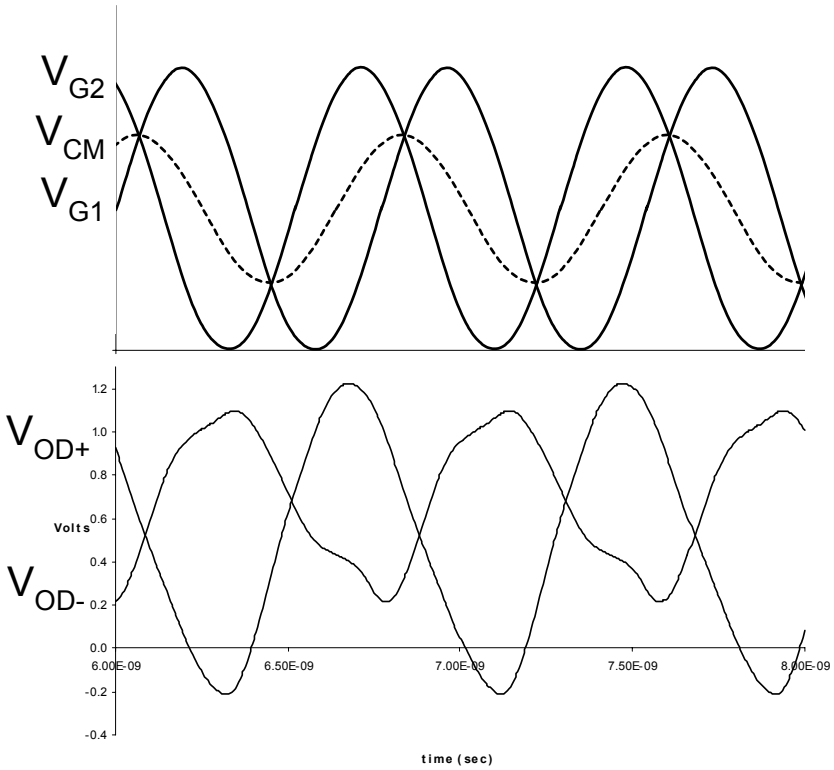

Figure A.9. Waveforms associated with Figure A.7.

Idealized waveforms are shown for comparator inputs V_{G1} and V_{G2}; also shown are simulated output waveforms in a 0.35um CMOS process. It can be seen from the simulated waveforms that outputs V_{OD+} and V_{OD-} deviate significantly from the ideal differential representation of the single-ended ring signal. The two major nonidealities are duty-cycle distortion and waveform asymmetry. The main cause of these nonidealities is the varying common mode of the inputs V_{G1} and V_{G2}, shown as dashed waveform V_{CM} in Figures A.8 and A.9. Although low frequency common mode variations are rejected by the differential pair, at higher frequencies common mode

rejection is reduced significantly due to C_S. Variation in V_{CM} causes variation in the voltage V_S, which in turn causes a variation in differential pair bias current I_S in accordance with $C_S(dV_S/dt)$. This variation in I_S results in varying waveform amplitude at the differential pair output.

A.3.3.2 Improved Conversion Technique

Figure A.10 shows the single-ended to differential conversion technique developed in this work.

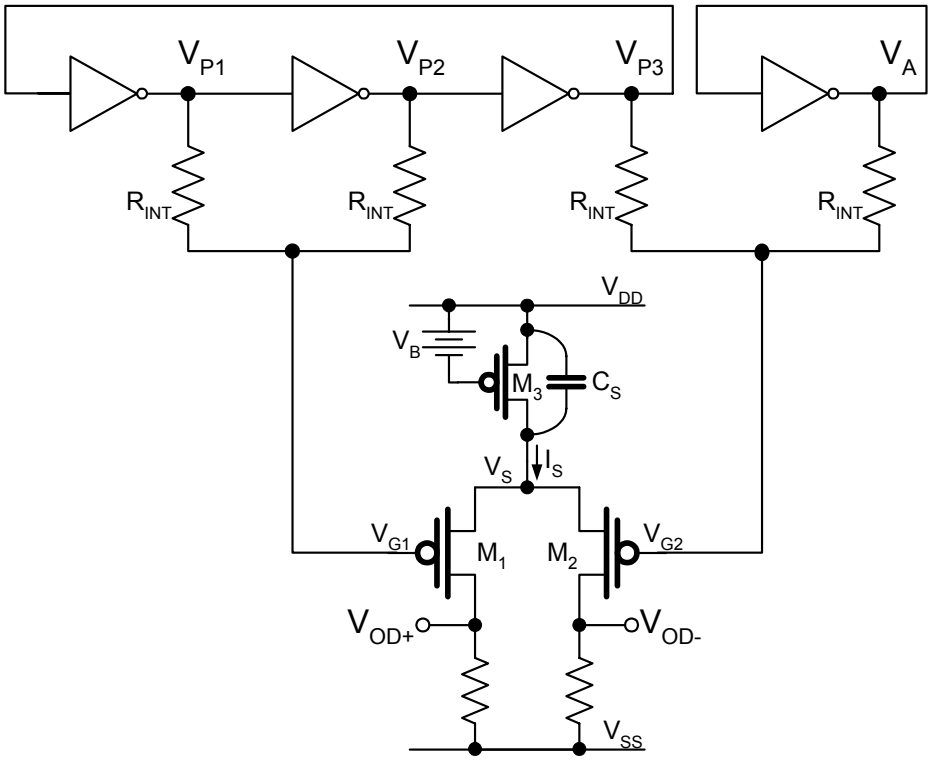

Figure A.10. Improved single-ended to differential converter.

In this approach, the same differential pair amplifier is used but the inputs V_{G1} and V_{G2} are taken from an interpolating network. Assuming resistors R_{INT} to be of equal value, the outputs of the interpolating network are given by

$$V_{G1} = \frac{V_{P2} + V_{P3}}{2} \tag{A.4}$$

$$V_{G2} = \frac{V_{P1} + V_A}{2} \tag{A.5}$$

The function of the interpolating network is to develop a differential representation of the SRO signal with constant common mode component. To see how this function results, we first develop idealized expressions for the phase voltages V_{P1}, V_{P2}, and V_{P3}.

At each stage of the ring, the oscillator waveform propagates with a phase lag of $\pi/3$ radians (due to the stage delay) as well as an inversion ($\pm\pi$ radians). Although the ring oscillator is often thought to be a "square wave" oscillator, at high speeds the waveforms in a three-stage ring are more nearly sinusoidal. If we idealize the waveforms to be sinusoidal with equal delay in each stage, then the voltage waveforms at each phase can be represented as

$$V_{P1} = V_A + V_{PK}\sin(\omega t) \tag{A.6}$$

$$V_{P2} = V_A + V_{PK}\sin(\omega t + 2\pi/3) \tag{A.7}$$

$$V_{P3} = V_A + V_{PK}\sin(\omega t - 2\pi/3) \tag{A.8}$$

$$V_A = \frac{V_{PK}}{2} \tag{A.9}$$

with sinusoid frequency ω, peak amplitude V_{PK}, and DC average V_A. Substituting (A.5) through (A.8) into (A.3) and (A.4), and performing some trigonometric manipulation, gives

$$V_{G1} = V_A + \left(\frac{V_{PK}}{2}\right)\sin(\omega t) \tag{A.10}$$

$$V_{G2} = V_A - \left(\frac{V_{PK}}{2}\right)\sin(\omega t) \tag{A.11}$$

Thus (A.9) and (A.10) show that V_{G1} and V_{G2} constitute a signal pair with common mode V_A and differential signal $V_{PK}\sin(\omega t)$.

Figure A.11 shows the waveforms associated with the approach of Figure A.10.

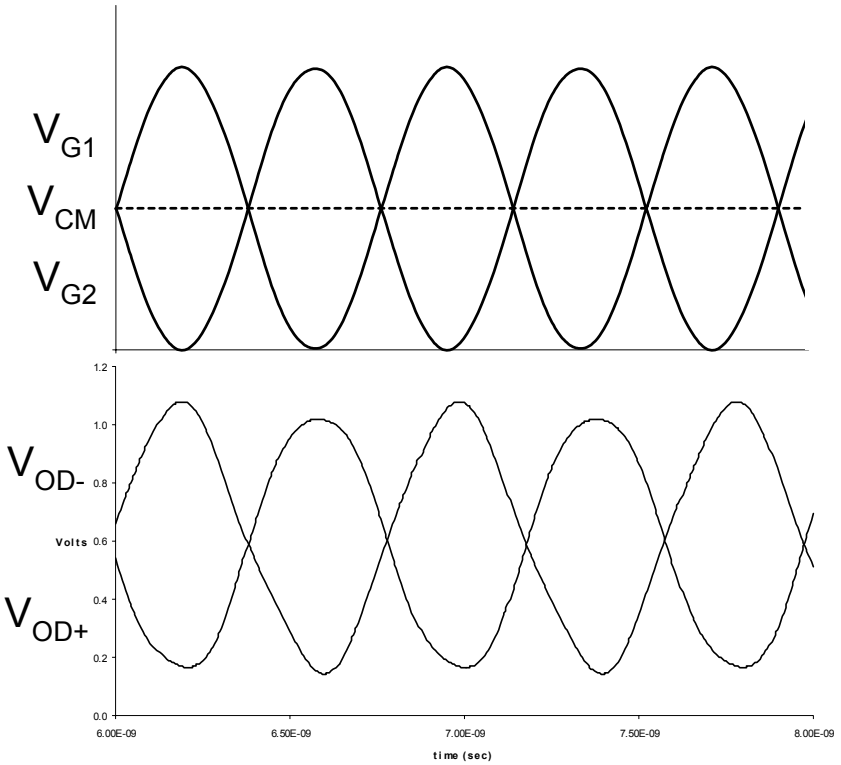

Figure A.11. Waveforms associated with Figure A.10.

The idealized waveforms for comparator inputs V_{G1} and V_{G2} show a constant common mode component $V_{CM}=V_A$. It can be seen that the simulated outputs V_{OD+} and V_{OD-} exhibit much improved duty cycle regularity and amplitude symmetry.

In practice, V_{CM} is not constant since the signal from each phase of the VCO is not purely sinusoidal; for a three-stage VCO operating near maximum speed the assumption of pure sinusoids is only approximately true. This results in some variation in V_{CM}, which causes small variations in V_S and I_S. This in turn causes the slight variation in the amplitudes of

V_{OD+} and V_{OD-} as shown in the simulated waveforms in Figure A.11. Even with these slight variations, waveform symmetry is significantly improved from the cases shown in Figures A.8 and A.9.

A.3.3.3 Verification of Improvement

The circuit has been operated at VCO speeds of up to 1.3GHz.

To examine performance in the presence of power supply noise, the circuit configurations of Figures A.6 and A.10 were simulated with a 200mV pk-pk, 100MHz sine wave superimposed on the 3.3V power supply. Zero-crossing times of the output differential waveforms are shown in Figures A.12 and A.13. Jitter for the circuit using the improved technique is 1.73ps rms, which represents a 5X reduction from the 9.85ps rms for the circuit of Figure A.6.

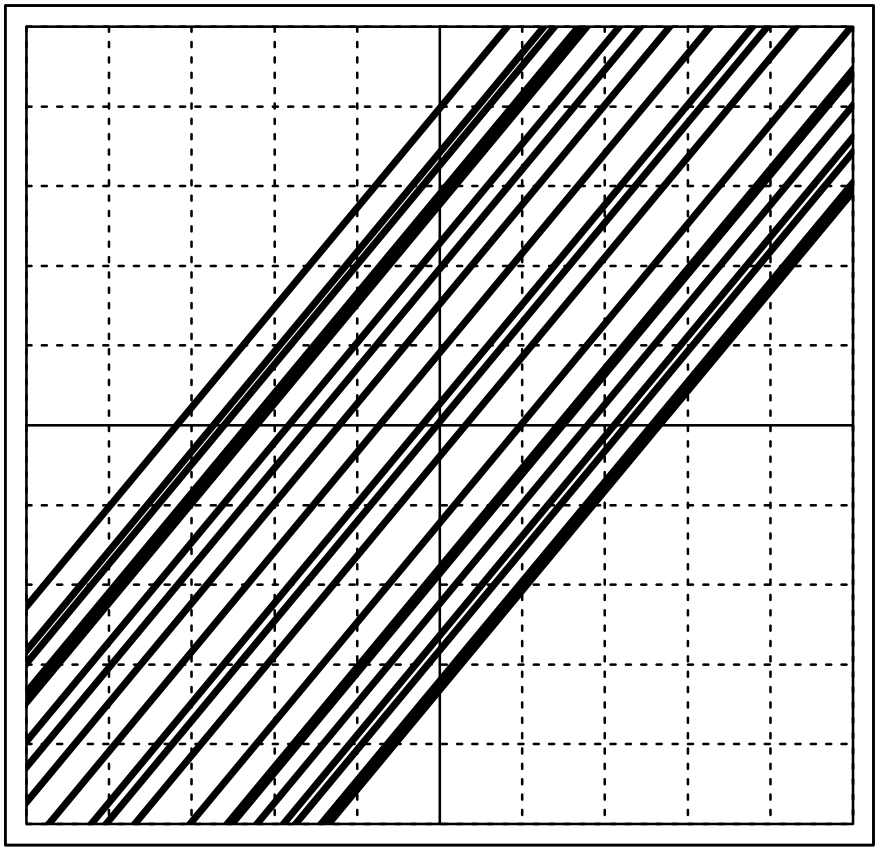

Figure A.12. Simulated output, simple differential pair buffer in Figure A.6. Jitter = 9.85 ps rms. Horizontal: 5ps/div. Vertical: 20mV/div.

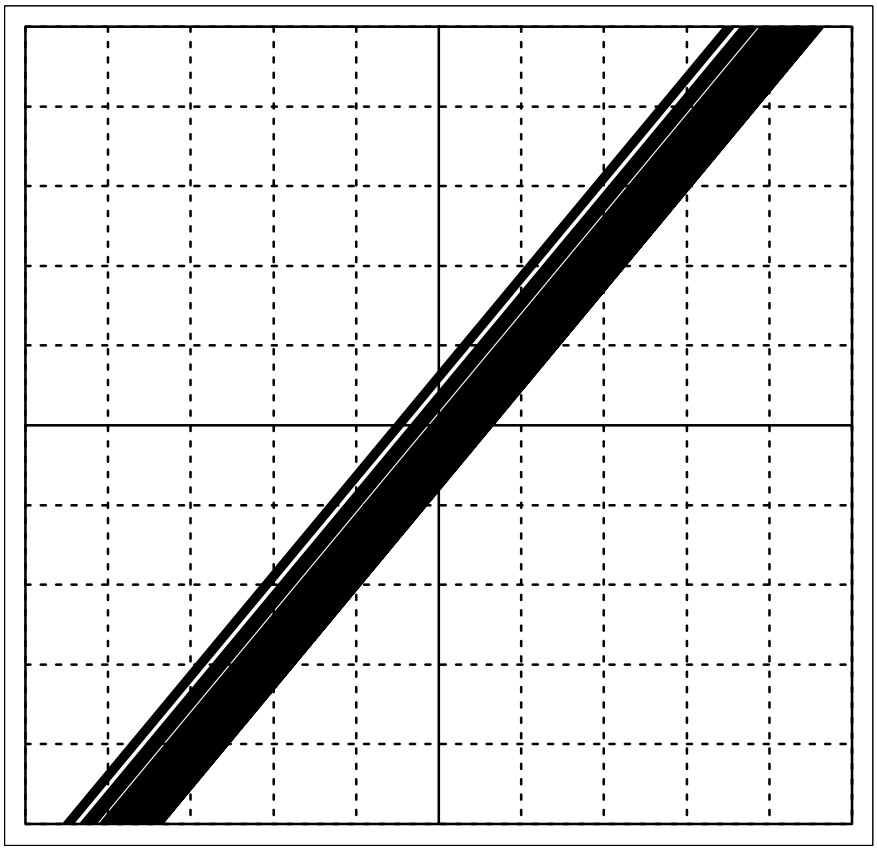

Figure A.13. Simulated output, improved differential pair buffer in Figure A.10. Jitter = 1.73 ps rms Horizontal: 5ps/div. Vertical: 20mV/div.

A.3.3.4 Publication of Results

A journal paper based on the design of this converter was submitted to the IEEE Journal of Solid State Circuits and has been accepted for publication.

A.3.4 Divide-by-64 Prescaler

The gigahertz clock frequencies in the ring oscillator must be brought down to a lower frequency before being fed into the phase-frequency detector. With expected VCO frequencies in excess of 1GHz, it was determined that it would make the task of bringing the VCO output off-chip, through the bond-wire inductance, easier if it was first divided down to a lower frequency. A divide-by-64 block made up of 6 cascaded divide-by-2s was designed to accomplish this. Each divide-by-2 is realized by placing the inverted output of a D-flip-flop (DFF) back into the D-input. The schematic of one divide-by-2 cell is shown in Figure A.14. The dividers employ a Current Mode Logic (CML) architecture, which performs logic functions through the steering of currents through sets of differential pairs. Latching is carried out by a master-slave latch configuration driven by the input clock.

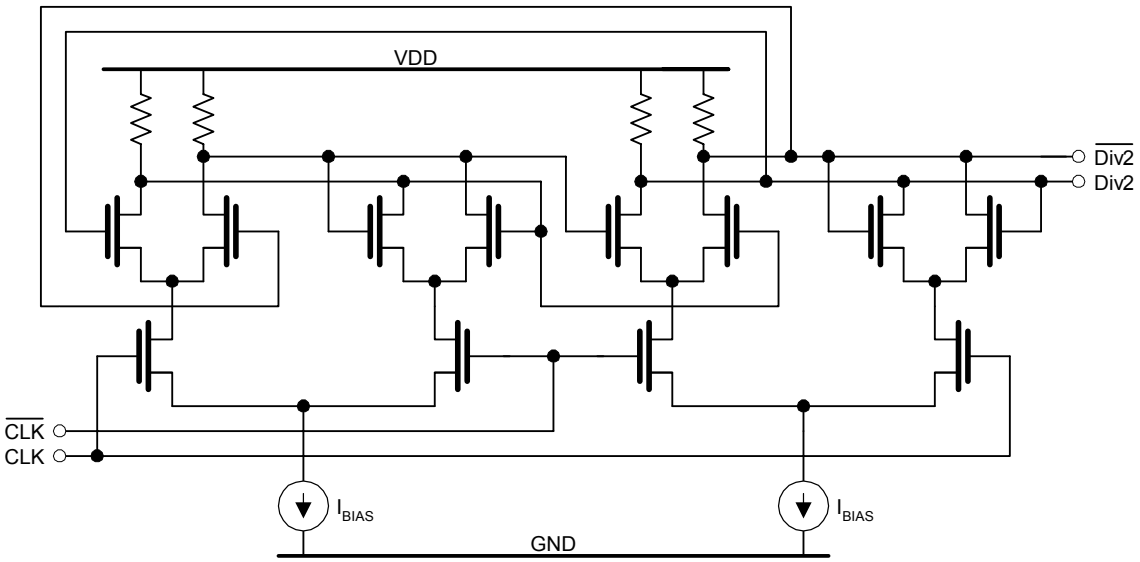

Figure A.14. A divide-by-2 cell. 8 such cells in series make up the divide-by-64.

The divided-by-64 signal is used only in the PLL where it is used to provide the VCO feedback input for the Phase-Frequency Detector. For all four VCOs, the signal that is taken off-chip is tapped off the divided-by-8 stage in the divide-by-64.

The divider was simulated to speeds of up to 2GHz.

A.3.5 Output Driver

In order to drive the high-frequency differential VCO signals off-chip, an output buffer is required to provide the necessary current drive. The divided-by-8 VCO output is fed into a differential pair amplifier that subsequently drives the gates of two open-drain P-type transistors. The drains are directly connected to output pins on the package. These pins

are subsequently connected through external resistors to ground to realize a current to voltage conversion. The resulting voltage signal is then fed through a 4:1 transformer to transform the impedance to 50Ω for interfacing to test equipment.

A.4 The Phase-Locked Loop

All the blocks described above are common to all the VCOs on the chip. The smallest VCO was designed with the option to operate closed loop as a Phase-Locked Loop (PLL). The PLL layout and chip micrograph are shown in Figures A.15 and A.16. The additional functional blocks required to close the loop and form the PLL are described in this section.

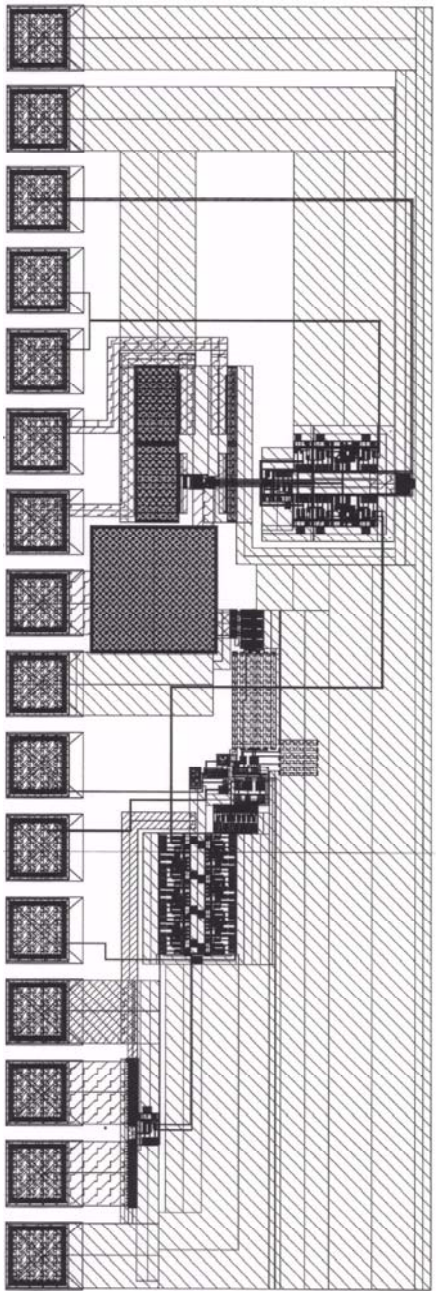

Figure A.15. Layout of the PLL.

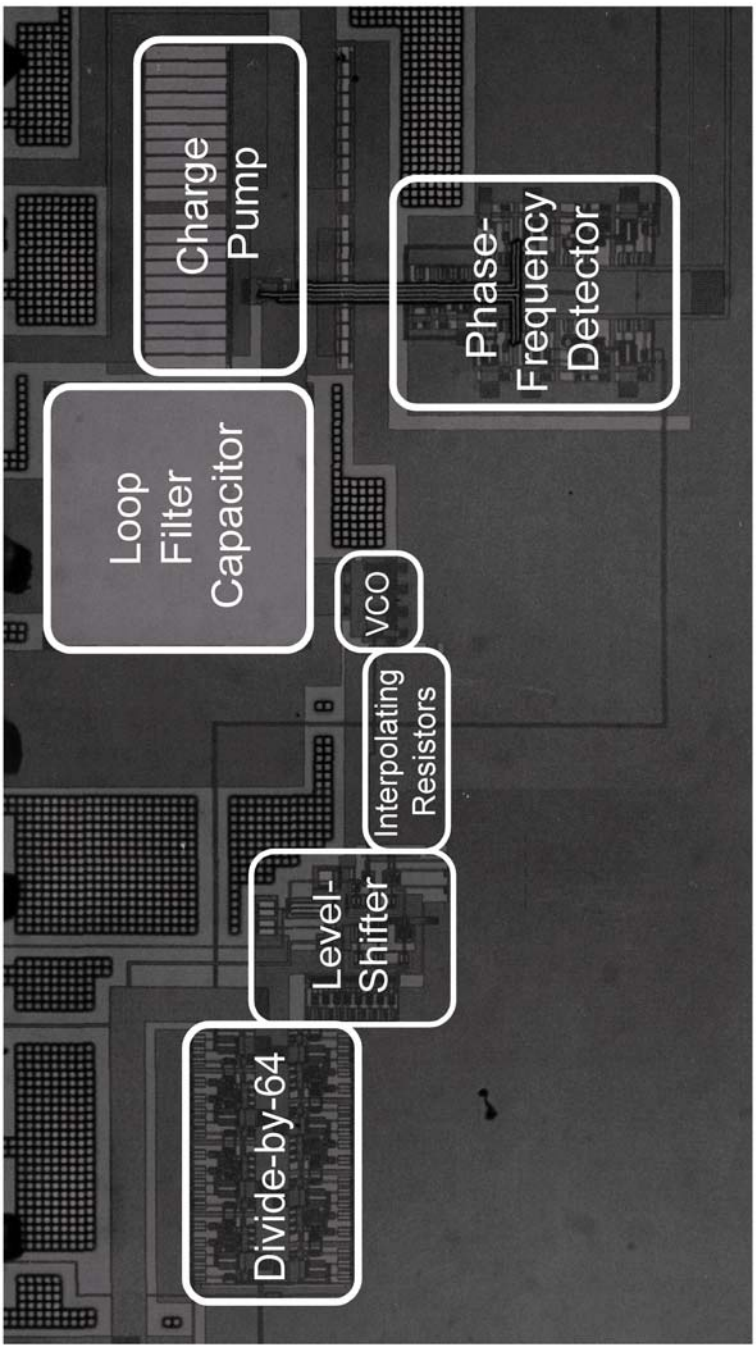

Figure A.16. Micrograph of the PLL.

A.4.1 Phase-Frequency Detector

The Phase-Frequency Detector, or PFD, in this work utilizes a pair of D-flip-flops similar to those used in the dividers, and a NAND gate. A block diagram of the PFD is shown in Figure A.17. The DFFs used in the PFD are enhanced with a reset function. A schematic of the DFF is shown in Figure A.18. The reset function of the DFF is triggered by a NAND logic gate when the outputs of both DFFs are logic high.

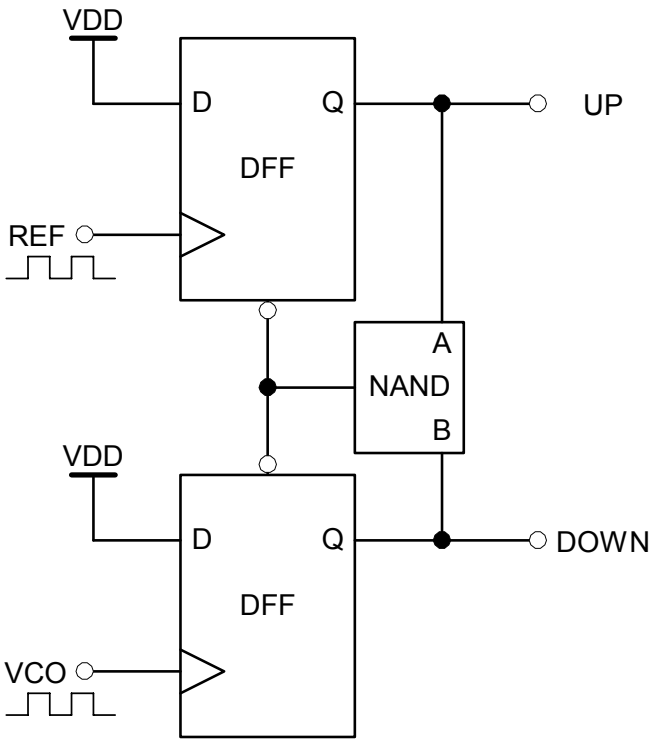

Figure A.17. Block diagram of PFD.

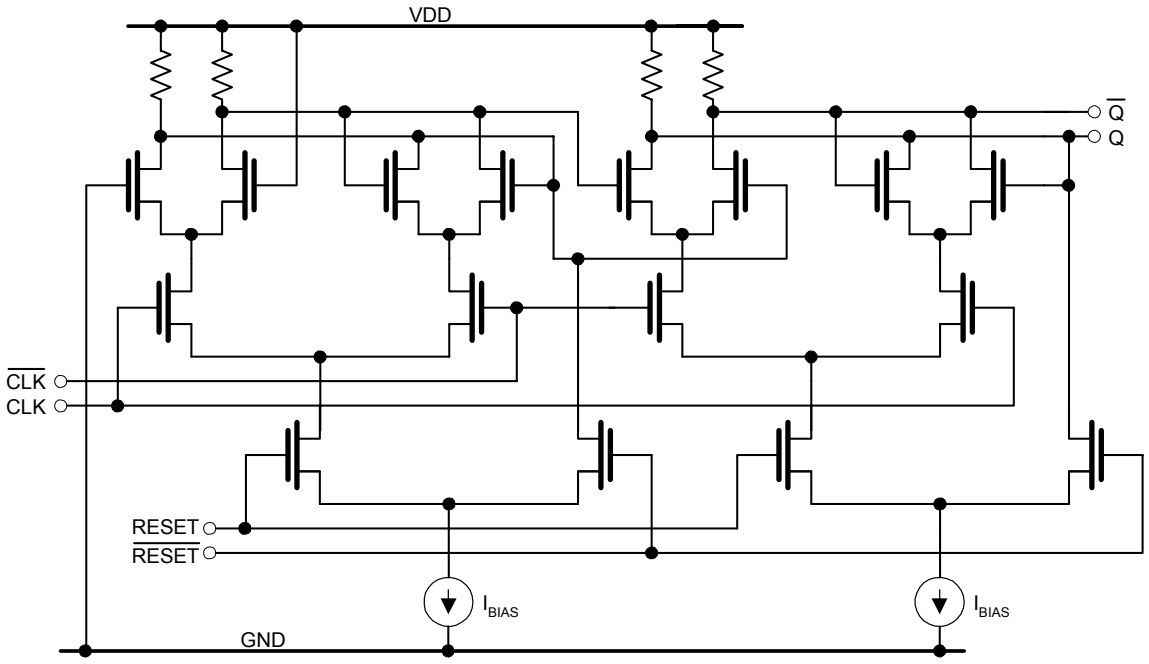

Figure A.18. Schematic of D-Flip-Flop with reset used in PFD.

The NAND gate utilized in the PFD is shown in Figure A.19. The principle of operation is simple. Only when inputs A and B are both high will I_{BIAS} flow through the load resistor on the right. In that situation, the NAND output will be forced to a logic low, thus realizing a NAND function.

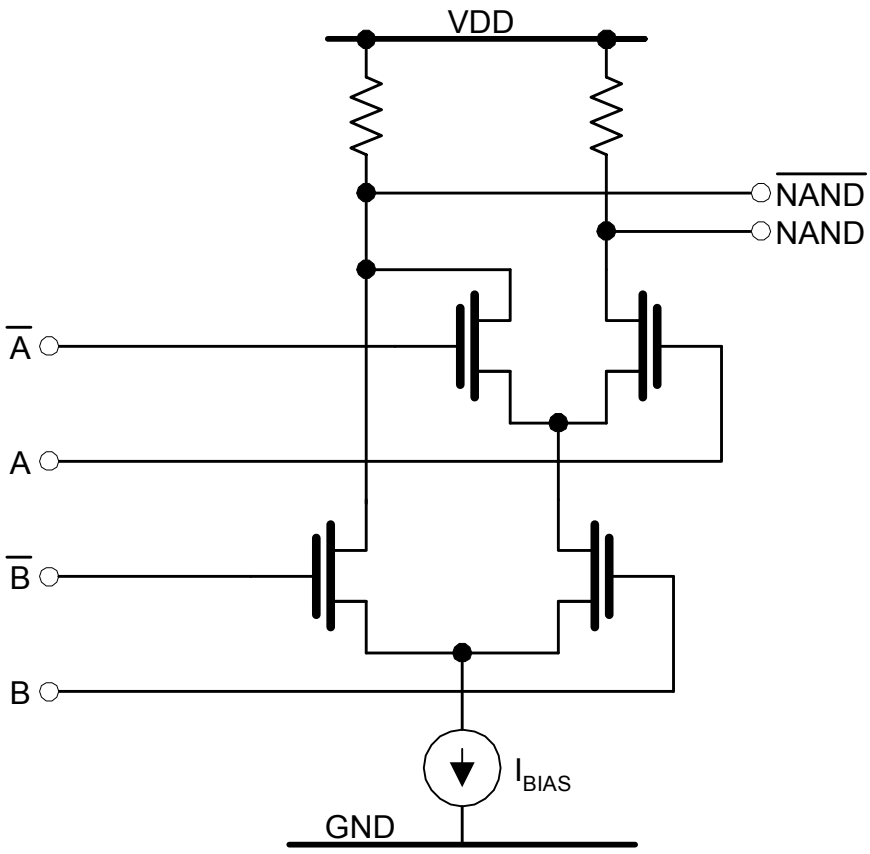

Figure A.19. Schematic of differential NAND gate used in PDF.

Although shown in Figure A.17 as being single-ended, the PFD is really differential. The differential UP and DOWN outputs of the PFD feed into the charge pump. Figure A.20 shows the layout of the entire PFD.

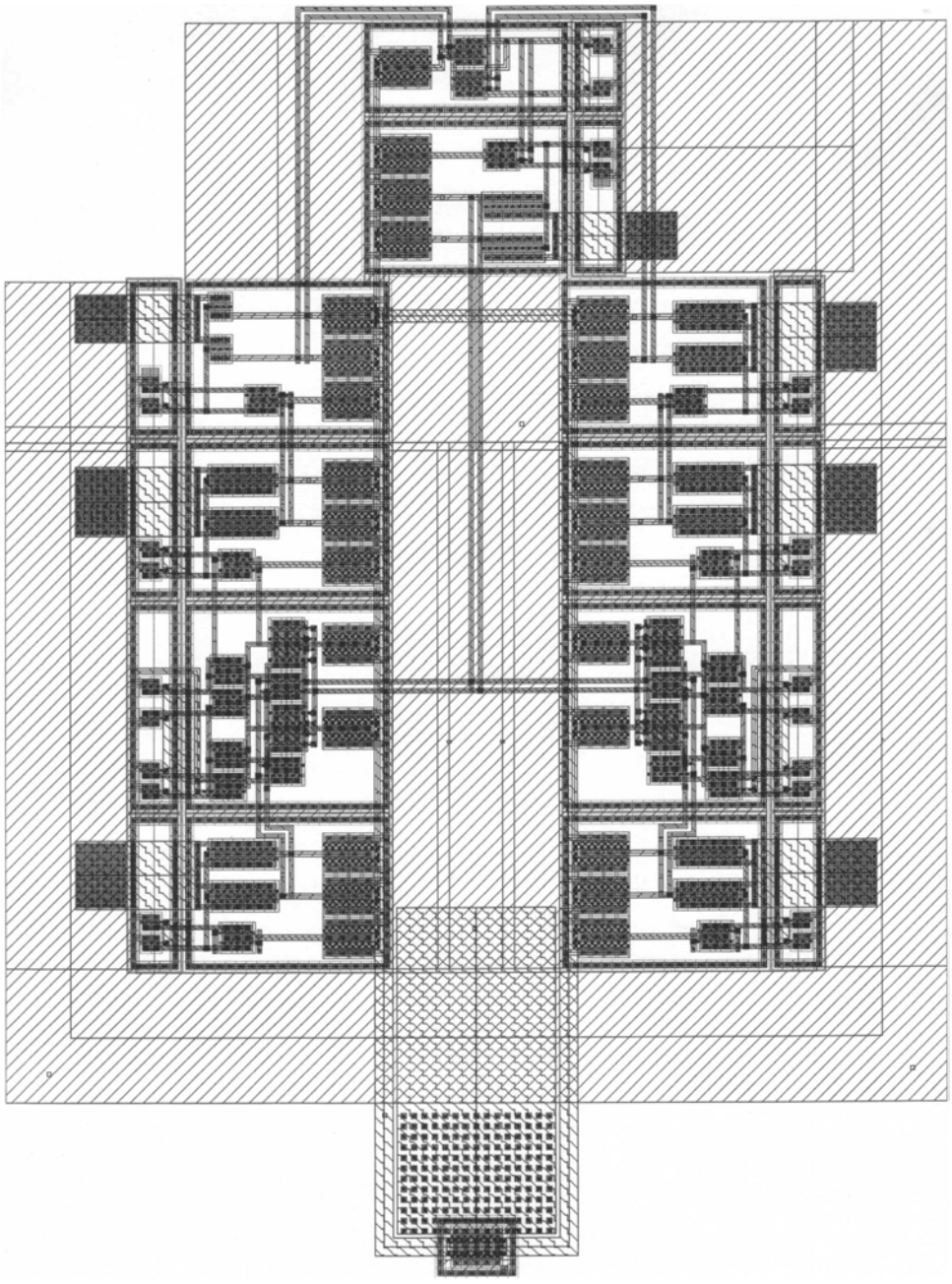

Figure A.20. Layout of PFD showing the NAND gate at the top and D-Flip-Flops on each side.

A.4.2 Charge Pump

The Charge Pump is formed with two differential amplifiers, one N-type and the other P-type, and current mirrors, again, one N- and one P-type. This is shown in Figure A.21.

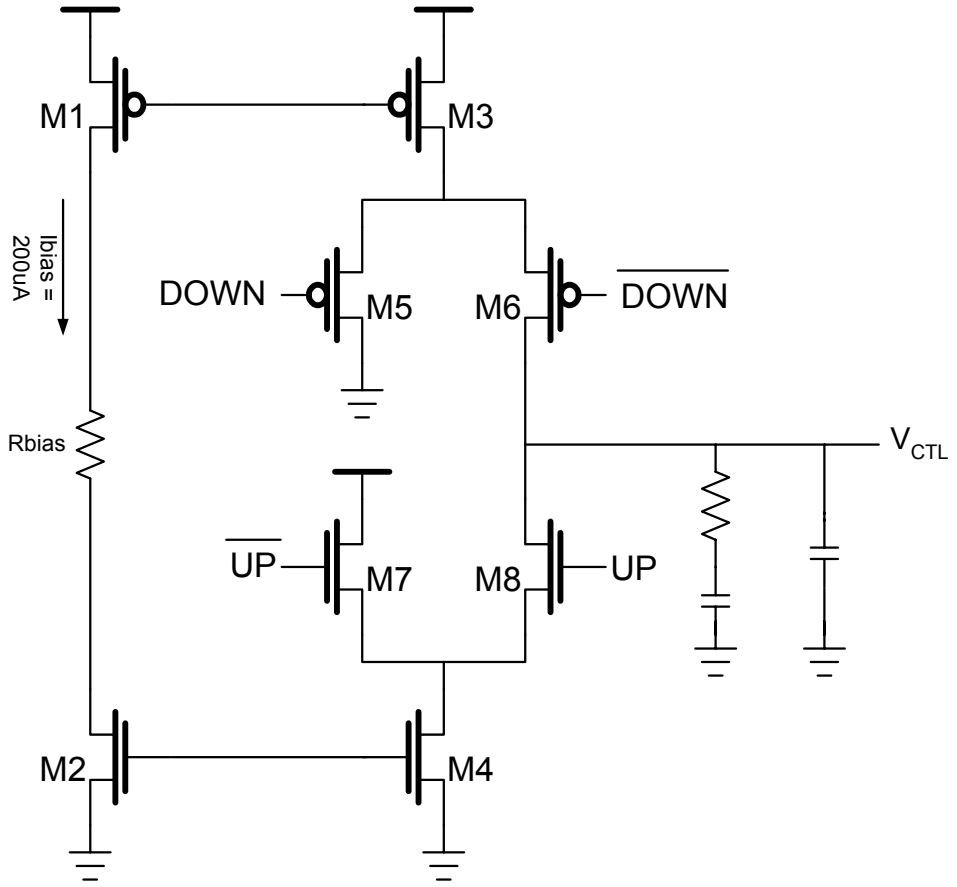

Figure A.21. Schematic of charge pump.

The bias current for the current mirrors is set by an external resistor between the drains on the primary sides of the current mirrors. This will ensure that the current in both the

N- and P-type mirrors is equal. The current sources have a large W/L ratio so as to minimize the effects of channel length modulation as the voltage at the output of the charge pump approaches the supply and ground rails. The steering differential pairs have their gates tied to the outputs of the PFD. Depending on how the PFD outputs swing the charge pump inputs, the currents in the NMOS and PMOS current mirrors are made to flow in one of a few ways. Table 3 summarizes the states of the charge pump inputs and the flow of current in each state.

UP	**DN**	**PMOS Current Flow**	**NMOS Current Flow**	**Net Effect**	**Vctl**	**FVCO**
HI	**LO**	VDD to GND	VCTL to GND	Current pulled out of VCTL	Decreases	Increases
LO	**HI**	VDD to VCTL	VDD to GND	Current pumped into VCTL	Increases	Decreases
LO	**LO**	VDD to GND	VDD to GND	No Change	Remains the same	No Change
HI	**HI**	VDD to VCTL	VCTL to GND	No Change	Remains the same	No Change

Table 3. Table of charge pump states and the resultant effects.

Remember that in this implementation of the VCO, the V_{CTL}-f_{VCO} relationship is negative. In other words, when the voltage at V_{CTL} is decreased f_{VCO} is increased, and vice-versa. Remember also that the control voltage is derived from the integration of charge in the loop filter capacitor. Thus, the size of the loop filter capacitor has an effect on the rate of change in V_{CTL} for a given bias current.

A.4.3 On-Chip Loop Filter Capacitor

The loop filter has two capacitors and the smaller of the two is small enough that it can be placed on-chip. In addition, placing it close to the VCO has the added effect of providing good bypassing at the control voltage node.

The capacitor was realized using a PMOS transistor whose source and drain were shorted to each other. This is shown in Figure A.22.

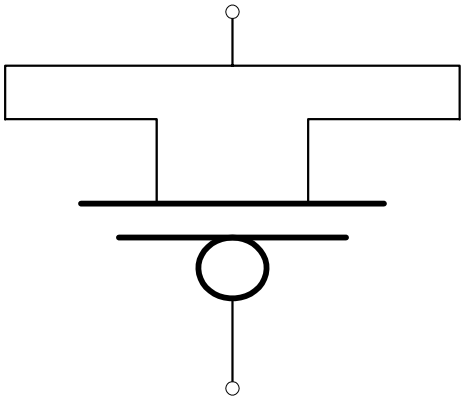

Figure A.22. Schematic of the PMOS capacitor.

The terminals of the capacitor are formed between the gate and source-drain nodes. For MOSFET capacitors to function properly, they must be in strong inversion [1]. For this to happen, the gate-source voltage has to exceed the transistor threshold voltage V_{th}. Because a PMOS transistor is used here, the gate must be at a lower voltage than the source-drain node. In this case, as part of the loop filter, this capacitor is placed so that the source-drain node is tied to VDD while the gate is tied to V_{CTL}. The characteristic of this type of capacitor is shown in Figure A.23. If the VCO is in operation then that condition must be satisfied because the gate of the control transistor must be at least Vt below VDD.

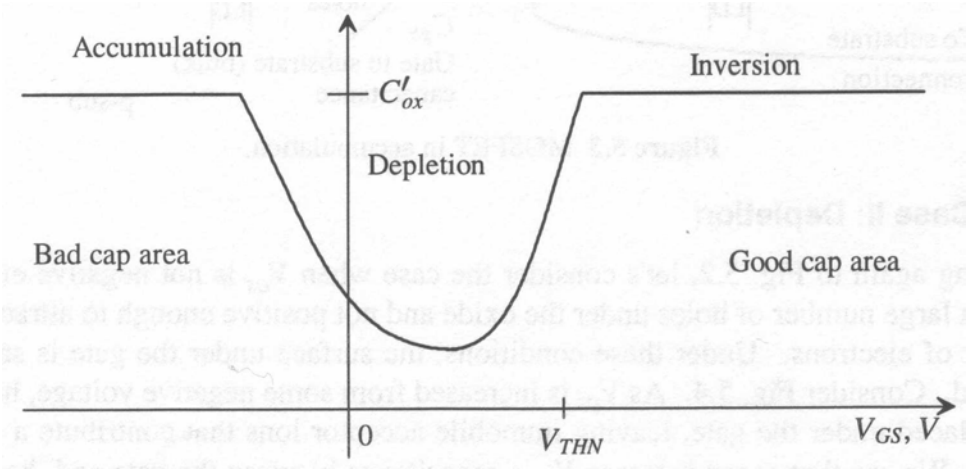

Figure A.23. Capacitance versus applied voltage for a NMOS capacitor [1].

A.5 Chip Layout and Chip Micrograph

The entire chip was laid out in Cadence and placed on a 84-pin pad frame. Each of the 4 sides of the chip contains one each of the VCOs and the other unused pins are connected to blocks of the sub-blocks that make up the VCOs and PLL. This was done to allow for individual performance testing and troubleshooting of individual blocks.

A.5.1 Layout in Cadence

Figure A.24 shows the layout of the whole chip as it looks in Cadence.

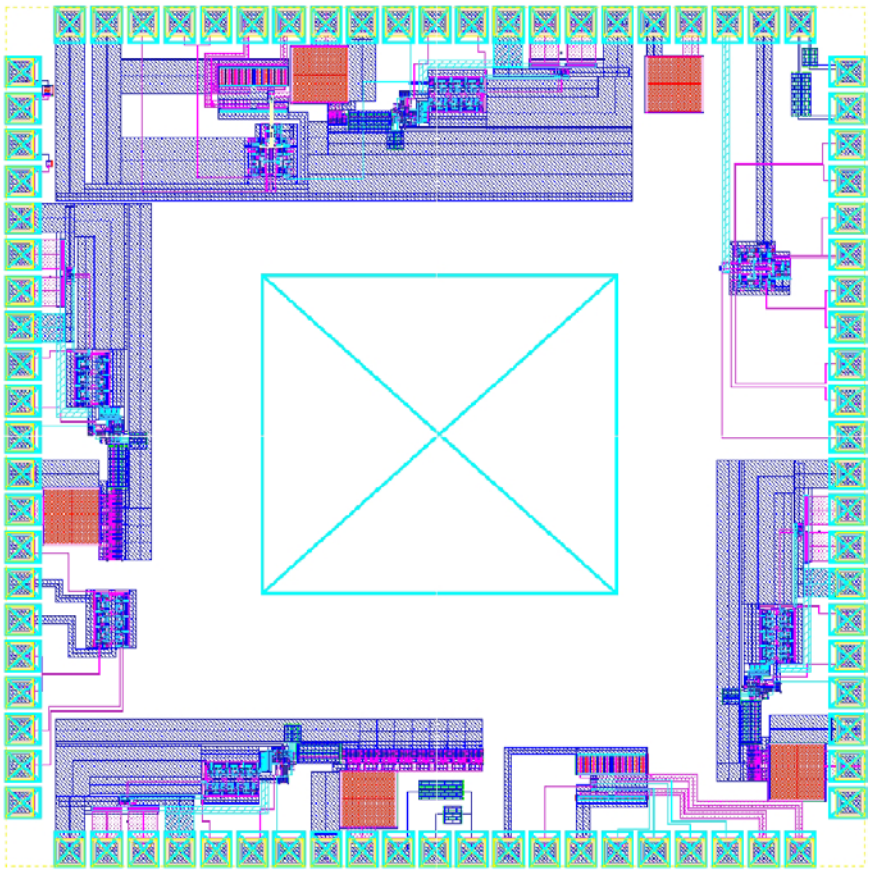

Figure A.24. Layout of chip in Cadence.

A.5.2 Chip Micrograph

Figure A.25 shows a micrograph of the chip.

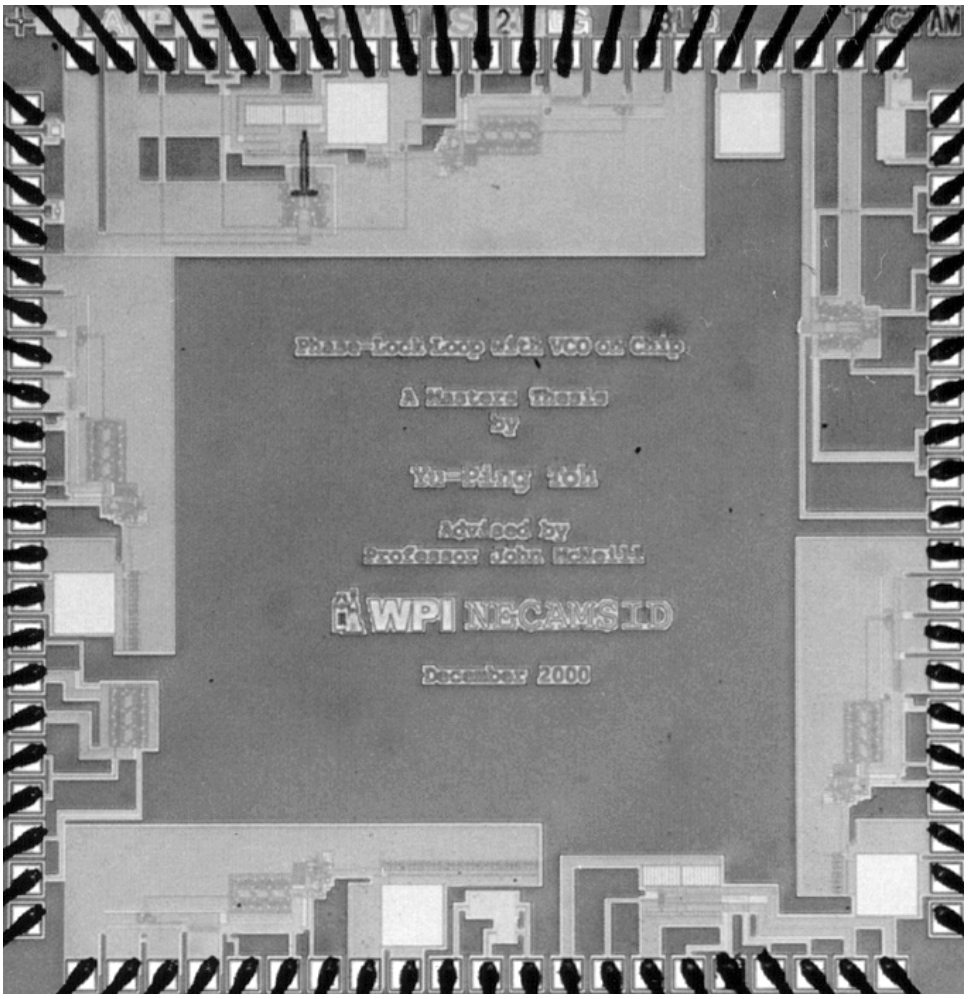

Figure A.25. Chip micrograph.

A.6 Evaluation Board Design

In order to test the chip, an evaluation board had to be designed and fabricated. Considerations for the board design include:

- Ensuring minimum-length traces from the VCO output pins to the SMB connectors.
- Adequate by-pass capacitance placed as close to the supply pins as possible.
- Continuous ground plane throughout the underside of the board.

Figure A.26 shows the layout of the evaluation board.

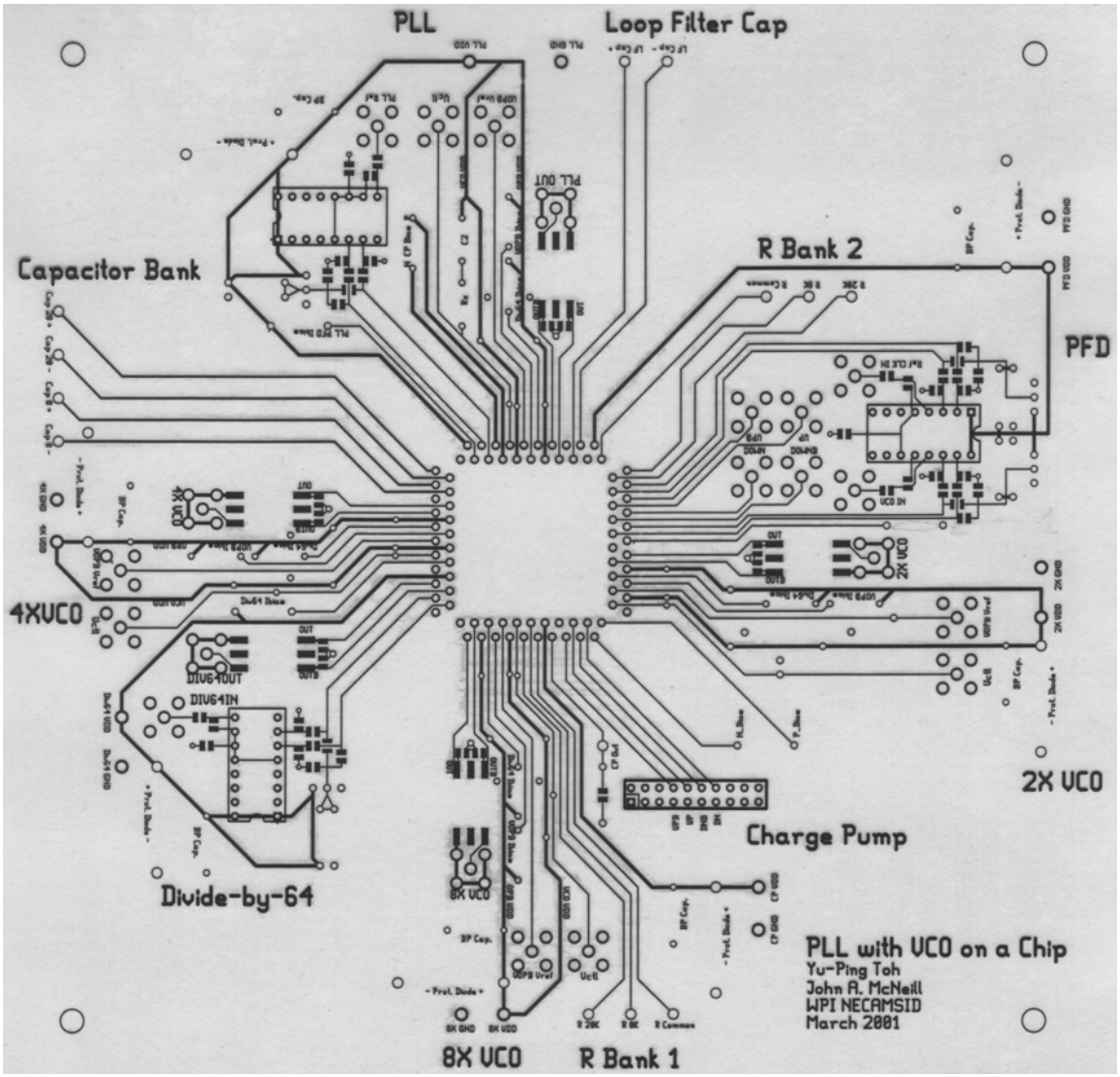

Figure A.26. Layout of the evaluation board.

Appendix B Effect of Mismatch in Interpolating Resistors

This appendix describes the effect of mismatch in interpolating resistors on the accuracy of the phase interpolation technique.

Consider the interpolating network shown in Figure B.1.

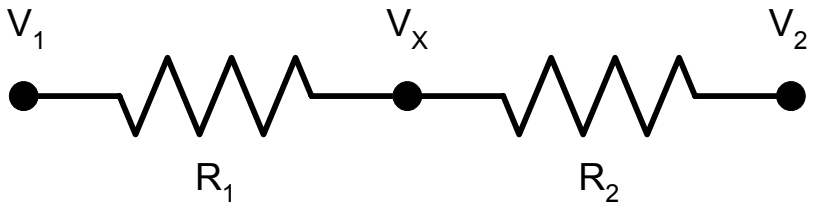

Figure B.1. Interpolating network.

In general, the interpolated voltage V_X will be given by:

$$V_X = \left(\frac{R_2}{R_1 + R_2}\right)V_1 + \left(\frac{R_1}{R_1 + R_2}\right)V_2 \tag{B.1}$$

Defining mismatch variables for R_1 and R_2

$$\Delta R = R_1 - R_2 \tag{B.2}$$

$$R = \frac{R_1 + R_2}{2} \tag{B.3}$$

allows us to express R_1 and R_2 in terms of ideal and mismatch components:

$$R_1 = R + \frac{\Delta R}{2} \tag{B.4}$$

$$R_2 = R - \frac{\Delta R}{2} \tag{B.5}$$

Substituting B.4 and B.5 into B.1 gives

$$V_X = \left(\frac{R - \frac{\Delta R}{2}}{2R} \right) V_1 + \left(\frac{R + \frac{\Delta R}{2}}{2R} \right) V_2 \tag{B.6}$$

which can be rearranged as follows:

$$V_X = \underbrace{\frac{1}{2}(V_1 + V_2)}_{DESIRED} + \underbrace{\frac{1}{4}\frac{\Delta R}{R}(V_2 - V_1)}_{MISMATCH\ ERROR} \tag{B.7}$$

We will examine the two interpolation cases separately. First, the interpolation between two phases of the ring: for mathematical convenience, we will represent V_1 and V_2 as

$$V_1 = V_{PK} \sin(\omega t - \phi) \tag{B.8}$$

$$V_2 = V_{PK} \sin(\omega t + \phi) \tag{B.9}$$

with sinusoid frequency ω, peak amplitude V_{PK}, and ignoring the DC average V_A. The total phase difference is 2ϕ, which would be 120° in the case of a three-stage ring. Substituting (B.8) and (B.9) into (B.7), gives

$$V_X = \underbrace{\frac{1}{2}\left(V_{PK}\sin(\omega t-\phi)+V_{PK}\sin(\omega t+\phi)\right)}_{DESIRED}+\underbrace{\frac{1}{4}\frac{\Delta R}{R}\left(V_{PK}\sin(\omega t+\phi)-V_{PK}\sin(\omega t-\phi)\right)}_{MISMATCH\ ERROR} \quad (B.10)$$

and using the trigonometric identity sin(A+B)=sinAcosB+cosAsinB gives

$$V_X = \underbrace{V_{PK}\sin(\omega t)\cos(\phi)}_{DESIRED}+\underbrace{\frac{1}{2}\frac{\Delta R}{R}V_{PK}\cos(\omega t)\sin(\phi)}_{MISMATCH\ ERROR} \quad (B.11)$$

Examination of (B.11) shows that the mismatch error results in a cos(ωt) term in quadrature with the desired term. This will lead to a phase error in the interpolated signal. In the specific case of a three-stage ring with a total phase difference of 2ϕ = 120°, substituting ϕ = 60° into (B.11) gives

$$V_X = \underbrace{\frac{V_{PK}}{2}\sin(\omega t)}_{DESIRED}+\underbrace{\frac{\sqrt{3}}{4}\frac{\Delta R}{R}V_{PK}\cos(\omega t)}_{MISMATCH\ ERROR} \quad (B.12)$$

Expressing (B.12) in polar form (assuming mismatch ΔR/R small) gives

$$V_X = \frac{V_{PK}}{2}\sin(\omega t+\Delta\phi) \quad (B.13)$$

in which the phase error $\Delta\phi$ is obtained from the rectangular-to-polar conversion (using the small angle approximation) as follows:

$$\Delta\phi = \tan^{-1}\left(\frac{\frac{\sqrt{3}}{4}\frac{\Delta R}{R}V_{PK}}{\frac{V_{PK}}{2}}\right) \approx \frac{\sqrt{3}}{2}\frac{\Delta R}{R} \tag{B.14}$$

The result in (B.14) gives the phase error in radians. This result indicates that the matching requirements are modest: a fractional mismatch of 4% corresponds to a phase error of

$$\Delta\phi \approx \frac{\sqrt{3}}{2}(0.04) = 0.035 rad = 2° \tag{B.14}$$

In the case of interpolation between one phase of the ring and the waveform average: for mathematical convenience, we will represent V_1 and V_2 as

$$V_1 = V_{PK}\sin(\omega t) \tag{B.15}$$

$$V_2 = 0 \tag{B.16}$$

Substituting (B-15) and (B-16) into (B-7), gives

$$V_X = \underbrace{\frac{1}{2}\left(V_{PK}\sin(\omega t)\right)}_{DESIRED} + \underbrace{\frac{1}{4}\frac{\Delta R}{R}\left(-V_{PK}\sin(\omega t)\right)}_{MISMATCH\ ERROR} \tag{B.17}$$

which can be expressed as

$$V_X = \underbrace{\frac{1}{2}\left(V_{PK}\sin(\omega t)\right)}_{DESIRED}\left[1+\frac{1}{2}\frac{\Delta R}{R}\right] \tag{B.17}$$

which gives for the fractional amplitude error

$$\frac{\Delta V}{V} = \frac{1}{2}\left(\frac{\Delta R}{R}\right) \tag{B.18}$$

The results in (B.18) indicate that the matching requirement is modest: a fractional mismatch of 2% corresponds to a fractional amplitude error of 1%.

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