# Design of Low Noise, Low Power Linear CMOS Image Sensors

by

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# Abstract

The implementation of active pixel based image sensors in CMOS technology is becoming increasingly important for producing imaging systems that can be manufactured with low cost, low power, simple interface, and with good image quality. The major obstacle in the design of CMOS imagers is Fixed Pattern Noise (FPN) and Signal-to-Noise-Ratio (SNR) of the video output. This research focuses on minimizing FPN and improving SNR in linear CMOS image sensors which are needed in scanning and swiping applications such as finger print sensing, spectroscopy, and medical imaging systems. FPN is reduced in this research through the use of closed loop operational amplifiers in active pixels and through performing Correlated Double Sampling (CDS). SNR is improved by increasing the pixel saturation voltage.

This thesis concludes that FPN can be reduced using the closed loop opamp buffers. The major FPN noise sources are the shot noise from the photodiode, $k$TC noise from the sampling capacitors, and offset mismatches in the sample and hold amplifiers all of which are not compensated by CDS. Sample and hold amplifier offset mismatch is identified as the largest contributor to FPN.

The digital interface issues of CMOS imagers are also studied. The design of a 12-bit pipelined analog-to-digital-converter (ADC) in standard CMOS technology is presented. The integration of this ADC onto the imager chip would result in a digital image sensor.

# Acknowledgments

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# Chapter 1

# Introduction

## 1.1 Motivation

Over the past decade, developments in image-sensor technology brought new image capture equipment to the market. Camcorders and Digital Cameras are the well known products of this development. At the same time due to improvements in wireless and portable electronics, there is increasing demand for miniaturized, low-power and cost efficient imaging systems. This trend has led to a shift in technology from Charge Coupled Device (CCD) based image sensors to Complementary Metal Oxide Semiconductor (CMOS) based imagers. This is mainly because CMOS-based image sensors offer the potential opportunity to integrate low-power signal processing circuitry on-chip and hence reduce component and packaging cost. There is also great demand for wide dynamic range, high fill-factor and high resolution image sensors in some applications such as spectroscopy and fingerprint sensors. These specific applications employ scanning and swiping methods to capture images and hence a linear image sensor is preferred to area format image sensor.

Digital interface of the imager chip is essential to overcome system level issues such as signal integrity. To implement digital interface to the imager chip requires an on-chip analog to digital converter. This research presents a new linear image sensor architecture

and circuit techniques that lead to low power, wide dynamic range, high fill-factor and high resolution linear image sensor with digital interface. The proposed circuit design is based on a standard $0.4\mu m$ CMOS process to further reduce cost of the imager chip.

## 1.2 Image Sensor Terminology

The definition of most commonly used terms in solid state image sensors is given below

**Charge-coupled device (CCD):** CCD is a charge transfer device that collects light in pixels and then uses clock pulses to shift the charge along a chain of pixels.

**Correlated double sampling (CDS):** CDS is the technique of taking two samples of a signal closely spaced in time and subtracting the first signal from the second to remove the low frequency correlated noise.

**Dark current:** The signal charge that the pixel collects in the absence of light divided by the integration time.

**Dynamic range:** It is ratio of the saturation signal to the root mean square (rms) noise floor of the sensor.

**Fill factor:** It is the ratio of light sensitive area to the pixels total area.

**Fixed pattern noise (FPN):** It is the noise due to mismatch in the properties - transistor thresholds, gain, parasitic capacitance, pixel geometry - of pixels.

**Integration time:** It is the time that the sensor is exposed to light to integrate the photo generated signal charge.

**Microlens:** It is a lens etched directly on the chip's surface for each pixel to focus the light on to the light sensitive area of the pixel.

**Photocurrent/photocharge:** It is is current/charge generated due to the exposure of silicon to light.

**Photosite:** It is the portion of the silicon that functions as a light-sensitive area.

**Pixel:** It is discrete photosensitive cell that collects and holds a photocharge.

**Quantum efficiency:** It is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area.

## 1.3 Organization of thesis

An overview of the existing image sensor technology and a comparison of different available technologies is given in chapter 2. Chapter 3 presents the design techniques for CMOS imagers. The details of the proposed architecture are given in chapter 4, while prototype design and experimental results of the test chip are presented in chapter 5. Digital interface of the imager using a 12 ADC architecture is presented in chapter 6 and conclusions are drawn in chapter 7.

# Chapter 2

# Image Sensor Technology

The solid state imaging devices depend on the photovoltaic response of silicon when exposed to light. Based on this principle, initial research in the 1960's led to the development of Metal Oxide Semiconductor (MOS) image sensors [1]. Different solid state image sensors - computational sensor [2], scanistor [3], phototransistor [4] - with varying degrees of success were reported. All these sensors suffered from low sensitivity as there was no mechanism for photocharge integration. Even though a sensor based on photo flux integration in a p-n junction [5] was discovered, and further developments [6] , [7] in this area resulted thereafter, the biggest problem with MOS image sensors - Fixed Pattern Noise (FPN) - was explored almost at the same time[8]. Later, with the invention of CCDs - in 1970 [9] - which were relatively immune to FPN, the main focus of image sensor research shifted to CCD based sensors.

## 2.1 CCD Image Sensor

CCD is a shift register formed by a string of charge storage devices - capacitors. The two processes that are fundamental to the operation of a CCD are charge storage and charge coupling. CCDs are used in photo sensor arrays, memories and signal processing systems

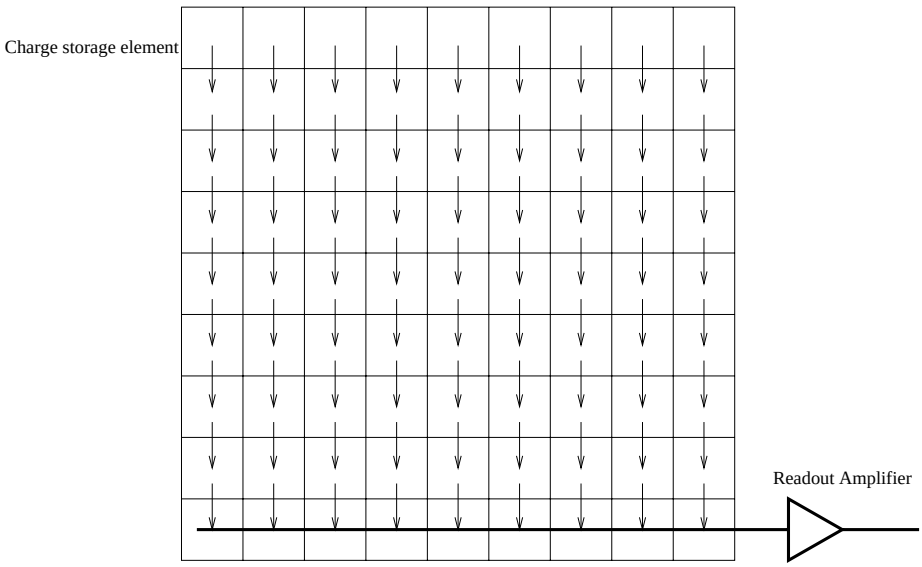


Figure 2.1: Charge transfer in a CCD

and the means of charge accumulation, charge storage and charge transfer varies with the application. For example, charge accumulation in CCDs used as photosensor arrays in imaging applications is due to the capture of light on the light sensitive areas of the CCD called photosites. The photocharge is shifted along a row of pixels to a charge sensitive readout amplifier. Once a row is read, the charge on the above rows is shifted one row down as shown in figure. 2.1. On the next clock pulse, the charge on the last row is again shifted to the readout amplifier. The process of charge storage and charge transfer is described briefly in the following section.

### Charge Storage and Transfer

The charge storage and transfer operation in a CCD is shown in figure 2.2. The charge is stored in a MOS capacitor [9] and the charge is transferred between potential wells at or near a silicon (Si) - silicon dioxide ($SiO_2$) interface [11]. The MOS capacitors (MOSCAP), pulsed by a multi phase clock voltage form these wells. Prior to the application of gate bias to the MOSCAP, there is uniform distribution of majority carriers - holes in p-type

semiconductor. The application of positive step voltage to the gate of the MOSCAP forms a depletion region in the p-type substrate beneath a gate. This particular gate causes a minimum of electron energy - a potential well - to exist at the $Si - SiO_2$ interface. However the potential well will be filled either with photo generated electrons or thermally generated ones. The introduction of minority-carrier signals reduces the depth of the well. The charge filled in the well can be transferred to the adjacent well by clocking the adjacent gate. Thus the direction of charge transfer is determined by the clock-phase sequence. More elaborate analysis of the operation and physics of CCDs is given in [12] and [13].

## 2.2 CMOS Image Sensor

Even though CMOS Image Sensors appeared in 1967, CCDs have prevailed since their invention in 1970. However the major problem with CCDs is that they are manufactured in foundries using specialized and expensive processes that can only be used to make CCDs, and therefore cannot take advantage of economies of scale general purpose fab. Meanwhile, recent advances in the CMOS technology for microprocessors and Application Specific Integrated Circuits (ASICs) to the development of highly integrated image sensors with on chip signal processing algorithms, sensor array controls and image processing. Also, CMOS is by far the most common, lowest cost and highest yielding process in the world. Using the same process to manufacture CMOS image sensors cuts cost dramatically because of the fixed costs of the plant are spread over a much larger number of devices. As a result of this economy scale, the cost of fabricating a CMOS wafer is lower than the cost of fabricating a similar wafer using the more specialized CCD process.

### CMOS Image Sensor Architecture

A CMOS image sensor consists of an array of pixels that are typically selected a row at a time by row select logic. This logic can either be a shift register or a decoder. The pixels

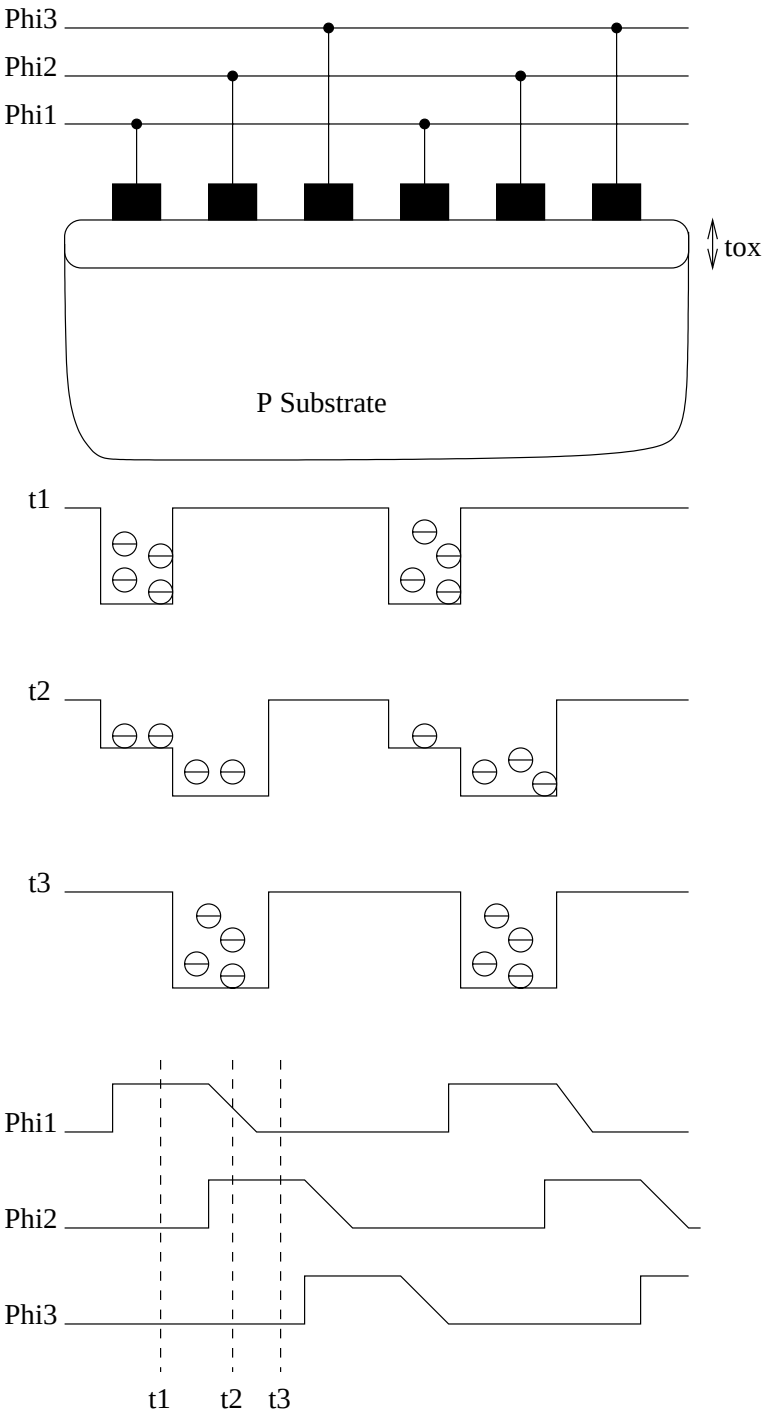


Figure 2.2: Charge storage and transfer in a CCD

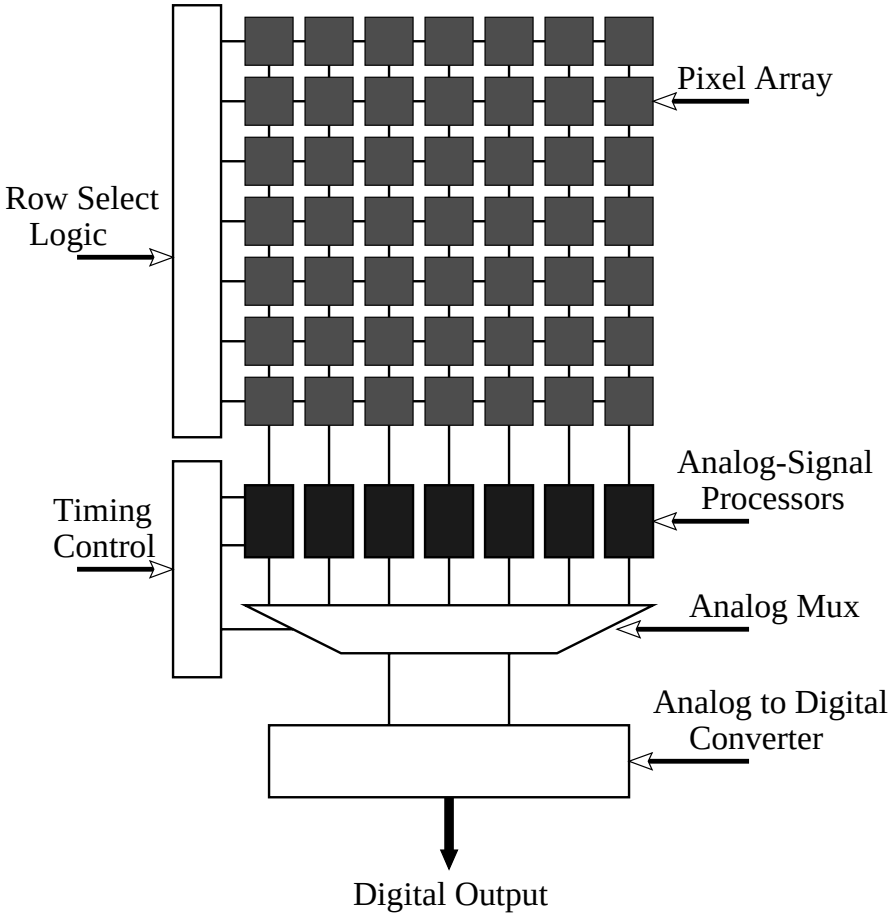


Figure 2.3: CMOS image sensor architectural block diagram

are read out to the vertical column busses that connect the selected row of pixels to column-parallel analog signal processing blocks which perform functions such as sample and hold, correlated double sampling and fixed pattern noise (FPN) suppression. In order to provide digital interface of the imager chip, some image sensors contain on-chip analog to digital converters (ADC). The generic architectural block diagram of a CMOS image sensor is shown in figure 2.3. The row select logic and timing control unit are also integrated on to the chip. The timing control unit generates the timing signals for sample and hold and correlated double sampling (CDS). The analog multiplexer performs column-select operation on the bank of analog signal processors. The analog output is converted into its digital equivalent

by the on-chip analog to digital converter.

## 2.3 CMOS VS CCD

The subtle differences in the methods of imaging the light and techniques of reading out signal charges between CMOS and CCD image sensors result in wide differences in their performance. The most important differences between the CCD and CMOS image sensors are in their noise performance, sensitivity, power consumption, dynamic range, compatibility with integration of on-chip electronics and cost.

### Noise

The noise introduced into the output video signal by the image sensors and associated circuitry is the greatest factor that limits operation at low light levels. This noise which masks small photosignals in both types of arrays, comes from mismatches in parasitic capacitances and thermally generated carriers. Moreover, CCDs suffer noise from transfer loss [14].

### Fixed Pattern Noise

In MOS image sensors, FPN noise results from mismatches between threshold voltages of the transistors and parasitic gate-source, gate-drain capacitances. Values of noise are in the $1 - 5\,mV_{rms}$. While CCDs are not affected by FPN from the mismatch of transistors, they have fixed pattern noise resulting from capacitance between clock lines and output lines. The noise resulting from this can be filtered using a low-pass filter.

### Transfer Noise

The transfer-loss noise is the result of charges left behind after the transfer operations and hence predominant in CCD imager sensors. This noise is most noticeable when large quantities of charges are transferred, corresponding to high intensity levels. It appears as a

white smear in the sensed image. The transfer noise is not present in MOS image sensors as the sensed charge is converted to voltage and then multiplexed.

### Supply Voltage

CCDs require multiple voltage supplies to transfer charge from pixel to pixel and an additional supply to reduce dark-current noise - using surface state pinning - which is partially responsible for CCDs high sensitivity and dynamic range. Meanwhile, CMOS image sensors require only one supply voltage compared with the three or four that CCDs need.

### Power Consumption

Even though a CCD image sensor chip consumes less power than the CMOS imager, CCD support circuits use more power compared to that of CMOS. This is mainly because support circuits are integrated on-chip in CMOS imagers, while in CCD image sensors the support circuits are off-chip and hence have to drive large capacitive interconnects and loads at high voltages. Power consumption in a CMOS based system is about 100 times less than that of the CCD based system.

### Readout Mode

CMOS imagers allow various modes of readout - windowed readout, scanning readout, accelerated readout. On the other hand CCDs perform readout by transferring the charge from pixel to pixel (figure 2.1) that requires reading the entire array of pixels.

### Sensitivity

CCD image sensors have greater sensitivity and thus require smaller integration time. CMOS pixels that incorporate active transistors have reduced sensitivity to incident light because of less light sensitive area.

### Dynamic Range

The dynamic range of CCDs is larger than that of CMOS pixels because of lower dark current and higher sensitivity of CCDs. The lower dark current in CCDs is achieved by employing surface-state pinning.

### Fill factor

CMOS based pixels typically have a 20 to 30 percent fill factor while that of CCDs is more than 80 percent. This is mostly due to integration of circuitry into the pixel area in CMOS based pixels. To counter the low fill factor, the CMOS based pixels can use micro lens to improve fill factor.

### Quantum Efficiency

Reduced sensitivity of CMOS pixels reduces the quantum efficiency to far less than that of CCDs of the same pixel size. CMOS pixels achieves quantum efficiencies that peak between 30 - 35 percent in the red and near infrared region of the spectrum [15].

### Cost

Due to latest developments in CMOS technology, CMOS sensors have the ability to integrate timing control units, analog signal processors and digital signal processors on a single chip. The integration of all the support circuits lead to low-cost and smaller products compared to that based on CCDs. But due to additional process steps required for color filtering and micro lens deposition, the cost advantage of standard CMOS processing over CCDs is unclear.

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# Chapter 3

# Design Techniques for CMOS Image Sensors

A CMOS image sensor chip typically consists of a front-end circuitry which first receives the photocurrents and an analog signal processing circuitry to process the detected signal. In general, the way the input photocurrent is processed depends on the overall architecture of the image sensor chip. This chapter discusses various front-end design techniques and also presents back-end analog processing techniques to suppress low frequency flicker noise and fixed pattern noise.

## 3.1 Front-end Design

The block diagram of the front-end circuit is shown in figure 3.1 . In general, the front-end of a CMOS image sensor consists of a photodetector and a buffer to prevent the loading of the sensitive sense node. The sense node is reset by a reset switch at the start of photocharge integration. The photocharge is converted to a voltage ($V = Q/C$) by the parasitic capacitance ($C_{total}$) at the sense node. The parasitic capacitance $C_{total}$, is the sum of input capacitance ($C_{in\_buf}$) of the buffer and the parasitic capacitance associated with

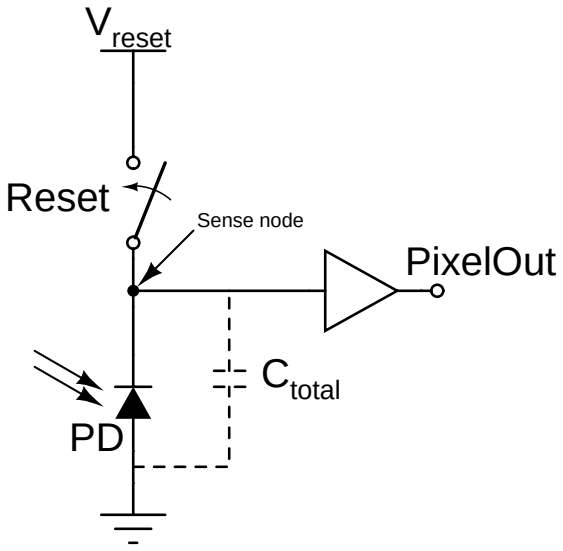



Figure 3.1: Front-end block diagram of a CMOS image sensor

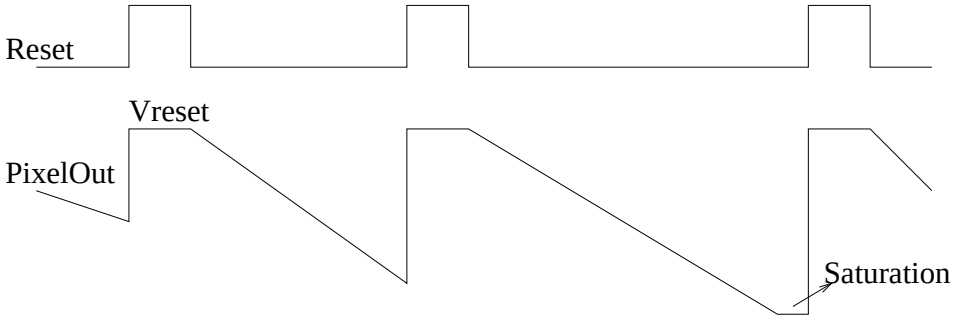



Figure 3.2: Operation of the imager front-end

the photo detector ($C_{PD}$). The operation of the front-end is demonstrated in figure 3.2 . This front-end is often referred to as Active Pixel Sensor (APS) because of the presence of the active amplifier (buffer) in the pixel. In contrast to the active pixel sensors, there are Passive Pixel Sensors (PPS) which do not contain any active amplifier in the pixel. Even though PPSs are used in various image sensor chips [1],[2],[3], more recent CMOS image sensor chips employ APS based arrays due to potential improvement in the performance of the pixel. The CMOS APS trades fill factor for improved performance compared to PPS. Loss in optical signal due to reduction in fill factor is more than compensated by reduction

in read noise for a net increase in signal-to-noise ratio and dynamic range [1]. The following sections describe the issues involved with reset switch, photo detector and buffer design.

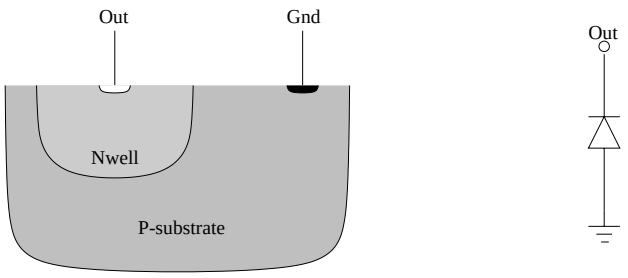
### Reset switch design

The reset switch periodically resets the sense node to a particular bias voltage. The reset switch can be implemented either using a n-channel MOS (NMOS) transistor or a p-channel MOS (PMOS) transistor. A transmission gate is not generally used since the size of the reset switch directly affects the fill factor of the pixel. The major issues involved with the MOS reset switch are output swing limitation due to back bias of the NMOS transistor in N-well process when biasing the sense node to positive rail voltage (and similarly PMOS transistor in P-well process when biasing the sense node to negative rail voltage), fixed pattern noise (FPN) due to threshold variations from pixel to pixel, dark current resulting from the off-current of the reset transistor.

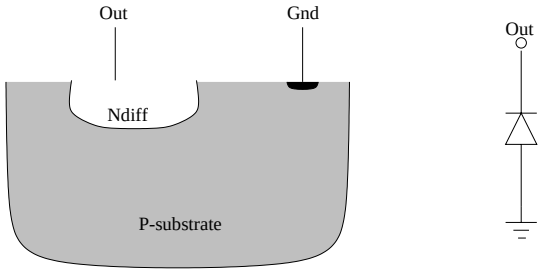
The output swing of any photodiode based pixel is in the range of 1 - 1.5V. So for supply voltages of 3.3V and above the output swing is not limited by back bias of reset transistor. On the other hand increase in threshold voltage reduces off-current and hence reduces dark current. Short range threshold voltage tracking - to reduce FPN - can be significantly improved using gate lengths slightly larger than the minimum gate length [5]. For example, in a 3.3.V Nwell 0.35$\mu m$ CMOS process, an NMOS transistor with length equal to 0.4$\mu m$ can be chosen to bias the sense node to positive rail. Such a choice would result in biasing the sense node to about 2.6 V with reduced FPN and dark current.

### Photodetector design

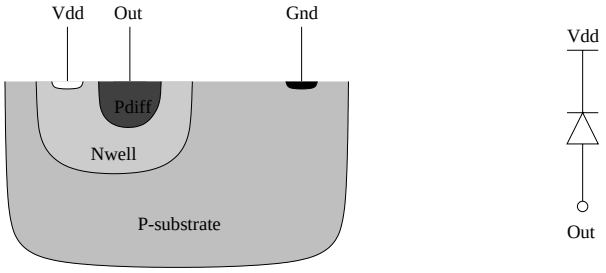
In a standard CMOS process, either Pwell or Nwell, several parasitic junction devices can be used as photo detecting elements [6]. A few commonly used photodetectors in CMOS technology are presented in figure 3.3. The photo response of the detector varies with the wavelength of the incident light. The diffusion-substrate junction diodes are very shallow



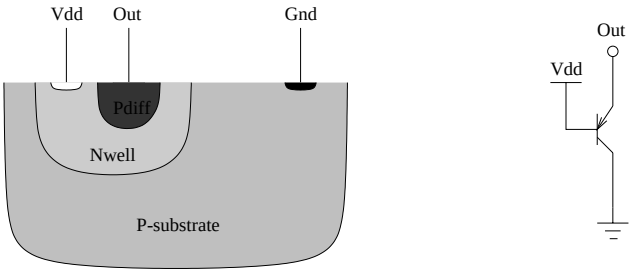

(a) Well - Substrate junction photodiode




(b) Diffusion - Substrate junction photodiode




(c) Well - Diffusion junction photodiode




(d) Vertical bipolar phototransistor

Figure 3.3: Photodetectors in CMOS technology

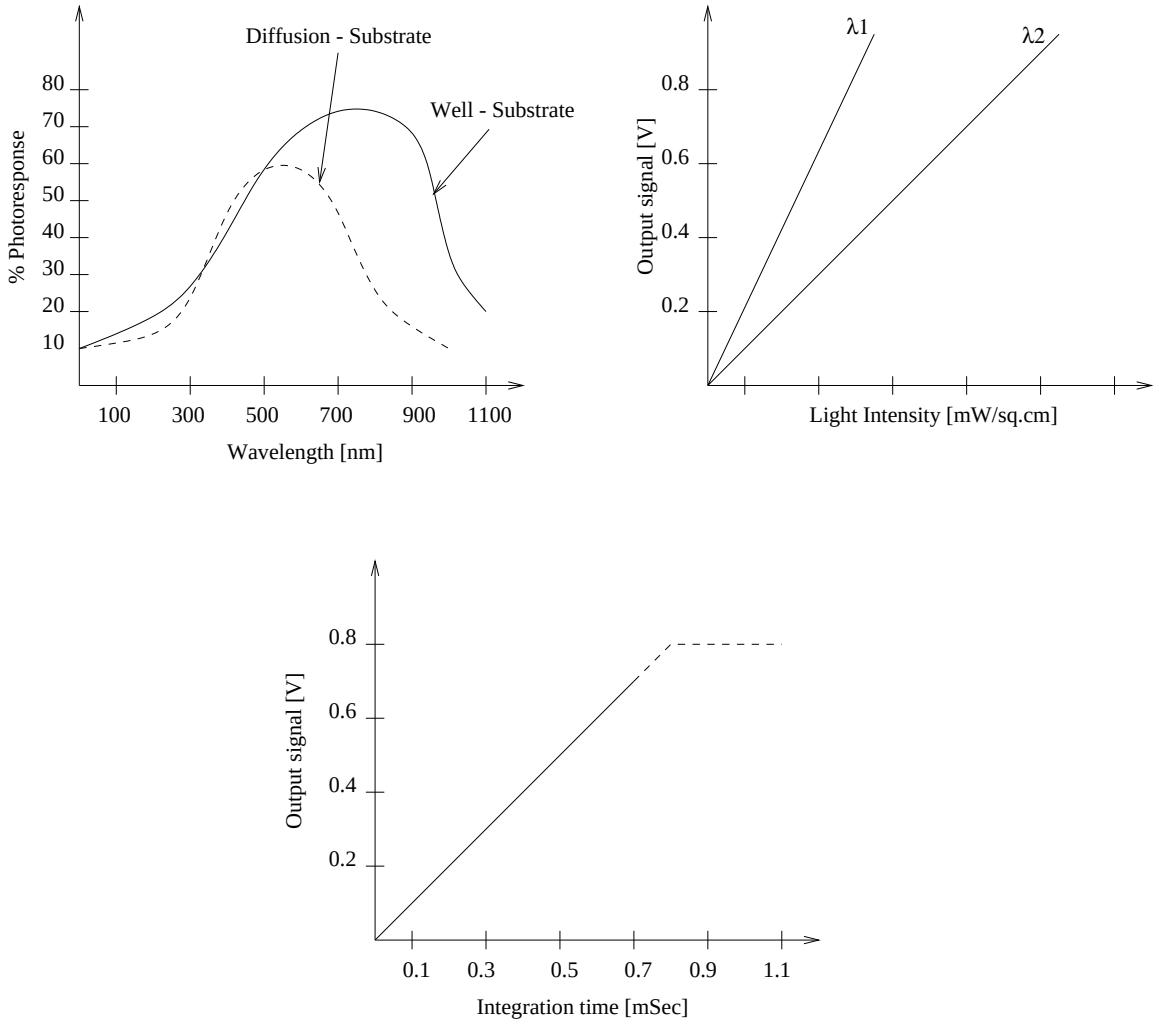



Figure 3.4: Performance characteristics of a photodiode

in advanced CMOS technologies. The shallow junction degrades the photo response of the diode and are therefore used at short wavelengths. The well-substrate junction diodes have broader depletion region because of the light impurity concentration of the well as compared to that of diffusion. Also well-substrate junction is deeper than diffusion-substrate diodes and hence has greater photon collection efficiency at longer wavelengths [7]. The output signal of the pixel is proportional to the intensity of light and integration time. Typical performance characteristics of a photodiode are shown in figure 3.4.

In addition to the photodetectors shown in figure 3.3, photogate [8] is also used as photodetector in some CMOS image sensor chips. Even though photogates have lower noise and higher conversion gain compared to photodiodes, they have lower quantum efficiency and larger pixel size [9]. Also since they are less compatible with CMOS technologies, photodiodes are being most often used.

### Buffer design

A buffer is used to prevent the loading of the sensitive sense node (see figure 3.1 on page 15). The buffer design issues, their implications on the image sensor performance and remedies to improve the performance are listed below

- The input capacitance of the buffer adds up to the total charge-to-voltage conversion capacitance at the sense node. So the input capacitance of the buffer should be minimized to maximize sensitivity of the pixel
- The area of the buffer trades with the fill factor of the pixel. So area of the buffer should be minimized to improve fill factor
- The non-unity buffer gain results in either loss or gain of the signal. In order to prevent the loss of signal, the buffer gain should be at least unity
- The input range of the buffer should be large enough to prevent clipping of the output
- The buffer noise directly affects the dynamic range of the sensor. So low-noise design techniques should be employed

Due to the area constraint on the buffer size, most of the CMOS image sensors [8] , [10] use source follower based unity gain buffers as shown in figure 3.5 . A nominal bias current of $10\mu A$ can be chosen to keep the size of the input device low. The major limitations of source follower are it has limited output swing and there is loss of signal due to the

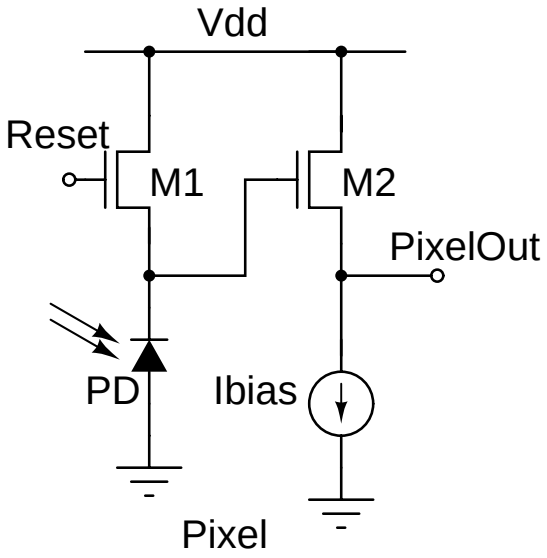



Figure 3.5: Source follower buffer based pixel

less-than-unity gain of the source follower. Also bias current variation and W/L mismatch due to process variation changes gain of the source follower, which appears as FPN of the imager. To circumvent these limitations, closed loop operational amplifiers can be used at least in linear image sensors where there is no limitation on the size of the active circuitry in the pixel.

## 3.2 Analog Signal Processor Design

On-chip analog signal processing is used to improve the performance and functionality of the image sensor. The most frequently used signal processing technique to suppress FPN is Correlated Double Sampling (CDS) [11]. In addition to CDS various other signal processing techniques are also demonstrated in recent CMOS image sensors - Double Delta Sampling [8], programmable amplification [12], video compression [13], dynamic range enhancement [14], discrete cosine transform [15], and intensity sorting [16]. The following section presents the CDS technique in detail.

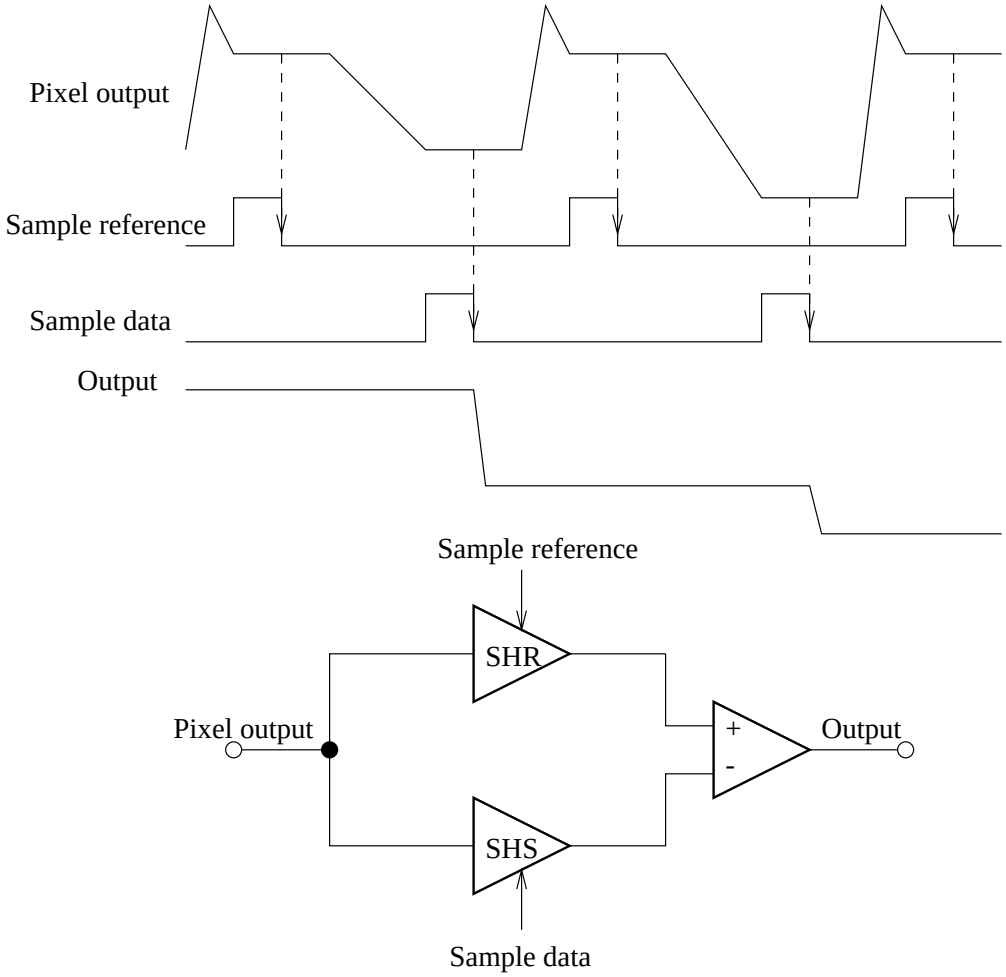



Figure 3.6: Timing and implementation of CDS

### Correlated double sampling

Correlated double sampling is a pseudo-differential-in-time technique in which the pixel output is sampled twice at different times during the pixel period and the output is the difference of the two samples. The first sample is generally the reference level and the second sample corresponds to the data signal. This pseudo differential sampling removes the correlated noise between the reference and the data signals. Furthermore, a noise source that is not correlated, but is slowly varying between the two samples will be reduced in magnitude. Figure 3.6 illustrates CDS scheme.

Noise in CMOS image sensors primarily consists of $k$T/C noise from the parasitic capacitance at the sense node, flicker ($1/f$) noise and white noise from the pixel buffer. Threshold mismatches in the reset switches and pixel buffer offsets also appears as noise on the output of the sensor. Such a noise is often referred to as fixed pattern noise. The $k$T/C noise is present during the sampling of both the reference and the data level. Therefore it is correlated and hence remove by CDS. Low frequency noise like $1/f$ noise, and other noise introduced from power supplies and substrate is also attenuated by CDS. Also FPN is cancelled by CDS.

CDS does not reduce the FPN due to dark current, uncorrelated high frequency temporal noise, and the optical shot noise. Second order effects due to gain non-linearity are also not corrected by CDS.

## 3.3 Readout Amplifier Design

Several readout modes - progressive-scan readout, window readout and skip readout - can be easily implemented in CMOS images sensors. The progressive-scan readout of an area format CMOS image sensor involves selecting a row and then reading out each pixel of the column by addressing them individually. Column readout can be either sequential or non-destructive depending on the application. In sequential readout, pixels in each column are read in a sequential manner while in non-destructive mode, pixels can be read randomly. A shift register is used to generate the control signals for sequential readout and a decoder is used for non-destructive readout. Figure 3.7 illustrates the column readout operation. Window readout and skip readout in which few pixels are readout from the array are less frequently used.

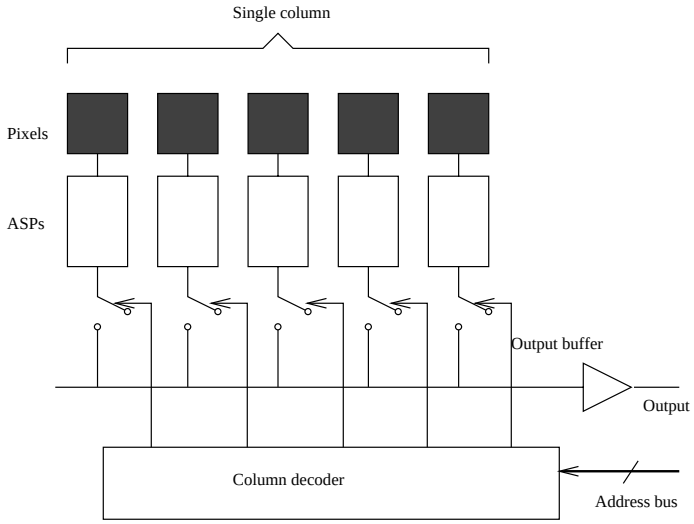



Figure 3.7: Column readout operation

## 3.4 Recent Performance Achievements In CMOS Imagers

Recent performance achievements in CMOS image sensors is summarized in Table 3.1 and Table 3.2

Table 3.1: Recent performance achievements in CMOS image sensors

| Source | Process | Pixels | Pixel size | Die size | Fill factor | Conversion gain |
|---|---|---|---|---|---|---|
| Ho[7] | $0.35\mu m$ | $1332 \times 1034$ | $5\mu m$ | - | 47% | - |
| Decker[17] | $0.8\mu m$ | $256 \times 256$ | - | - | 49% | $13.1\mu V/e^-$ |
| McIlrath[18] | $0.7\mu m$ | $512 \times 768$ | $15\mu m$ | $1cm^2$ | - | - |
| Iida[19] | $0.6\mu m$ | $640 \times 480$ | $5.6\mu m$ | $6.4 \times 5.4\,mm^2$ | 16.8% | $15.0\mu V/e^-$ |
| Nixon[8] | $1.2\mu m$ | $256 \times 256$ | $20\mu m$ | $5.3 \times 5.3\,mm^2$ | - | $10.6\mu V/e^-$ |
| Aw[20] | $1.2\mu m$ | $128 \times 128$ | $24\mu m$ | $3.2 \times 3.2\,mm^2$ | 25% | - |
| Dickinson[21] | $0.9\mu m$ | $256 \times 256$ | $20\mu m$ | $5.3 \times 5.3\,mm^2$ | 25% | $7.0\mu V/e^-$ |
| Fowler[2] | $1.2\mu m$ | $64 \times 64$ | $60\mu m$ | $6.5 \times 5.0\,mm^2$ | 3 % | - |
| Mendis[10] | $2\mu m$ | $128 \times 128$ | $40\mu m$ | $6.8 \times 6.8\,mm^2$ | 26% | $4.0\mu V/e^-$ |

Table 3.2: Recent performance achievements in CMOS image sensors (cont'd)

| Source | Saturation voltage | Dynamic range | Supply | Power | Output |
|---|---|---|---|---|---|
| Ho[7] | 1.2 V | 69 dB | 3.3 V | 165 mW | Analog |
| Decker[17] | 1.69 V | 70 dB | 5 V | 52 mW | Digital |
| McIlrath[18] | 2 V | 52 dB | 5 V | 50 mW | Analog |
| Iida[19] | 0.7 V | 60 dB | 5 V | 30 mW | Analog |
| Nixon[8] | 0.8 V | 75 dB | 5 V | 5 mW | Analog |
| Aw[20] | 0.47 V | 56 dB | 5 V | 100 mW | Analog |
| Dickinson[21] | 1.5 V | 74 dB | 5 V | 80 mW | Analog |
| Fowler[2] | - | 93 dB | 5 V | 1 mW | Digital |
| Mendis[10] | 0.6 V | 71 dB | 5 V | - | Analog |

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# Chapter 4

# Proposed Architecture

The proposed architecture of the linear image sensor is presented in this chapter. Even though, the design issues of CMOS image sensors are presented with respect to area format image sensors they are applicable to linear format sensors also. Nevertheless, linear imagers have an extra degree of freedom - no area constraint in the Y-direction of the sensor since pixels are present only in the X-direction. This extra degree of freedom is exploited in the design to enhance dynamic range, reduce FPN and lower power consumption . The proposed architecture enables two types of readout modes - sequential readout and non-destructive readout. As mentioned earlier, sequential readout is used in scanning/swiping-type imaging applications, while non-destructive readout is used in spectroscopy applications.

## 4.1 System Architecture

The proposed system architecture is shown in figure 4.1. Each pixel consists of a closed loop operational amplifier in unity gain configuration to improve the dynamic range and to prevent the loss of signal compared to that of source-follower based buffers. The opamp should have wide common mode range and open loop gain of at least 100 to prevent signal loss in closed loop configuration. The high open loop gain minimizes variation in closed

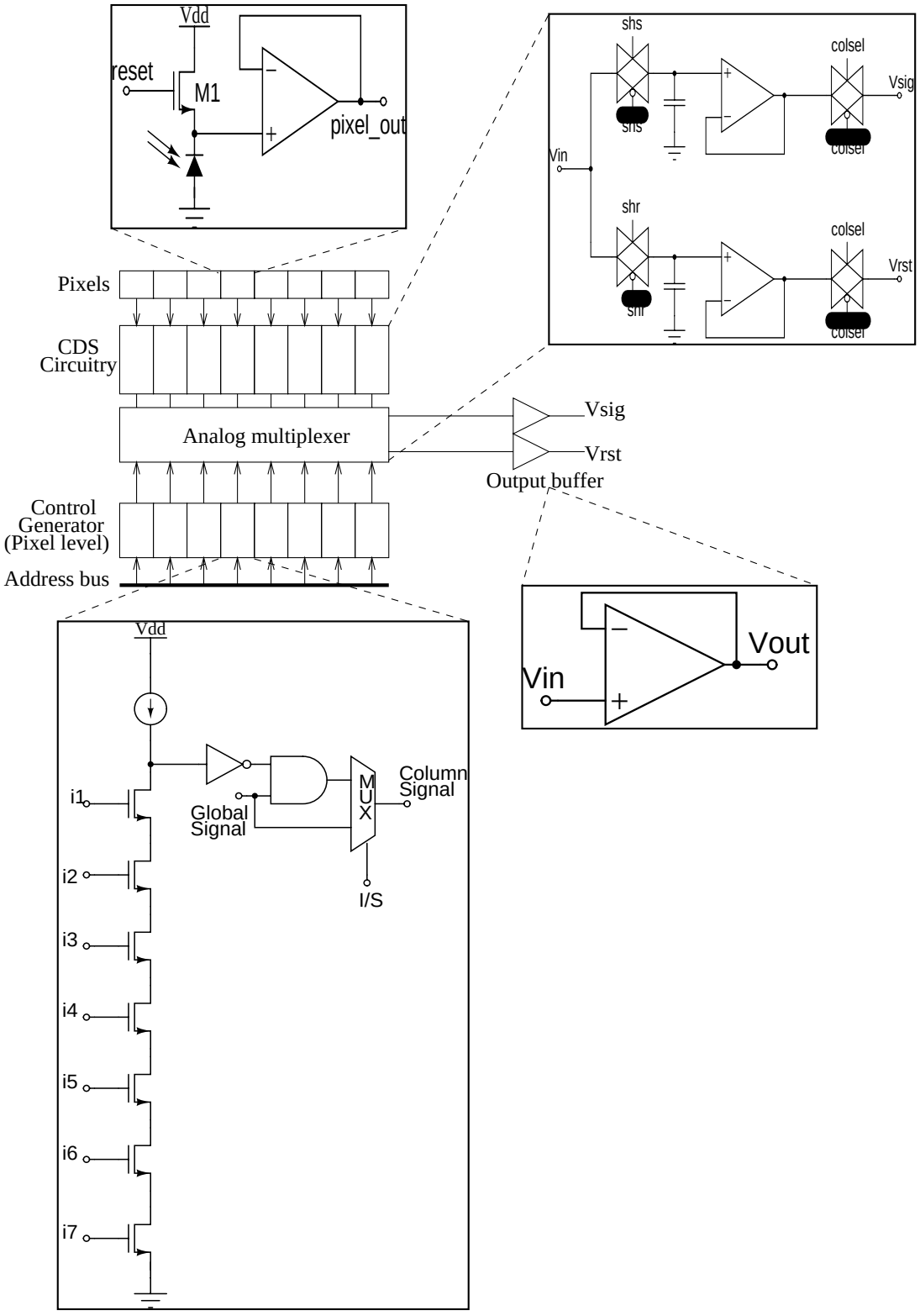



Figure 4.1: Linear image sensor architecture

loop gain due to process variation, thus reducing FPN.

Correlated double sampling is used to suppress FPN. Transmission gates and closed loop opamps are used in sample and hold circuits to preserve the dynamic range. The sampling clocks for the sample and hold circuits and other timing signals required in various readout modes are generated by the pixel level column decoders. The column decoders are realized using a series of NMOS transistors and a current source in order to the fit in the narrow layout constraint imposed by the pixel size. The output buffer is required to drive large off-chip capacitive loads, for example the input capacitance of a high resolution ADC.

## 4.2 Modes of Operation

As mentioned earlier, the proposed image sensor can be operated in two modes of operation depending on the type of readout - sequential readout, non-destructive readout.

### Sequential readout

In this mode of operation, the pixels are readout in a sequential manner after a specific photo charge integration time. The timing diagram for this mode is shown in figure 4.2 . The I/S, PixelAddress, GlobalReset, GlobalSHR, GlobalSHS and PowerDown are input signals external to the chip. Vsig and Vrst are the output signal and reset levels of the imager. I/S signal selects the mode of operation. GlobalReset is used to reset the pixels, GlobalSHR and GlobalSHS are used to sample the reset level and signal levels of the pixels respectively depending on the mode of operation. For example, when I/S is high sequential readout mode is selected and GlobalReset resets all the pixels. On the other hand when I/S is low non-destructive readout mode is selected and only the addressed pixel is reset. GlobalSHR and GlobalSHS function accordingly. The utility of the PowerDown signal is explained in section 4.3. Since the address bus and sampling clocks are external, the photocharge integration time and readout rate can be varied depending on the application. The integration time

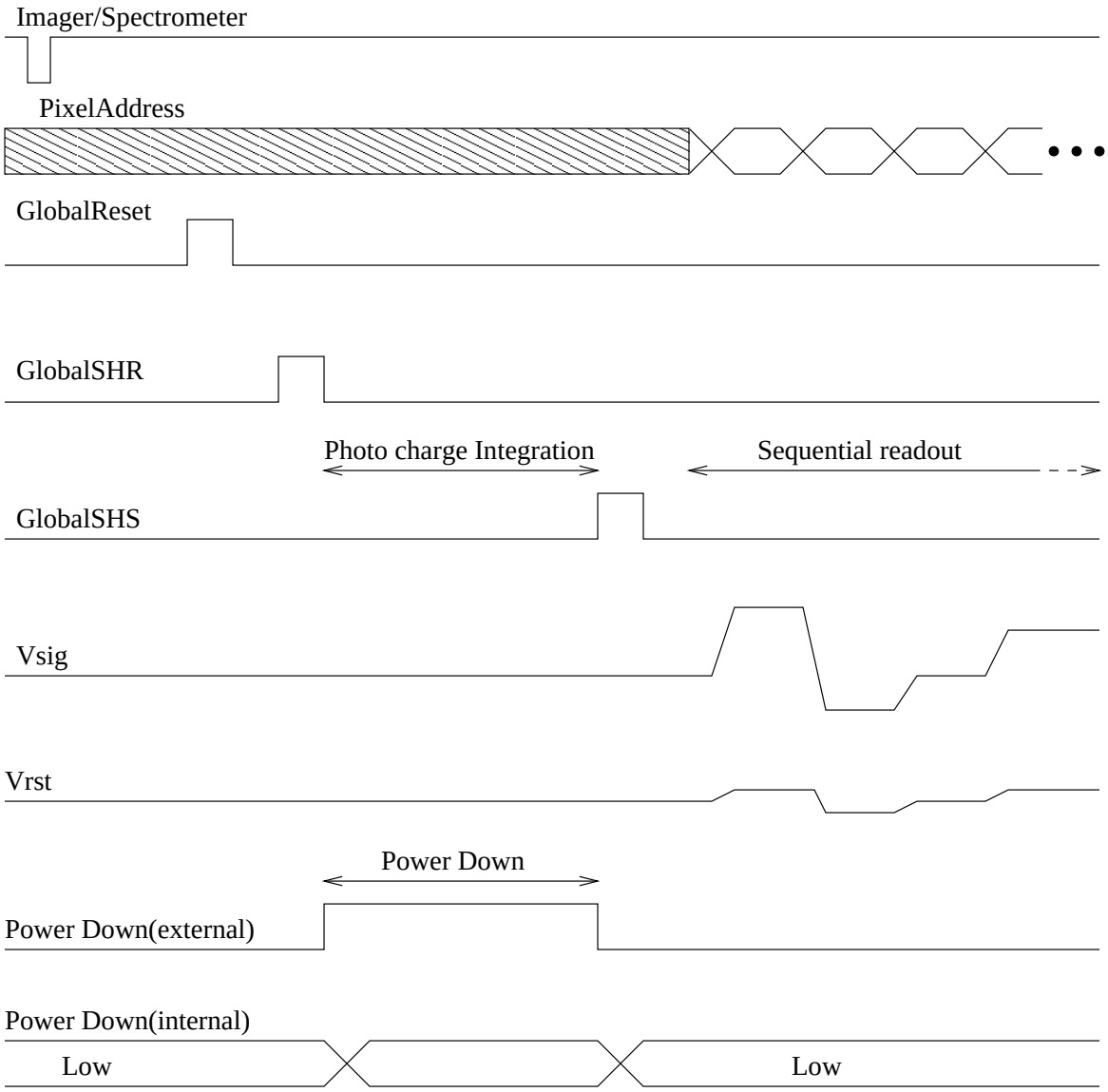



Figure 4.2: Sequential readout timing diagram

Table 4.1: Control signals and their functions

| Signal | Value | Function |
|---|---|---|
| I/S | 1 | Sequential readout mode |
| I/S | 0 | Non-destructive readout mode |
| GlobalReset | 1 | Reset pixel |
| GlobalReset | 0 | Photocharge integration |
| GlobalSHR | 1 | Sample reset level |
| GlobalSHR | 0 | Hold reset level |
| GlobalSHS | 1 | Sample signal level |
| GlobalSHS | 0 | Hold signal level |
| PowerDown | 0 | No power down |
| PowerDown | 1 | Power down |

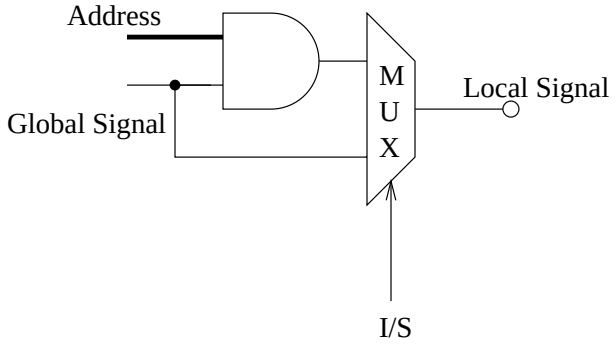



Figure 4.3: Column decoding logic

is determined by the time difference between GlobalSHR and GlobalSHS signals. The functionality of various signals is summarized in Table 4.1.

### Non-destructive readout

In this mode of operation, the pixels can be reset and readout in any random order. This readout mode is particularly useful in spectroscopy application, wherein the "bright" pixels are read more often compared to the "dark" pixels. The control signals to reset, sample and read a particular pixel are generated by "ANDing" the address bus with the appropriate global signal as shown in figure 4.3 . For example, to reset a particular pixel the address of that pixel is "ANDed" with the GlobalReset signal. The timing diagram of this mode of

readout is given in figure 4.4 .

## 4.3 Power Consumption Control

One of the major advantages of the CMOS image sensors over CCD based imagers is the lower power consumption of CMOS circuits. The usage of closed loop opamps in place of simpler two transistor source follower buffers in each pixel increases the power consumption drastically. Moreover, this power consumption increases rapidly with the number of pixels. To circumvent this problem, a power consumption control technique is proposed. This technique is based on the simple observation that all the pixels are not accessed simultaneously and hence the pixels need not be powered on all the time. Therefore, unaccessed pixels can be shut down to save power. This can be achieved by powering down all the appropriate circuits using the address bus and the power down signal as shown in figure 4.2 on page 31 and figure 4.4 on page 34. The major issue with this approach is the startup time of the circuitry. The startup time of the circuits should be much less than the readout time of the pixel. The startup time In any case, the circuits can be powered down during the photocharge integration and can be powered up before the readout. Since the integration time is very large compared to the total readout time, this approach reduces the average power consumption without any issues of startup time. Also, ideally only one pixel is powered on at anytime and the power consumption does not increase with the number of pixels.

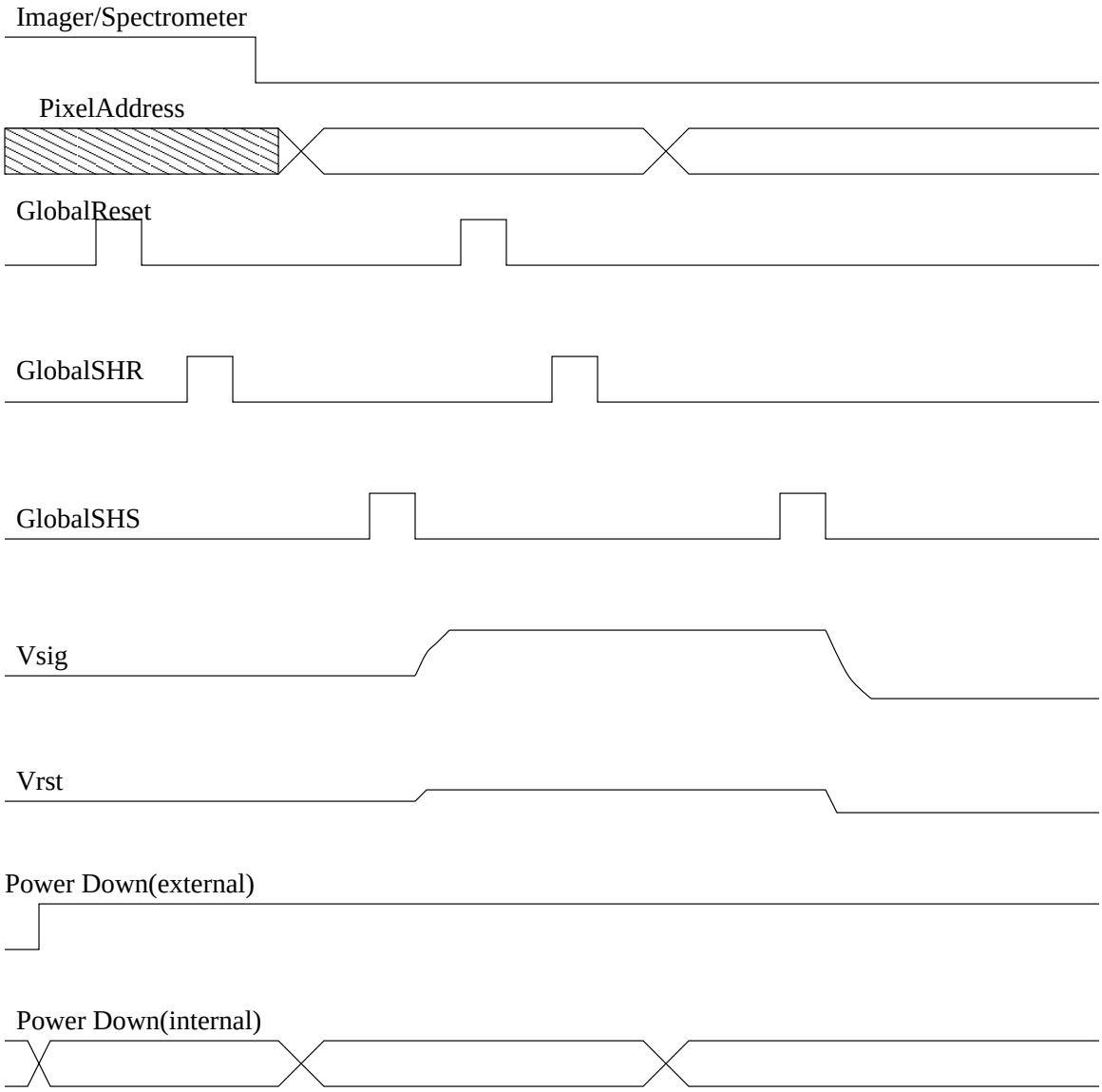



Figure 4.4: Non-destructive readout timing diagram

# Chapter 5

# Prototype Design and Experimental Results

In order to verify the practical feasibility of the proposed architecture a prototype linear image sensor is designed in standard $0.4\mu m$ CMOS process. In this chapter the circuit design of various building blocks and layout issues are presented.

## 5.1 Circuit Design

The building blocks of the image sensor are : pixel buffer, sample and hold amplifier, input/output buffers. The design of each of these building blocks is presented next.

### Pixel buffer

The schematic diagram of the pixel buffer is given in figure 5.1 . A NMOS reset switch is used to reduce the leakage current. A two stage folded cascode opamp (shown in figure 5.2) [1], [2], [7], [4], [5], [6] in unity gain configuration is used as the buffer. The opamp is designed for low input capacitance, high gain, wide common mode input range and large output swing.

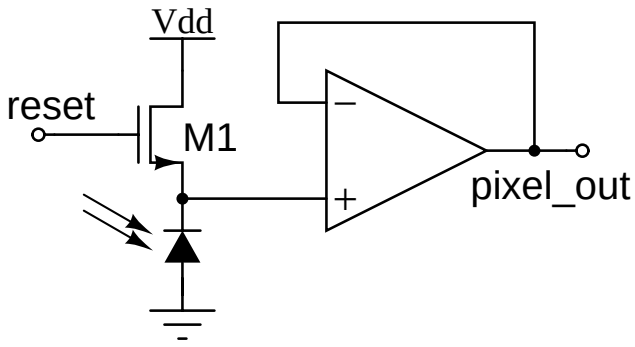



Figure 5.1: Pixel buffer schematic diagram

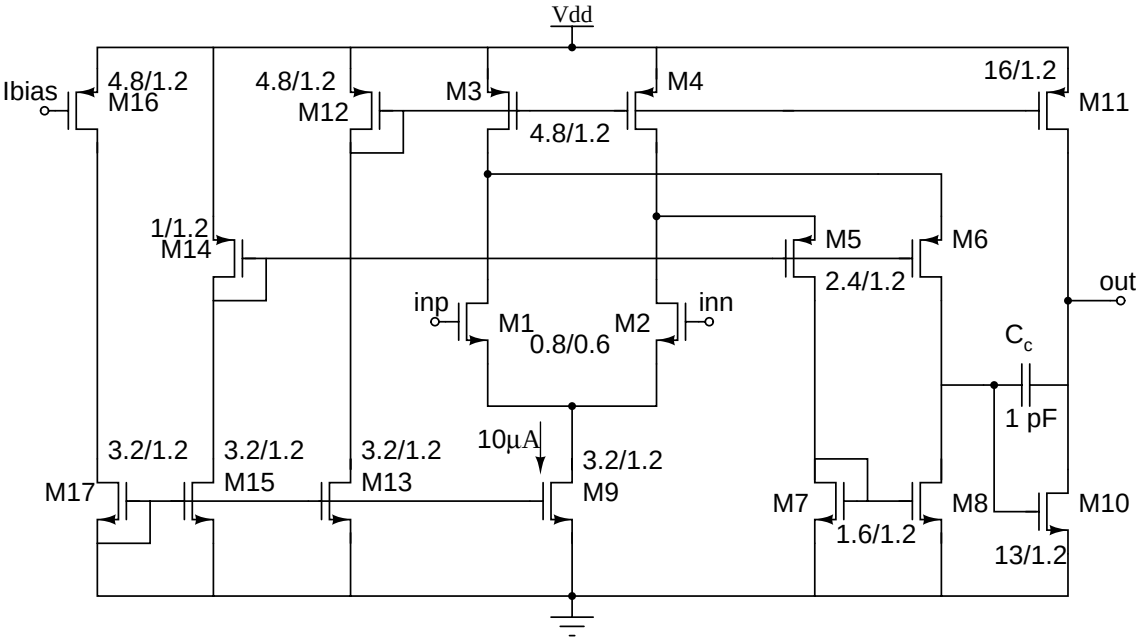



Figure 5.2: Two stage folded cascode opamp (all sizes in $\mu m$)

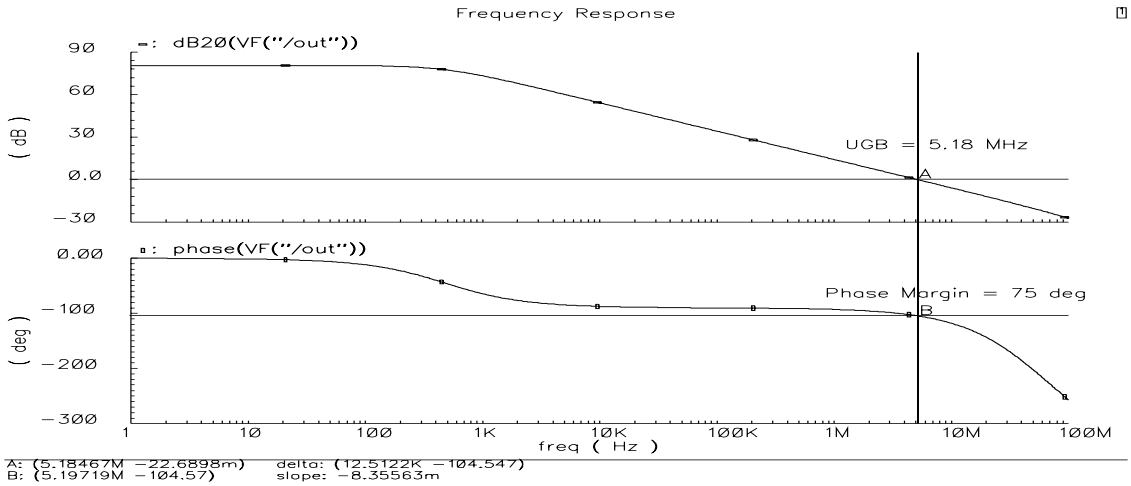
The input transistors M1, M2 are sized for high $g_m$ ($38\mu A/V$) and low $V_{eff} = V_{GS} - V_{TH}$ ($200mV$) for high gain and to reduce the lower limit on the input common mode range(see figure 5.3(b)). The minimum gate length is chosen for these transistor to reduce input capacitance. The offset due to mismatch of the input transistors is reduced by CDS. The output transistors M10, M11 are sized for high gain and large output swing. The cascode transistors M5, M6 and the bias transistors M3, M4, M7, M8 are sized based on the $V_{eff}$ value of M10 transistor. The bias current for the cascode transistors is chosen to be equal to the current in the input transistors. The opamp is miller compensated [7], [8] for a phase margin of 75°(see figure 5.3(a) ). Since the zero is much larger than the unity gain bandwidth, it is not compensated. The compensation capacitor is realized using MOSCAP [9]. The opamp is powered down by pulling up the PMOS transistors and pulling down the NMOS transistors in the power condition. The power down transistors are not shown in schematic.

The noise performance of the opamp is calculated as follows [10]. The equivalent input noise of each transistor is calculated and is referred to the output of the opamp by multiplying the equivalent input noise with the gain to the output of the opamp from the noise source. The equivalent input referred noise is then calculated by dividing the total output noise by the gain of the opamp. Alternatively, the output noise due to each transistor can be referred to the input by dividing the output noise by gain of the opamp and the equivalent input referred noise can be calculated by summing noise contributions of all the transistors at the input in a root mean square fashion. The noise calculations for the folded cascode opamp are shown below.

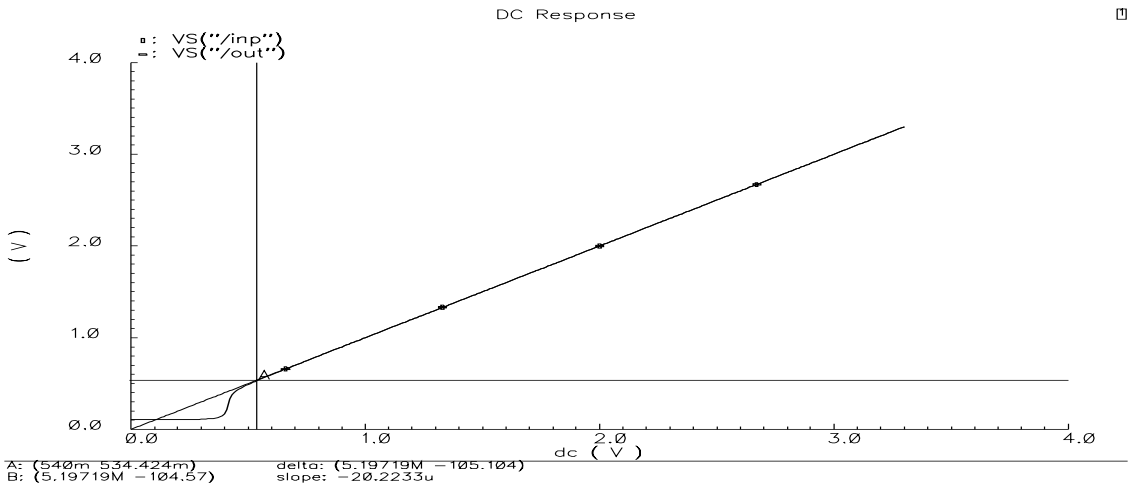
The gain of the opamp $A_V$ is given by,

$$A_V = A_{V1} \cdot A_{V2}$$

where $A_{V1}$ is the first stage gain and $A_{V2}$ is the second stage gain. Also,




(a) Frequency response of the opamp




(b) DC response of the opamp in unity gain configuration

Figure 5.3: Pixel buffer opamp performance

Table 5.1: Equivalent input noise voltages of the transistors

| MOS# | W($\mu m$) | L($\mu m$) | $g_m(\mu S)$ | $E_{ni}(nV_{RMS}/\sqrt{Hz})$ | $E_{1/f}(\mu V_{RMS}/\sqrt{Hz})$ @ 1Hz |
|---|---|---|---|---|---|
| M1,M2 | 0.8 | 0.6 | 38.25 | 16.97 | 2.7 |
| M3,M4 | 4.8 | 1.2 | 58 | 13.8 | 0.77 |
| M5,M6 | 2.4 | 1.2 | 31 | 18.87 | 1.1 |
| M7,M8 | 1.6 | 1.2 | 40.1 | 16.58 | 1.34 |
| M10 | 13 | 1.2 | 343.6 | 0.57 | 0.47 |
| M11 | 16 | 1.2 | 233.5 | 6.86 | 0.42 |

$$\begin{aligned} A_{V1} &= g_{m1} \cdot (r_{o6} \parallel r_{o8}) \\ &\approx g_{m1} \cdot r_{o8} \\ &= \frac{38.25}{0.26} \\ &= 145.4 \end{aligned}$$

since $r_{o8} = r_{ds8} = 3.8M\Omega$ *and* $r_{o6} = (g_{m6} r_{ds6}) \cdot r_{ds3} = 91M\Omega \gg r_{ds8}$

$$\begin{aligned} A_{V2} &= g_{m10} \cdot (r_{o10} \parallel r_{o11}) \\ &= \frac{343.6}{1.8 + 2.1} \\ &= 110.8 \end{aligned}$$

Therefore the total gain $A_V \approx 16300$, which matches closely with the simulated result (see figure 5.3(a))

The flicker noise coefficient $K_F$, for this process is $3.5 \times 10^{-12} V^2 \mu^2$. The noise calculations are shown in Table 5.1 and Table 5.2. $E_{ni}$ is the equivalent input white noise($\frac{8kT}{3g_m} df$) and $E_{1/f}$ is the equivalent input flicker noise($\frac{K_F}{WL} \frac{df}{f}$) at 1Hz.

The equivalent input referred white noise is,

Table 5.2: Contribution of each transistor noise source to the total output noise

| MOS# | $A_{Vnio}$ | $\frac{A_{Vnio}}{A_V}$ | $E_{ni}^2(10^{-18}V^2/Hz)$ | $E_{1/f}(10^{-12}V^2/Hz)$ |
|---|---|---|---|---|
| M1,M2 | $A_V$ | 1 | 288 | 7.3 |
| M3,M4 | $\frac{g_{m3}}{g_{m1}}A_V$ | 1.5 | 190 | 0.6 |
| M5,M6 | $\frac{g_{m5}}{g_{m1}}A_V$ | 0.8 | 356 | 1.2 |
| M7,M8 | $\frac{g_{m7}}{g_{m1}}A_V$ | 1.04 | 275 | 1.8 |
| M10 | $A_{V2}$ | $6.9 \times 10^{-3}$ | 32 | 0.22 |
| M11 | $\frac{g_{m11}}{g_{m10}}A_{V2}$ | $4.7 \times 10^{-3}$ | 47 | 0.18 |

$$\begin{aligned} E_n^{white} &\approx \sqrt{2(288 + (1.5)^2 \cdot 190 + (0.8)^2 \cdot 356 + (1.04)^2 \cdot 275)} \\ &\approx 70nV/\sqrt{Hz} \end{aligned}$$

The equivalent input referred flicker noise at 1Hz is,

$$\begin{aligned} E_n^{flicker} &\approx \sqrt{2(7.3 + (1.5)^2 \cdot 0.6 + (0.8)^2 \cdot 1.2 + (1.04)^2 \cdot 1.8)} \\ &\approx 6.7\mu V/\sqrt{Hz} \end{aligned}$$

The corner frequency $f_c$ is given by,

$$\begin{aligned} f_c &= \frac{(E_n^{flicker})^2}{(E_n^{white})^2} \\ &= 9.2kHz \end{aligned}$$

The following conclusions can be drawn from these calculations -

- The equivalent input referred noise is dominated by the devices in the input stage.
- A well designed low noise amplifier requires the noise to be dominated by the input

Table 5.3: Performance summary of the folded cascode opamp

| | |
|---|---|
| Open loop gain | 80dB |
| Load capacitance | 1pF |
| Input CMR | 0.9V - 2.9V |
| Output swing | 0.3V - 3.0V |
| Unity gain bandwidth | 5.2 MHz |
| Phase Margin | 75 deg |
| Start up time | $<$ 200 ns |
| Slew rate | $10V/\mu s$ |
| Settling time (0.1%) | $<$ 250 ns |
| Power down current | $10\,\mu A$ |
| Power consumption | 0.33 mW |
| Input referred white noise | $70nV/\sqrt{Hz}$ |
| Input referred flicker noise | $6.7\mu V/\sqrt{Hz}$ |

devices. The current design can be modified to achieve this by increasing the $g_m$ of the input devices - M1, M2.

- Flicker noise is dominated by the input devices.
- The transistors in the second stage have hardly any effect on the noise.

The performance summary of the folded cascode opamp is given in Table 5.3 .

The capacitance at the sense can be calculated as follows,

$$C_{sense}^{predicted} = C_{in\_buf} + C_{PD} + C_{misc}$$

where $C_{in\_buf}$ is the input capacitance of the input opamp buffer, $C_{PD}$ is the junction capacitance of the photodiode and $C_{misc}$ is the sum of source capacitance of the reset switch and the interconnect capacitance. Also,

$$\begin{aligned} C_{in\_buf} &= W \cdot L \cdot C_{ox} \\ &= 0.8\mu m \cdot 0.6\mu m \cdot 4.6fF/\mu m^2 \end{aligned}$$

$$= \quad 2.16fF$$

and from process data using unit junction capacitance $C_j$ of $60aF/\mu m^2$, the capacitance of a $14\mu m \times 14\mu m$ photodiode is,

$$\begin{aligned} C_{PD} &= A_{PD} \cdot C_j \\ &= 14\mu m \times 14\mu m \times 60aF/\mu m^2 \\ &= 11.76fF \end{aligned}$$

From layout, the parasitic inter connect capacitance is approximately $2fF$ and assuming $1fF$ source capacitance of the reset switch the total capacitance of the sense node is

$$C_{sense}^{predicted} \approx 17fF$$

Using the predicted sense node capacitance, the conversion gain can be calculated from simulation by plotting the output voltage for a given integration time as shown in figure 5.4 . The conversion gain is calculated as follows,

$$Predicted\ Conversion\ Gain = \frac{\Delta V}{\Delta Q}$$

and

$$\begin{aligned} \Delta Q &= Iphotodiode \cdot \Delta T \\ &= 6250e^- \end{aligned}$$

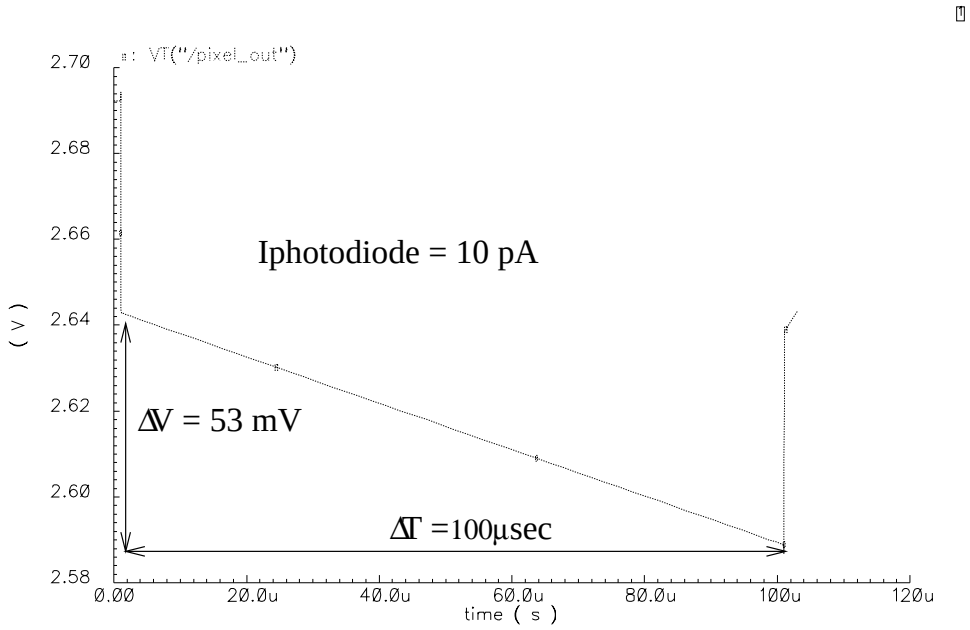



Figure 5.4: Conversion gain prediction

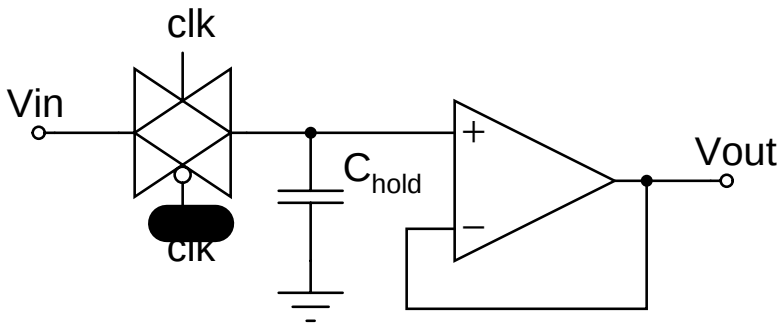



Figure 5.5: Sample and hold amplifier

Using $\Delta V = 53\,mV$,

$$Predicted\ Conversion\ Gain = 8.5\mu V/e^{-}$$

### Sample and hold amplifier

The schematic of the sample and hold amplifier used in the prototype is shown in figure 5.5 . The minimum value of the hold capacitor $C_{hold}$ is determined by the $kT/C$ noise limitation. A 1pF hold capacitance is chosen which gives rise to a noise of $64\mu V/\sqrt{Hz}$. The transmission gates are sized (W/L = 3) for the required sample mode bandwidth of 40 MHz. The two stage folded cascode opamp described earlier and shown in figure 5.2 on page 36 is reused to shorten design time. CDS scheme is implemented using the sample and hold amplifiers as shown in figure 5.6 . The signals *shs* and *shr* are clocks to sample the signal and reset level respectively. The transmission gates at the output of the sample and hold amplifier serve as an analog multiplexer. These transmission gates are enabled by the *colsel* signal which is generated by the pixel level column decoder.

### Column decoder

The column decoder is used to generate the control signals like the sampling clocks, power down for the two modes of operation. The seven bit address bus is decoded into a column

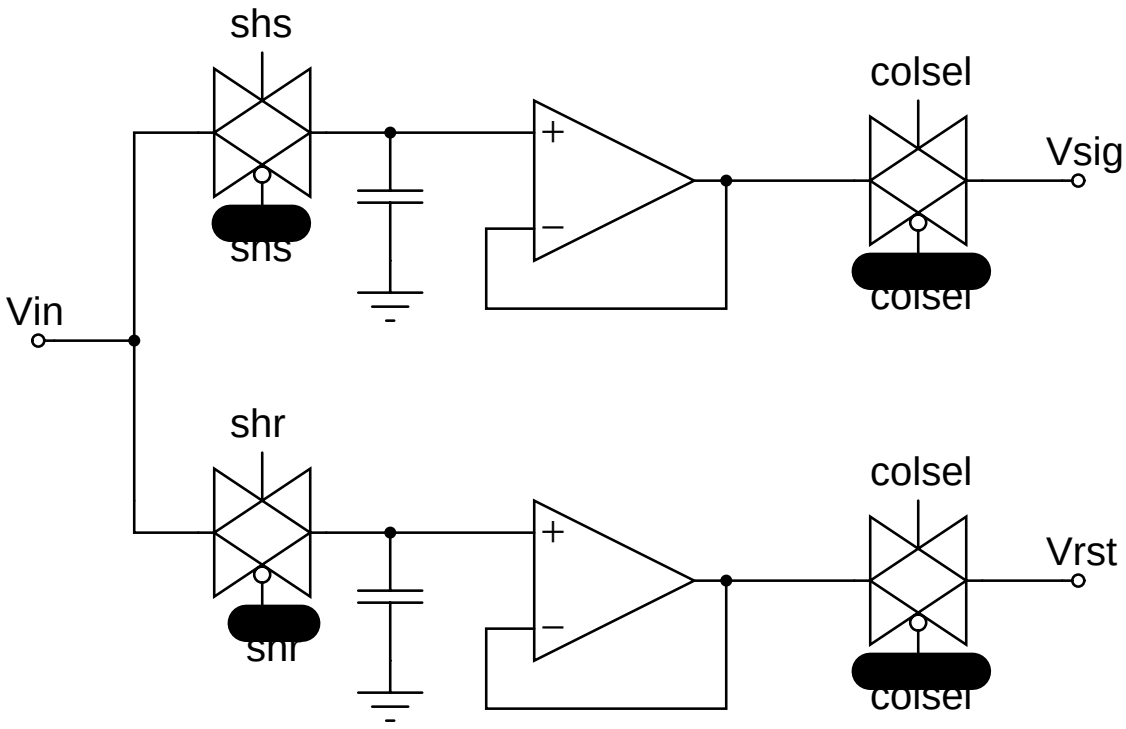



Figure 5.6: CDS implementation schematic

select (*colsel*) using a seven input AND gate. The control signals for a particular column are generated by "ANDing" the *colsel* signal with appropriate clocks depending on the mode of operation. The schematic of the column decoder is shown in figure 5.7 . The seven input NAND gate is designed using a current source and a tree of seven NMOS transistors for optimum layout design. The bias current is $20\mu A$ and the NMOS transistors are sized for low ON resistance of $1\,K\Omega$. Therefore when all the series resistors are ON, the output voltage is about 0.14 mV, which is small enough to be logic zero. The column level control signals for two modes of operation are generated by using a 2:1 multiplexer. The "select" signal to the multiplexer, I(imager)/S(spectrometer), determines the mode of operation. "Global signals" are used in case of "IMAGER" mode and "local" signals are used in SPECTROMETER mode to enable non-destructive readout.

### Output buffer

An output buffer is required to drive large off-chip capacitive loads, for example the input capacitance of a 12 bit analog to digital converter. A simple $g_m - C$ OTA as shown in figure 5.8 in unity gain configuration is used as an output buffer. The output stage is cascoded to increase gain. The bias current in the output stage is chosen from the slew rate requirement of $10V/\mu Sec$. The transistors M5, M6, M7 are sized for the required output swing of 2.5 V. Since there is only one high impedance node at the output, the dominant pole is determined by the load capacitance. Therefore the load capacitance also serves as the compensation capacitance. The non-dominant pole at the gate of M4 determines the phase margin. So the current mirror ratio from M4 to M5, B, is chosen to be three to achieve a phase margin of at least 65° (see figure 5.9(a)) even with low capacitive loads. The input transistors M1, M2 are chosen for large $g_m$ of 1 mA/V and wide input common mode range (see figure 5.9(b)).

The equivalent input referred noise of a symmetrical $g_m - C$ OTA shown in figure 5.8 can be calculated using a similar procedure as the one employed in evaluating the noise performance of the folded cascode opamp.

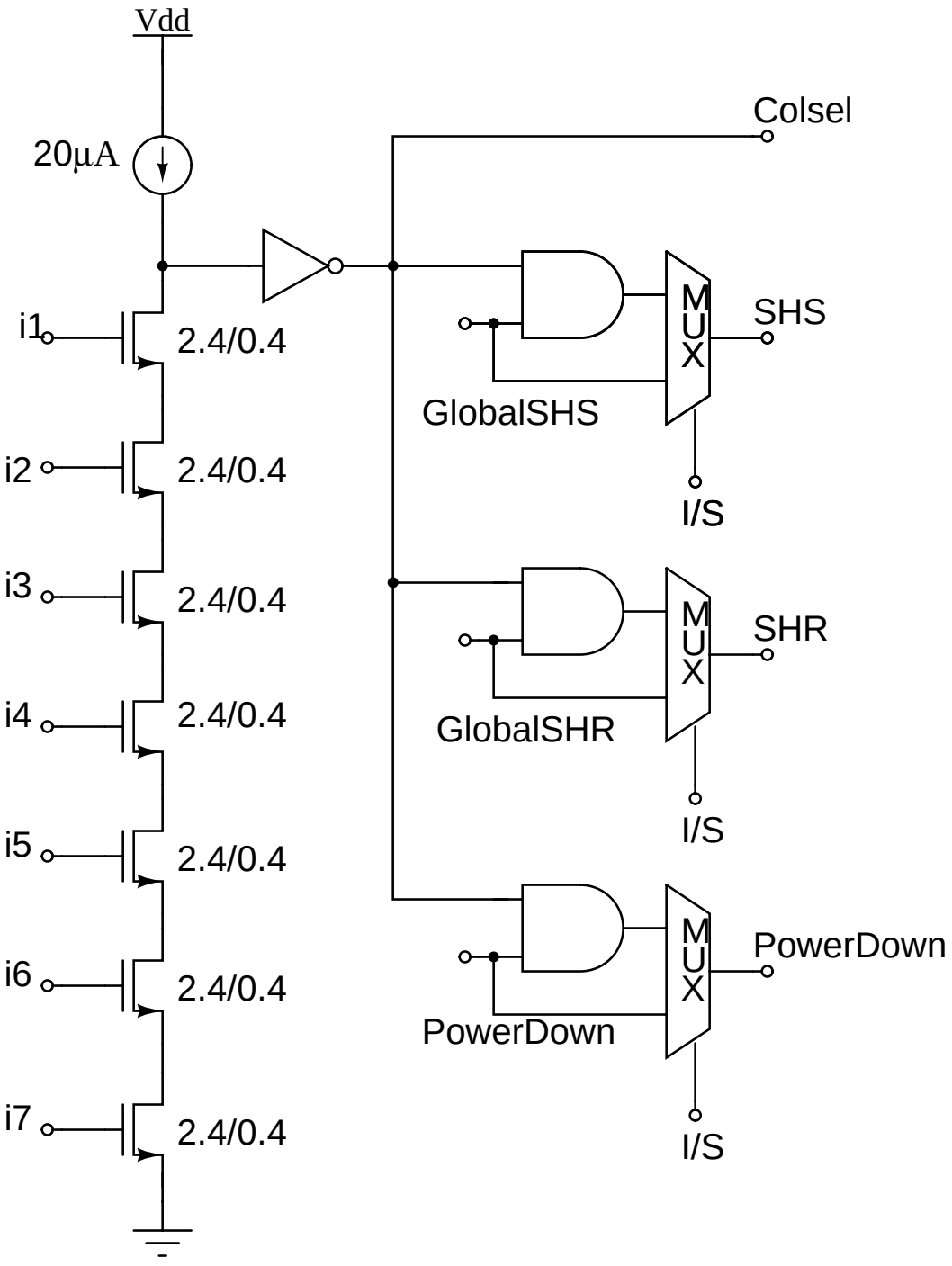



Figure 5.7: Column decoder schematic

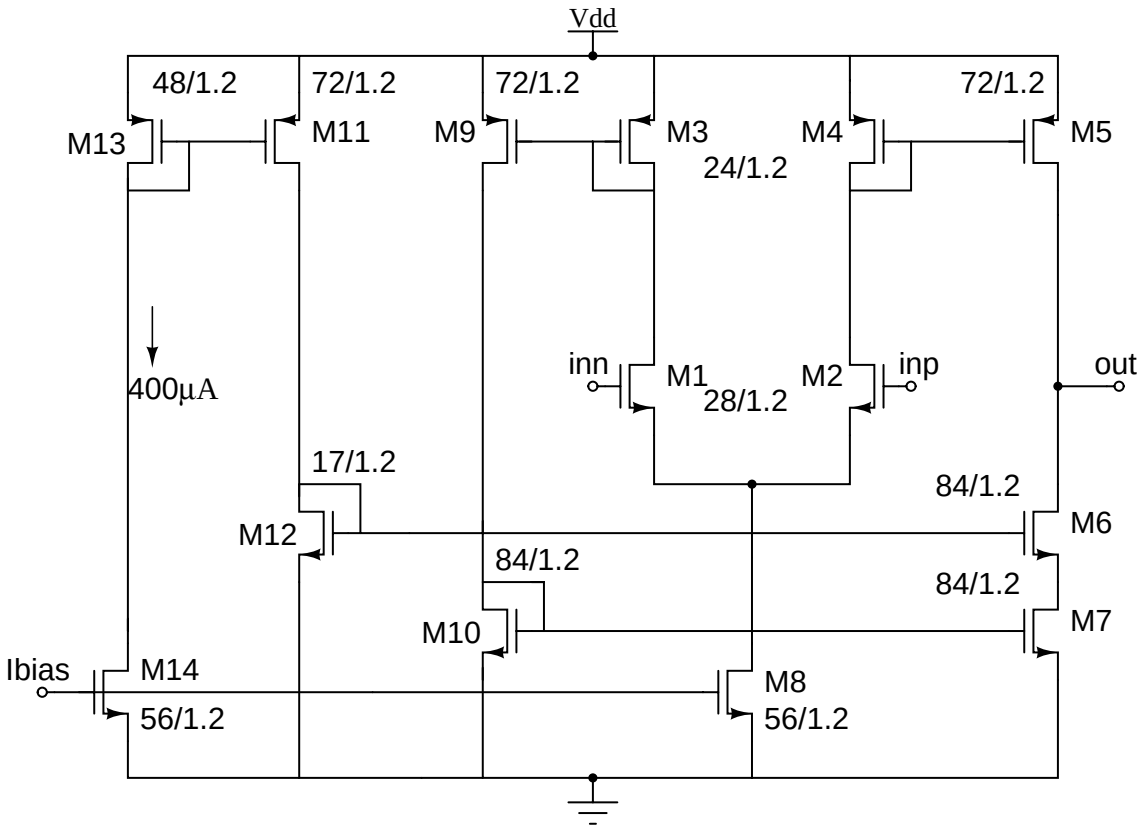
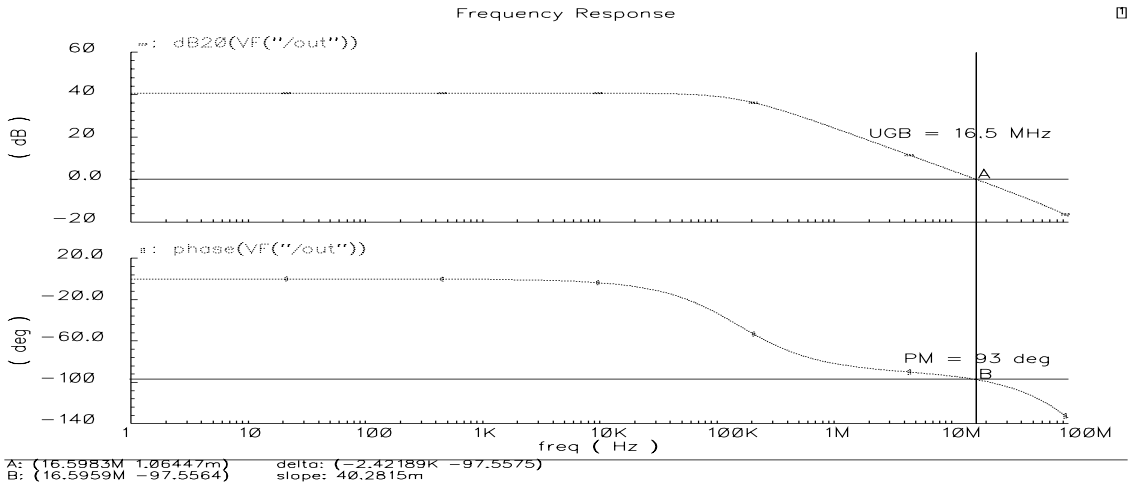
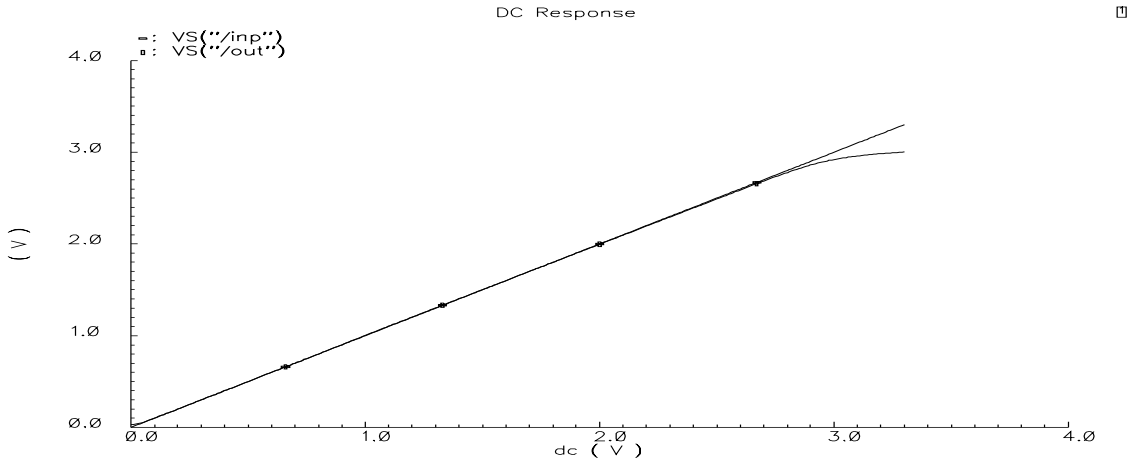



Figure 5.8: Output buffer schematic (all sizes in $\mu m$)




(a) Frequency response with 30 pF load




(b) DC response of the output buffer

Figure 5.9: Output buffer performance

Table 5.4: Equivalent input noise voltages of the transistors

| MOS# | W($\mu m$) | L($\mu m$) | $g_m(\mu S)$ | $E_{ni}(nV_{RMS}/\sqrt{Hz}$ | $E_{1/f}(\mu V_{RMS}/\sqrt{Hz})$ @ 1Hz |
|---|---|---|---|---|---|
| M1,M2 | 28 | 1.2 | 1092 | 3.16 | 0.32 |
| M3,M4 | 24 | 1.2 | 574 | 4.36 | 0.34 |
| M5,M9 | 72 | 1.2 | 1776 | 2.49 | 0.20 |
| M6 | 84 | 1.2 | 3332 | 1.82 | 0.19 |
| M7,M10 | 84 | 1.2 | 3192 | 1.84 | 0.19 |

The gain of the opamp $A_V$ is given by,

$$A_V = A_{V1} \cdot A_{V2}$$

where $A_{V1}$ is the first stage gain and $A_{V2}$ is the second stage gain.

Also,

$$\begin{aligned}
A_{V1} &= \frac{g_{m1}}{g_{m3}} \\
&= \frac{1092\mu}{574\mu} \\
&= 1.9 \\
A_{V2} &= g_{m5} \cdot (r_{o5} \parallel r_{o6}) \\
&= 1776\mu \cdot [r_{ds5} \parallel (g_{m6} r_{ds6} \cdot r_{ds7})] \\
&\approx 1776\mu \cdot r_{ds5}, \quad g_{m6} r_{ds6} \cdot r_{ds7} \gg r_{ds5} \\
&= 1776\mu \cdot 34.5k\Omega \\
&= 61.9
\end{aligned}$$

Therefore total gain $A_V \approx 117$ which matches very closely with the simulated open loop gain.

The noise calculations are shown in Table 5.4 and Table 5.5.

Table 5.5: Contribution of each transistor noise source to the total output noise

| MOS# | $A_{Vnio}$ | $\frac{A_{Vnio}}{A_V}$ | $E_{ni}^2(10^{-18}V^2/Hz)$ | $E_{1/f}(10^{-12}V^2/Hz)$ |
|---|---|---|---|---|
| M1,M2 | $A_V$ | 1 | 10 | 0.1 |
| M3,M4 | $\frac{g_{m3}}{g_{m1}}A_V$ | 0.5 | 19 | 0.12 |
| M5,M9 | $\frac{g_{m3}}{g_{m1}}A_V$ | 0.5 | 6.2 | 0.04 |
| M6 | $\frac{g_{m6}}{g_{m1}}\frac{A_V}{B}$ | 1 | 3.3 | 0.03 |
| M7,M10 | $\frac{g_{m7}}{g_{m1}}\frac{A_V}{B}$ | 0.97 | 3.4 | 0.03 |

The equivalent input referred white noise is,

$$\begin{aligned} E_n^{white} &\approx \sqrt{2(10 + (0.5)^2 \cdot 19 + (0.5)^2 \cdot 6.2 + 3.4) + 3.3} \\ &\approx 6.5nV/\sqrt{Hz} \end{aligned}$$

The equivalent input referred flicker noise at 1Hz is,

$$\begin{aligned} E_n^{flicker} &\approx \sqrt{2(0.1 + (0.5)^2 \cdot 1.2 + (0.5)^2 \cdot 0.04 + (0.97)^2 \cdot 0.03) + 0.03} \\ &\approx 0.6\mu V/\sqrt{Hz} \end{aligned}$$

The corner frequency $f_c$ is given by,

$$\begin{aligned} f_c &= \frac{(E_n^{flicker})^2}{(E_n^{white})^2} \\ &= 8.5kHz \end{aligned}$$

The following conclusions can be drawn from these calculations -

- Since the gain of the first stage is only 1.9, the noise contribution from the second stage transistors is not negligible

Table 5.6: Performance summary of $g_m - C$ OTA

| | |
|---|---|
| Open loop gain | 41dB |
| Load capacitance | 30pF |
| Input CMR | 0.9V - 2.9V |
| Output swing | 0.5V - 2.8V |
| Unity gain bandwidth | 16 MHz |
| Phase Margin | 80 deg |
| Slew rate | $10V/\mu s$ |
| Settling time (0.1%) | $<$ 250 ns |
| Power consumption | 10 mW |
| Input referred white noise | $6.5nV/\sqrt{Hz}$ |
| Input referred flicker noise | $0.6\mu V/\sqrt{Hz}$ |

- The noise contributions from all the transistors (except the input transistors) are scaled by $g_{m1}$. So the overall noise can be reduced by increasing $g_{m1}$, which also ensures that the overall noise is dominated by the input devices
- The noise contribution from the second stage transistors can further be reduced by increasing B

The performance summary of the folded cascode opamp is given in Table 5.6 .

## 5.2 Layout Design

The layout design is determined by the size of the photodiode. Since the photodiodes used in the prototype are $14\mu m \times 14\mu m$, the pixel buffer, CDS implementation circuitry and column decoders have to be layed out in less than $14\mu m$ width. This results in a "skinny" layout for each pixel. The pixel buffer is placed as close as possible to the photodiode to reduce the parasitic capacitance on the "sense node". The sample and hold circuit for signal is placed close to pixel buffer and address lines run through the middle of each column. Digital logic and sample and hold circuit for reset level are placed below the address lines. Since opamps with large capacitive driving capability are used, the routing length of the signals is not critical. The photodiodes are not silicided to increase sensitivity. This is done

using the silcide blocking mask layer. Metal 4 is used as light shield to prevent unnecessary photo charge integration. Two photo diodes at either end of the array are also light shielded to get a measure of dark current, which can be later used for dark reference. Guard ring separation is used to decouple substrate noise. Multiple bond pads are used for supplies to reduce bond wire inductance. A separate $V_{dd-reset}$ is used to reduce the noise coupling to the sensitive photo charge integration node. Inverter based buffers are used to buffer the input clocks .

## 5.3 Experimental Results

A $128 \times 1$ pixel CMOS image sensor prototype is fabricated in $0.4\mu m$, four metal, single poly standard CMOS process. The chip micro photograph of the prototype is shown in figure 5.11 . The total die size is $5mm^2$ and the prototypes are packaged in a 84 pin LCC package. The measured results from the prototype are presented below.

### Conversion Gain

Conversion gain is the measure of the pixel buffer and output circuit's ability to convert photo charge to voltage. This parameter is found by measuring the change in output voltage, $\Delta V$ [Volts], caused by a change in signal charge, $\Delta Q$ [electrons]. But $\Delta Q$ is related to the change in current by the equation,

$$\Delta Q = \Delta I \frac{T_{int}}{q} \ [electrons]$$

where $\Delta I$, is the change in input current during the integration period, $T_{int}$ and $q$ is the electron charge. Output referred conversion gain or electron sensitivity is given by,

$$S_e = \frac{\Delta V}{\Delta Q} \ [Volts/electron]$$

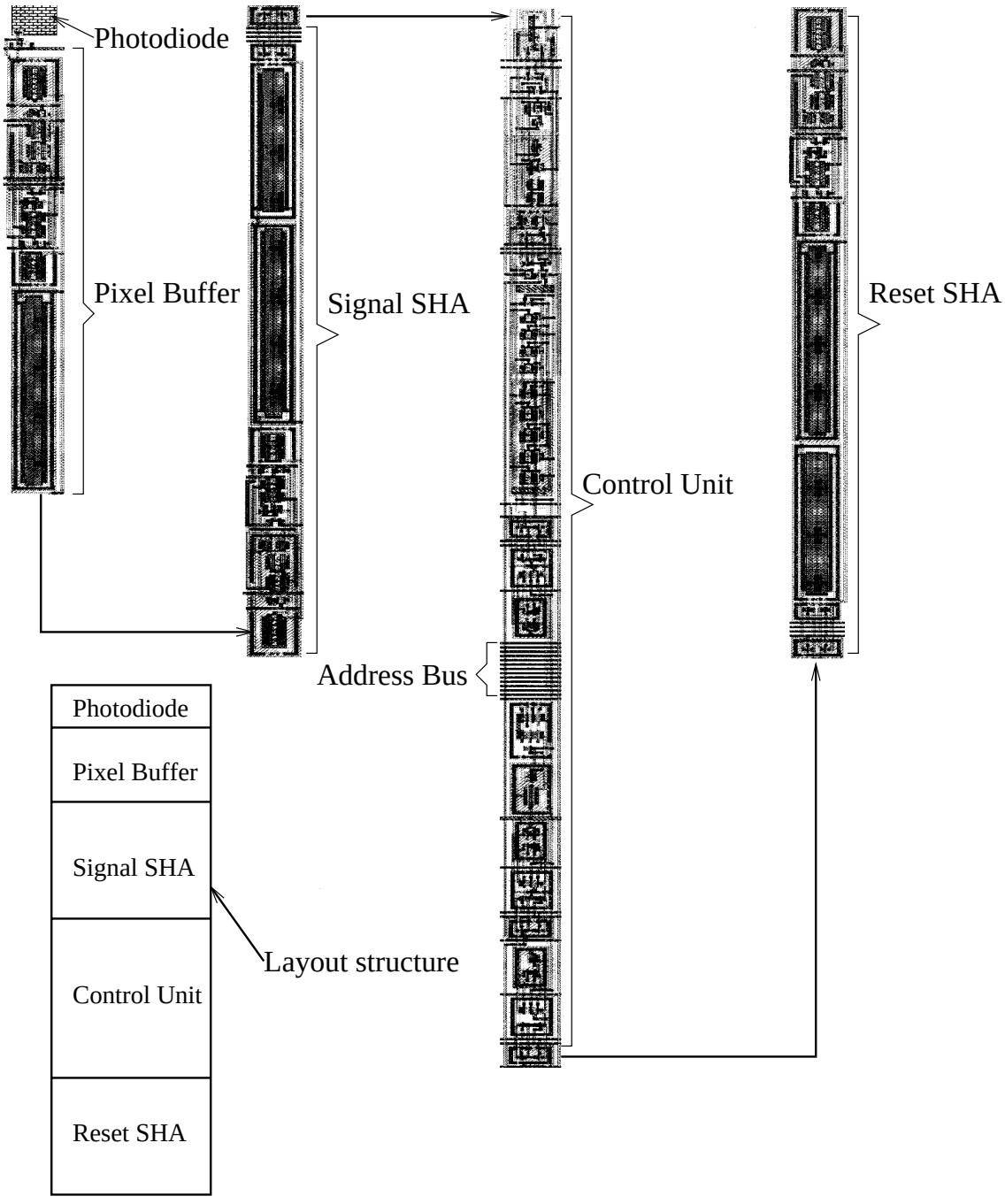



Figure 5.10: Single column layout

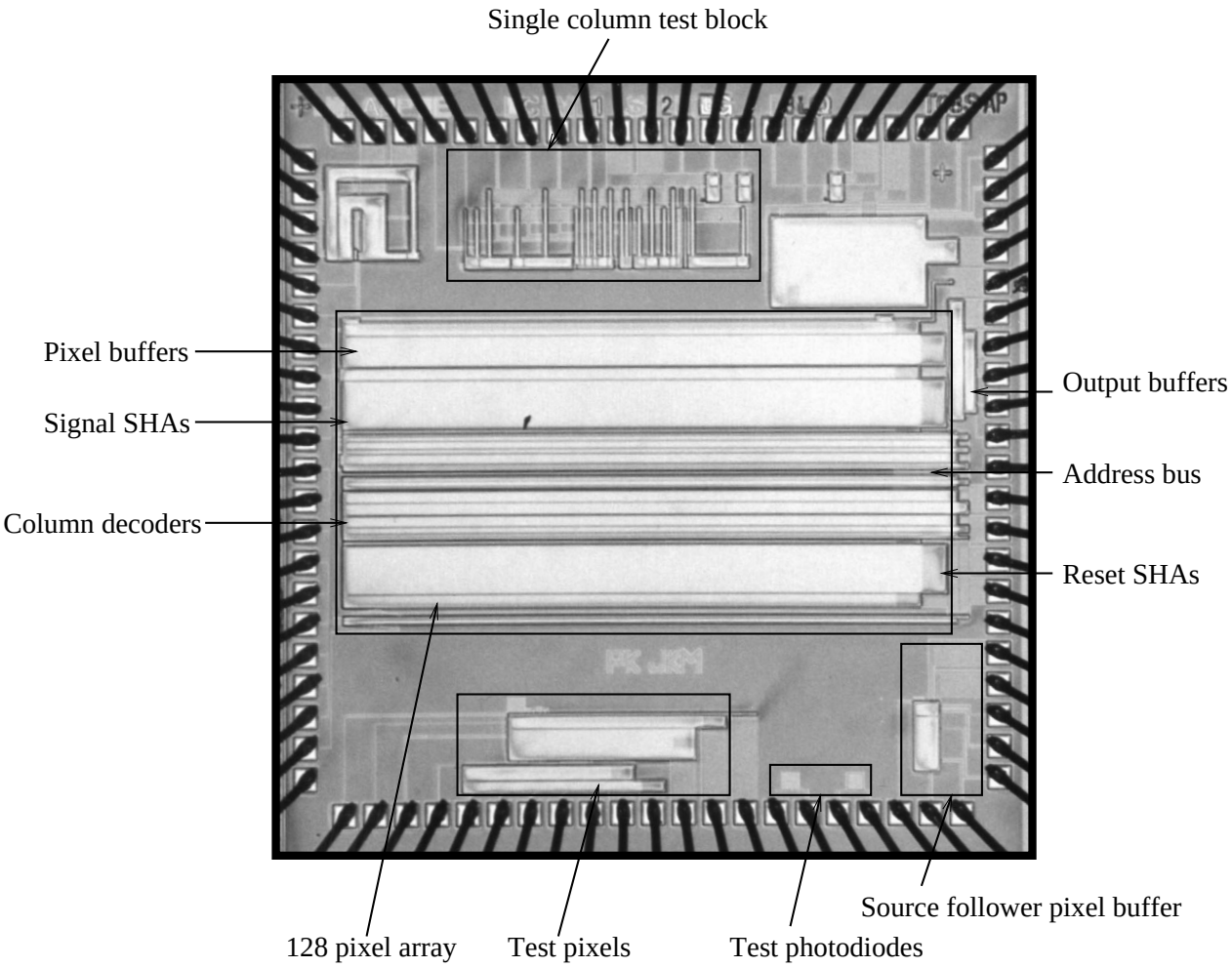



Figure 5.11: Image sensor micro photograph

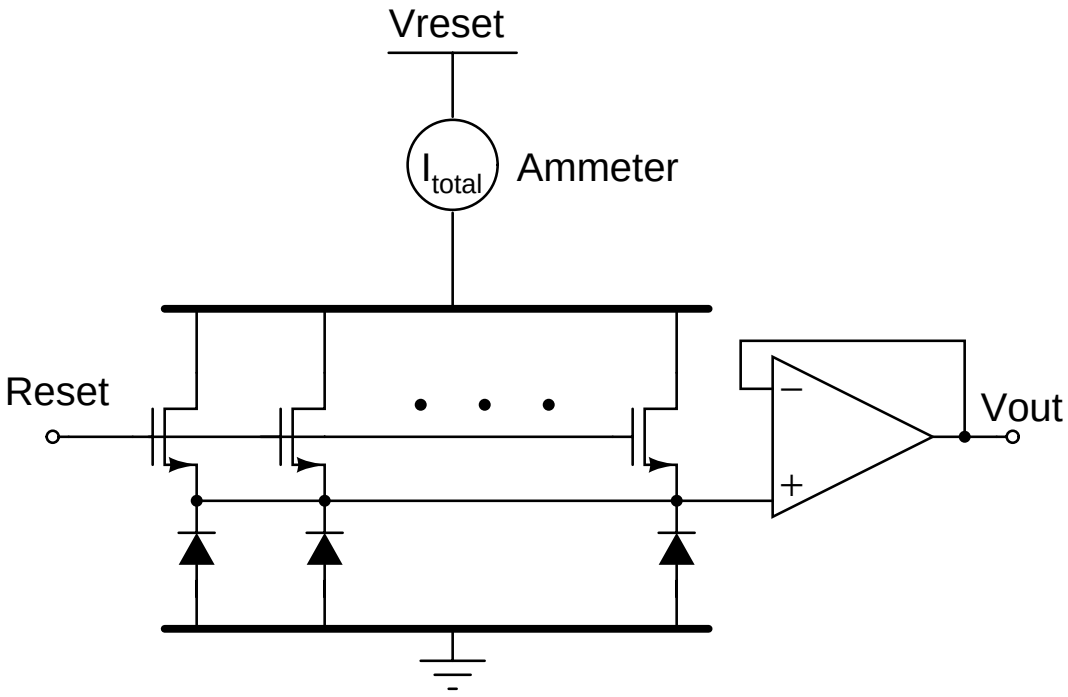



Figure 5.12: Conversion gain test setup

The test set up used for measuring conversion gain is shown in figure 5.12 . The current per pixel is equal to the total current $I_{total}$ divided by the number of pixels. Figure 5.13 shows the measured conversion gain plot. The conversion gain is equal $6.5\mu V/e^-$ which matches relatively closely with the predicted conversion gain of $8.5\mu V/e^-$. The capacitance of the sense node can be calculated using the output referred conversion gain as follows,

$$C_{sense\_node}^{measured} = \frac{q \cdot A_{analog\_path}}{S_e}$$

where, $q$ is the charge of electron, $A_{analog\_path}$ is the total gain of the analog signal path (see figure 5.14 ). The measured DC response and magnitude response of the analog signal path is shown in figure 5.15. Due to the use of high gain opamps, the analog signal path gain is unity and no gain peaking in the magnitude response indicates good stability. Using $S_e = 6.5\mu V/e^-$,

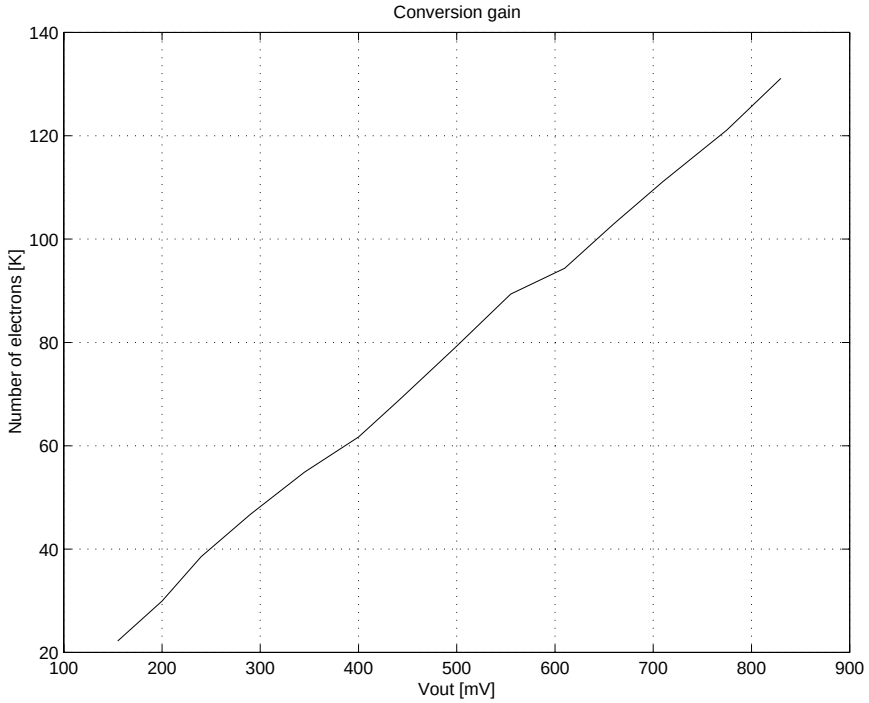



Figure 5.13: Measured conversion gain plot

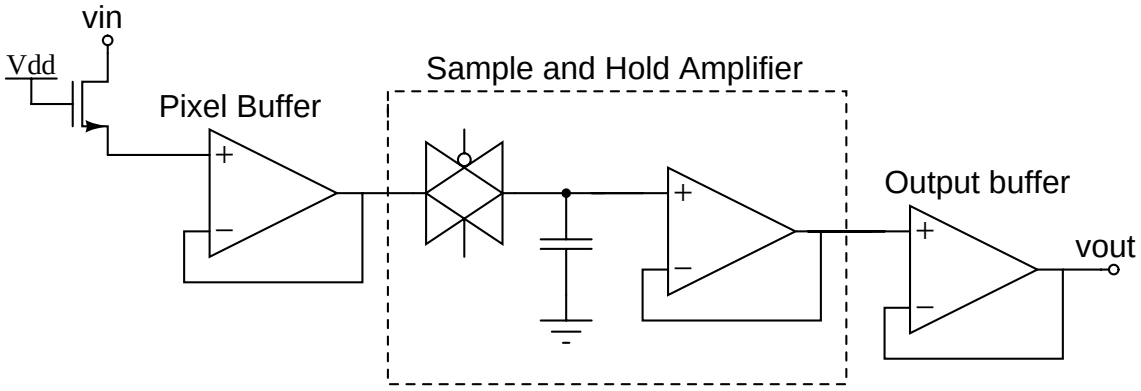
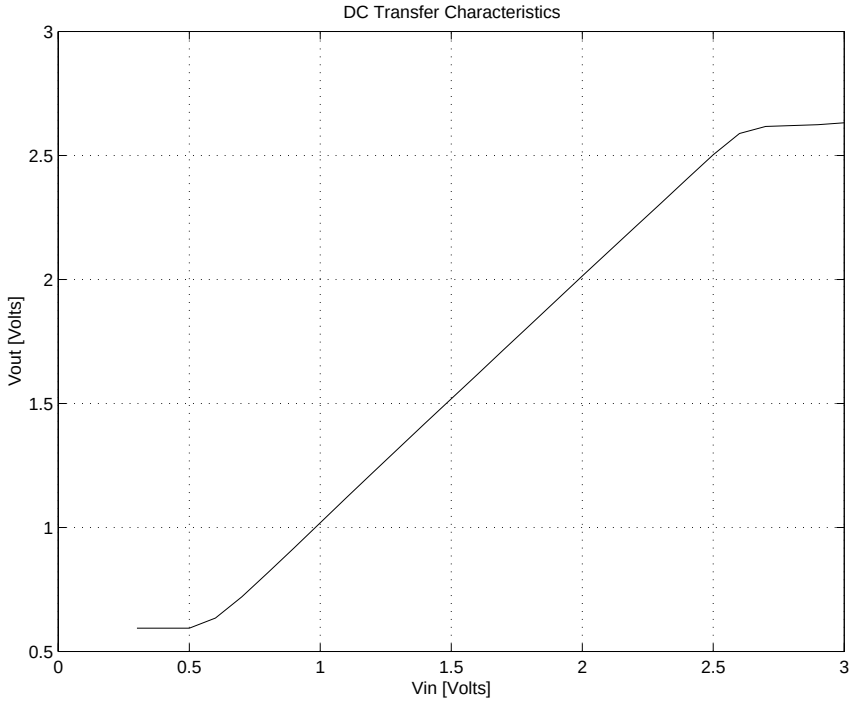
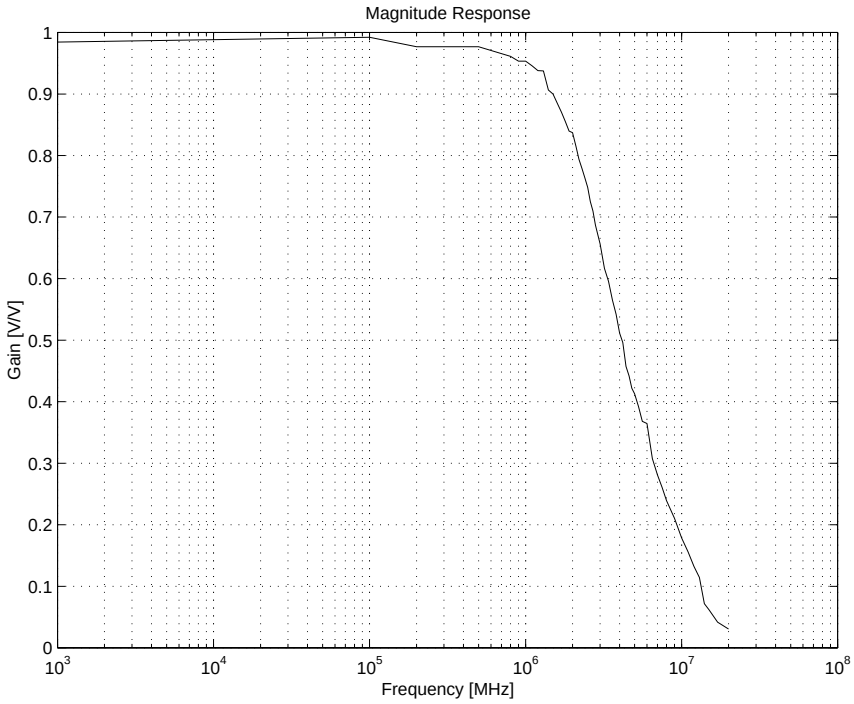



Figure 5.14: Analog signal path




(a) DC Response




(b) Magnitude Response

Figure 5.15: Measured analog signal path performance

$$C_{sense\_node}^{measured} = 24fF$$

which matches closely with the predicted value of $17fF$.

**Fixed Pattern Noise**

FPN is calculated for both the dark and illuminated conditions. Dark FPN is dominated by the offset mismatches in the signal path and FPN in illuminated condition is dominated by the shot noise of the photodiodes. With no illumination, 30 frames of 20 random pixels in the array are captured and FPN in dark is calculated as follows.

$$FPN_{frame} = \sigma_{frame} = \sqrt{\frac{\sum_{i=1}^{20}(Pixel_i - \overline{Pixel})^2}{20-1}}$$

where $FPN_{frame}$ is the FPN for a particular frame, $Pixel_i$ is output of $pixel\ i$ and $\overline{Pixel}$ is the mean output of the frame. The overall FPN is equal to the mean FPN of all the frames and is given by

$$FPN = \frac{\sum_{frame=1}^{30}\sigma_{frame}}{30}$$

Figure 5.16 shows the measured dark FPN for different frames. The mean dark FPN is 19 mV. The offset mismatch in the signal path is the major source of dark FPN. The DC transfer characteristic of analog signal path for 10 random pixels is shown in figure 5.17 and the standard deviation of the offset $\sigma_{offset}$, is calculated to be 22 mV. The offset mismatch contribution of output buffer can be neglected since it is common to all pixels. For simplicity, assuming no threshold voltage mismatch of reset NMOS transistor, the offset mismatch is contributed by pixel buffer and sample and hold amplifier offsets. Since the same opamp is used, the offset mismatch contribution of each closed loop opamp can be approximated to

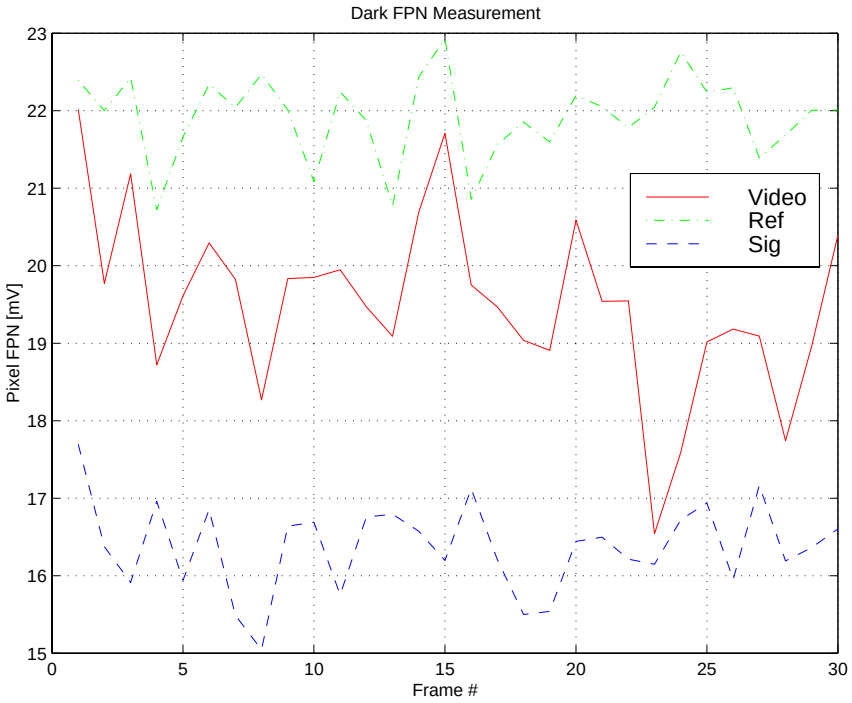



Figure 5.16: Measured Dark FPN - Sig is the signal output , Ref is the reference output and Video is the difference of Sig and Ref signals.

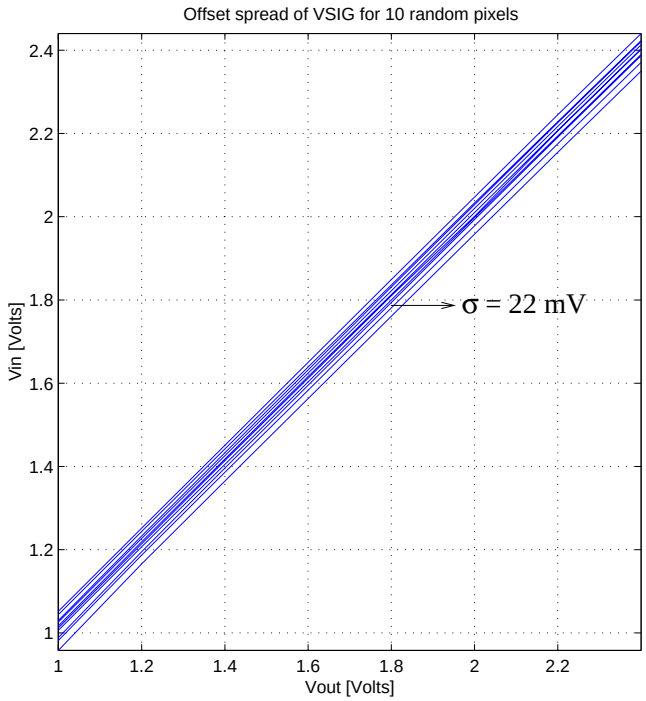



Figure 5.17: DC transfer characteristics of 10 random pixels

$\frac{\sigma_{offset}}{\sqrt{2}}$, which is equal to 16 mV. Note that FPN on the signal output is very close to 16 mV. The higher FPN on reference output can be attributed to larger offset mismatch spread in the reference signal path and due to coupling of the digital noise onto the reference output. Assuming equal offset mismatch variation for both reference and signal outputs FPN of the video output is equal to $\sqrt{2}$ times the individual mismatch. Therefore FPN due to offset mismatch is given by,

$$\begin{aligned} FPN_{offset} &= \sqrt{2} \cdot (\frac{\sigma_{offset}}{\sqrt{2}}) \\ &= \sigma_{offset} \\ &\approx 22\ mV \end{aligned}$$

The FPN due to offset matches match very closely with the measured FPN of the video output thus reinforcing that the major source of FPN is offset mismatch in sample and hold

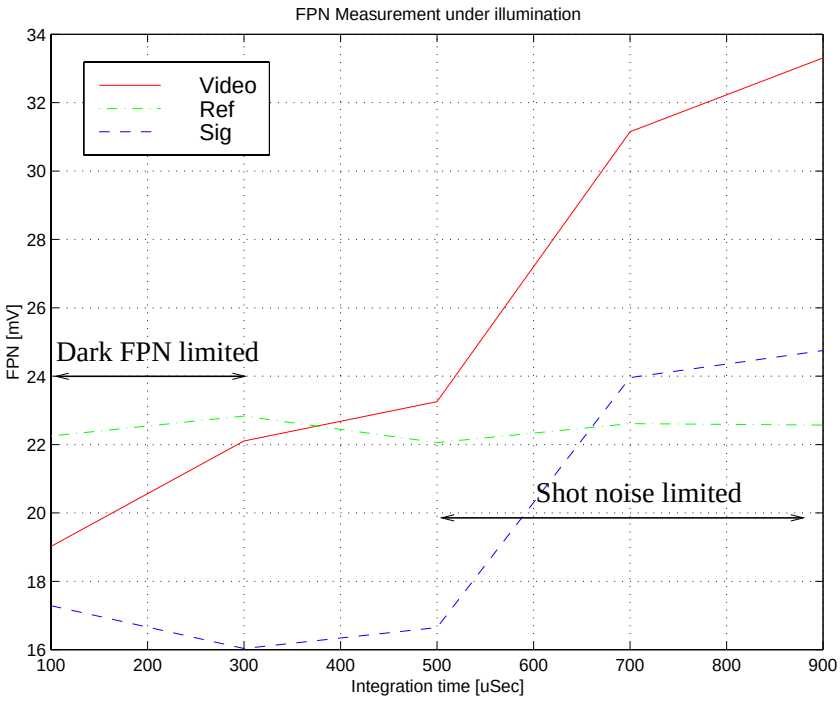



Figure 5.18: Measured FPN under illumination

amplifiers. FPN is also measured under illumination and the measured results are shown in figure 5.18 .For low integration times (equivalently low light levels), FPN is limited by the dark FPN and for high light levels) FPN is shot noise limited.

### Read Noise

Read noise is variation of the pixel output with different readouts. Read noise of a pixel is measured by calculating the standard deviation of the pixel output (dark condition) in 30 frames.

Mathematically,

$$read\_noise_{pixel} = \sigma_R = \sqrt{\frac{\Sigma_{frame=1}^{N}(Pixel - \overline{Pixel})^2}{N-1}}$$

where N is the number of frames and $\overline{Pixel}$ is the mean value of the pixel for N frames. The measured read noise for 20 different pixels with N = 30 is shown in figure 5.19 . The rms

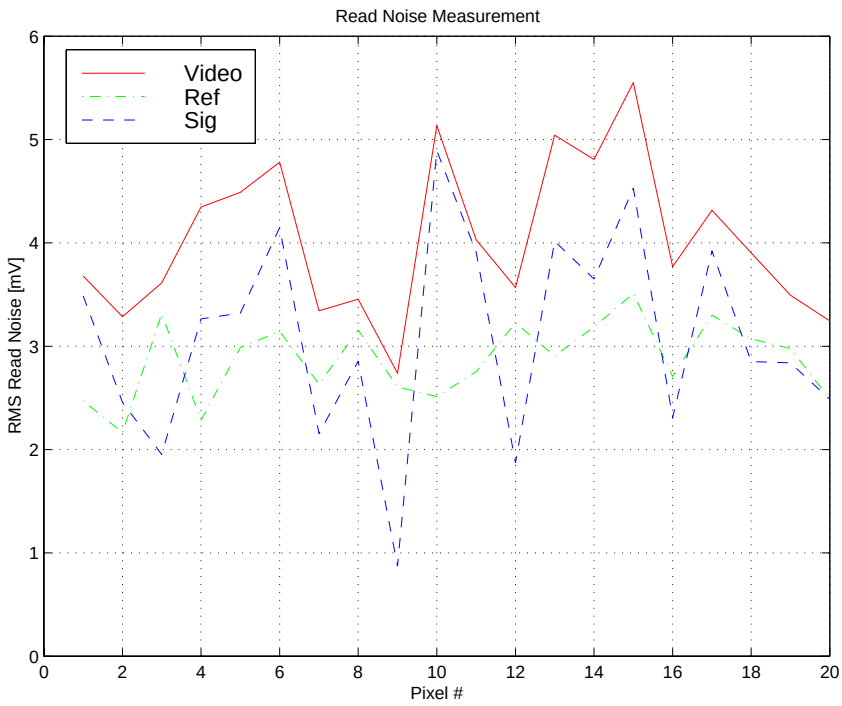



Figure 5.19: Measured read noise - Sig is the signal output , Ref is the reference output and Video is the difference of Sig and Ref signals.

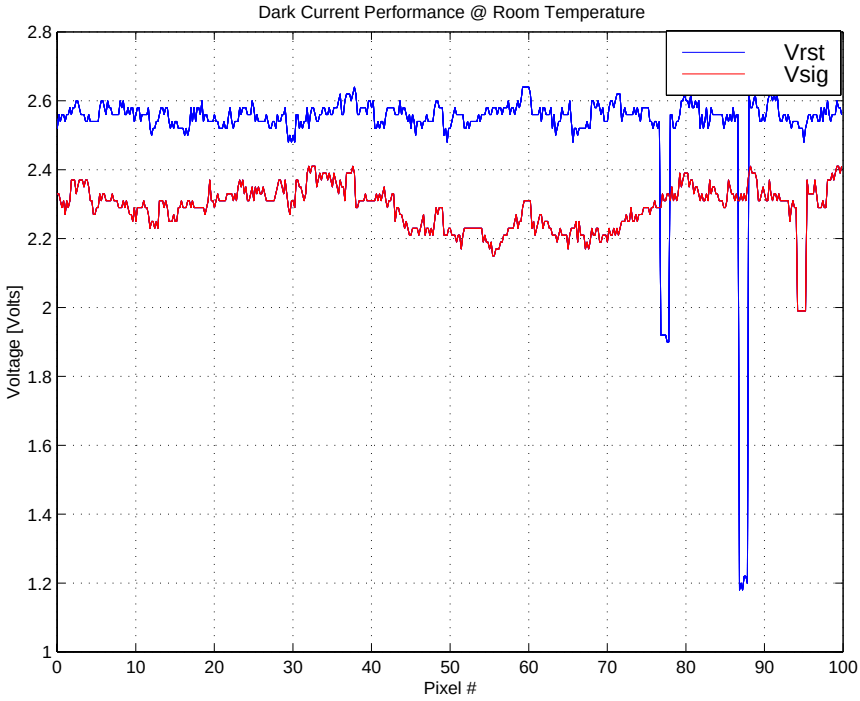



Figure 5.20: Measured dark current performance

read noise of the array is equal to the mean read noise of measured 20 pixels and is equal to 4 mV.

### Dark Current

Dark current is measured by integrating the leakage current over large integration time. Figure 5.20 shows the measured output for 1 second integration time. The mean dark current is 200 mV/sec. The dynamic range will be halved in 5 seconds and hence can be defined as the maximum shutter exposure time. This value of dark current is very high and is mainly due to high leakage current associated with low $V_{th}$ devices in deep sub micron standard CMOS technology.

### Linearity

The linearity of the sensor is measured with respect to intensity and integration time and is shown in figure 5.21 . The maximum integral non linearity (INL) is less than 5% in both cases.

### Signal to Noise Ratio (SNR)

The output SNR is the ratio of the saturation voltage and the rms noise floor as shown in figure 5.22 . The measured SNR is,

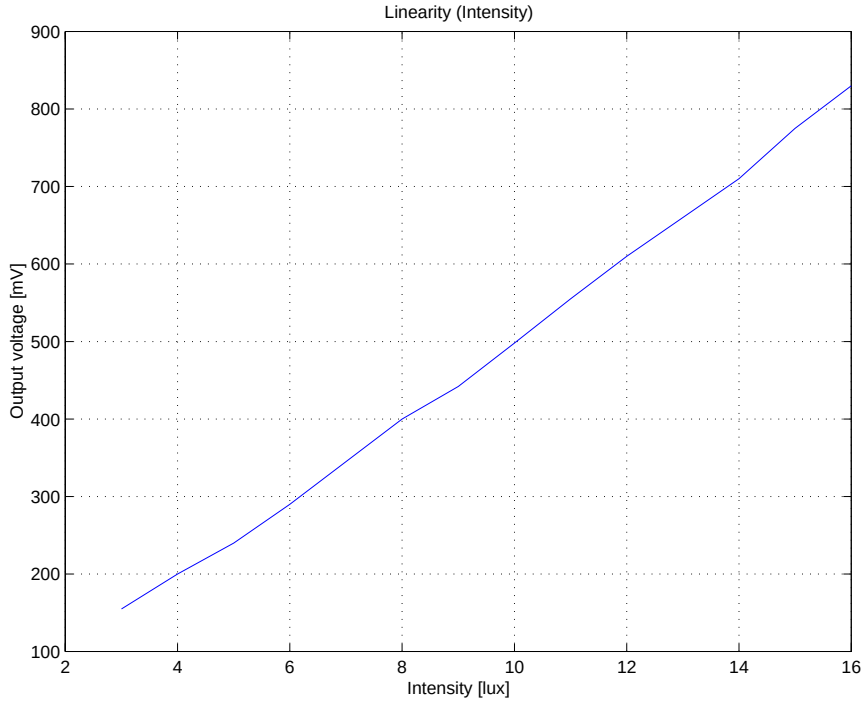
$$\begin{aligned} SNR &= \frac{Saturation\ Volatge}{RMS\ read\ noise\ (\sigma_R)} \\ &= \frac{2000\ mV}{4\ mV} \\ &= 54\ dB \end{aligned}$$

### Readout Timing Verification

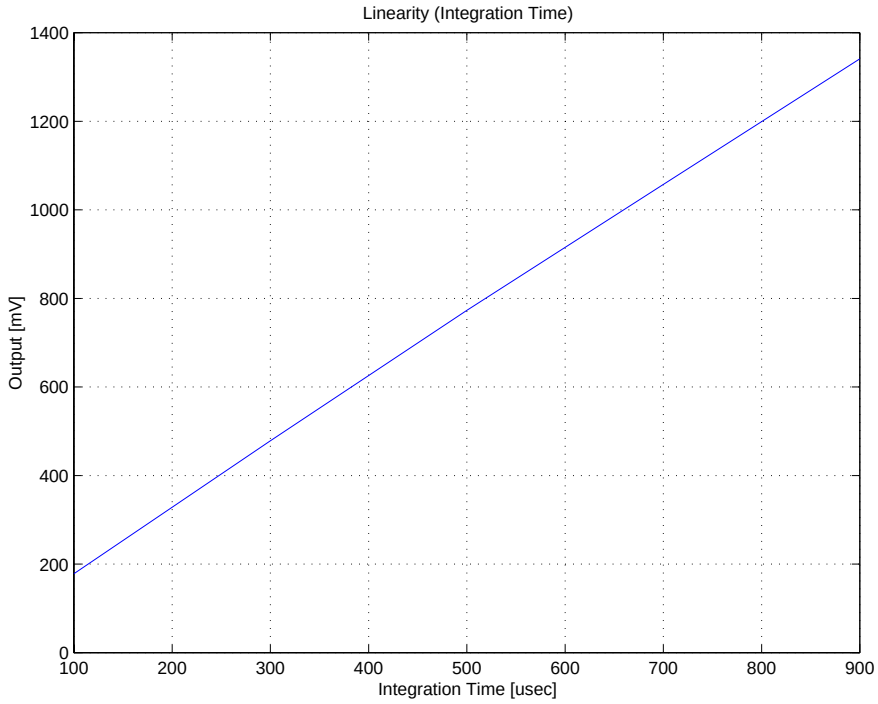
The measured array output in two modes of readout is shown in figure 5.23 . Four pixels on either sides of the array are light shielded by Metal4 to use their output as dark reference. The measured results indicate that they are not completely shielded. The non-destructive readout mode is also found to be fully operational.

### Photodiode Response

The measured response of different Nwell - Psubstrate and Ndiff - Psubstrate photodiodes is shown in figure 5.24. As expected, the PMOS reset switch based pixels show wider saturation voltage. Also, Nwell - Psubstrate photodiode is more sensitive than the Ndiff - Psubstrate photodiode at "white light" wavelengths. A more comprehensive characterization of the photodiodes is required. The "startup time" in the response is due to the output swing limitation of the output buffer. The PMOS reset based pixels are more sensitive due to




(a) Linearity with respect to intensity




(b) Linearity with respect to integration time

Figure 5.21: Linearity measurement

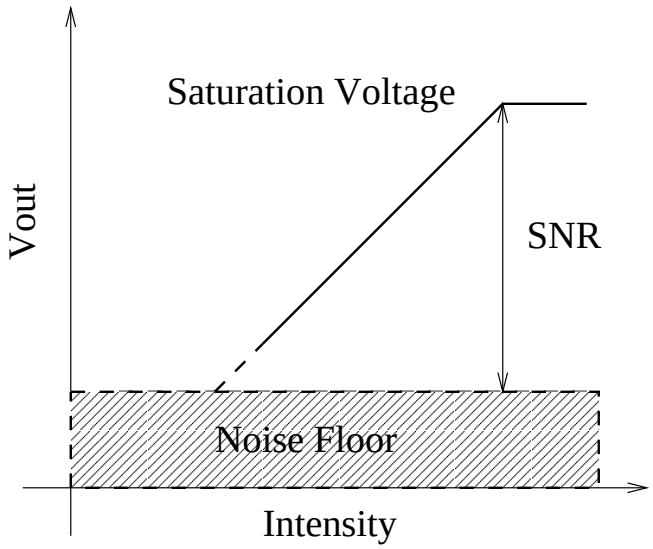
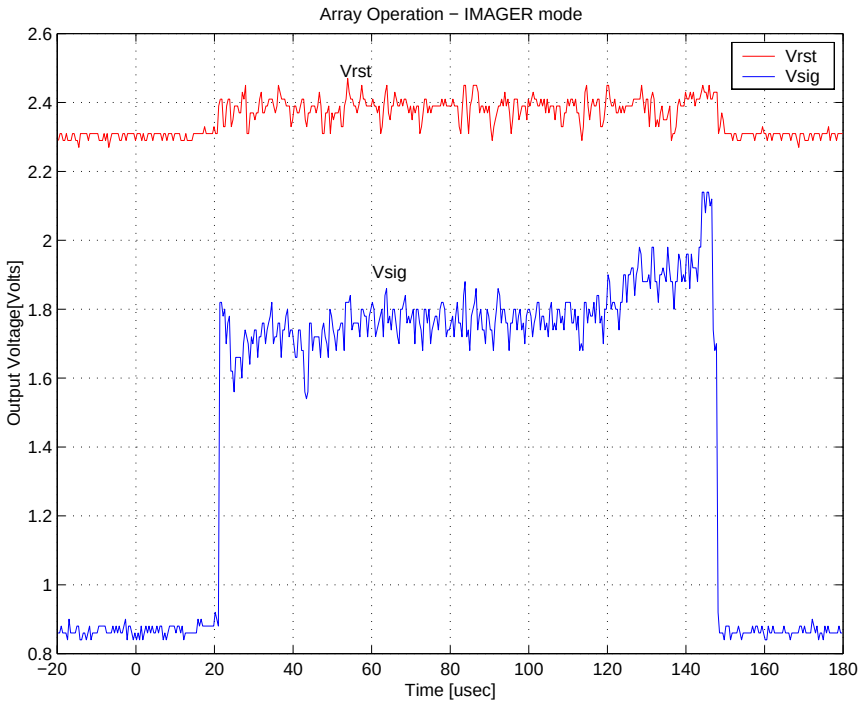
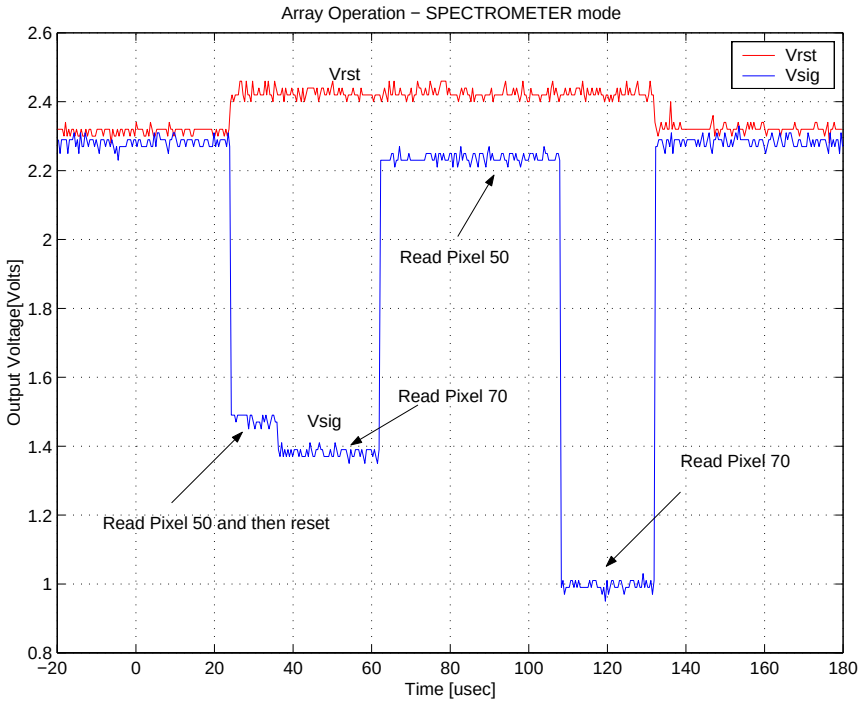



Figure 5.22: Signal to Noise Ratio definition

larger reverse bias across of the photodiode.

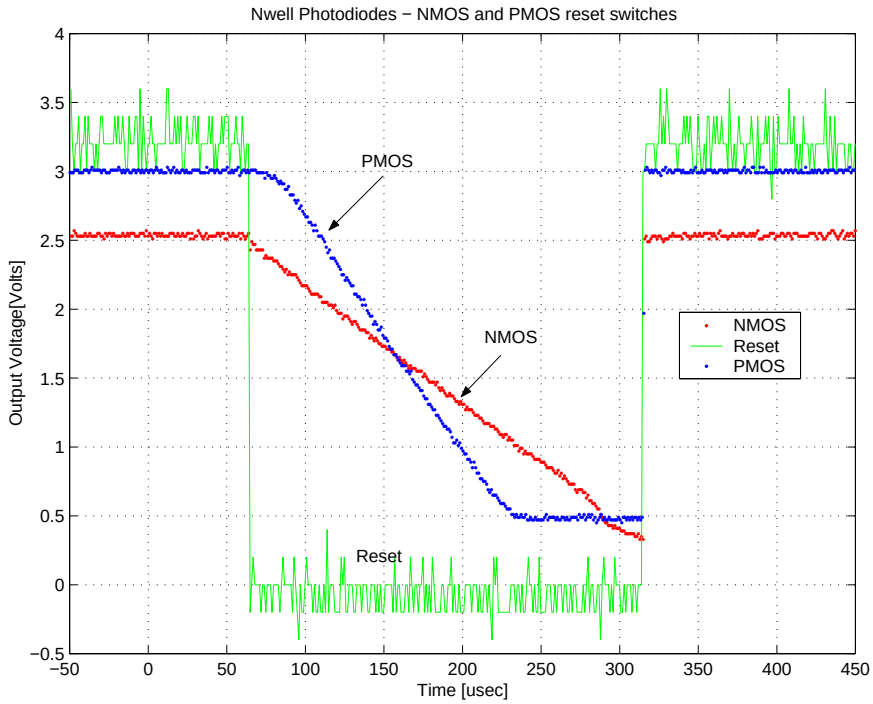



(a) Measured sequential reaodout (IMAGER) timing

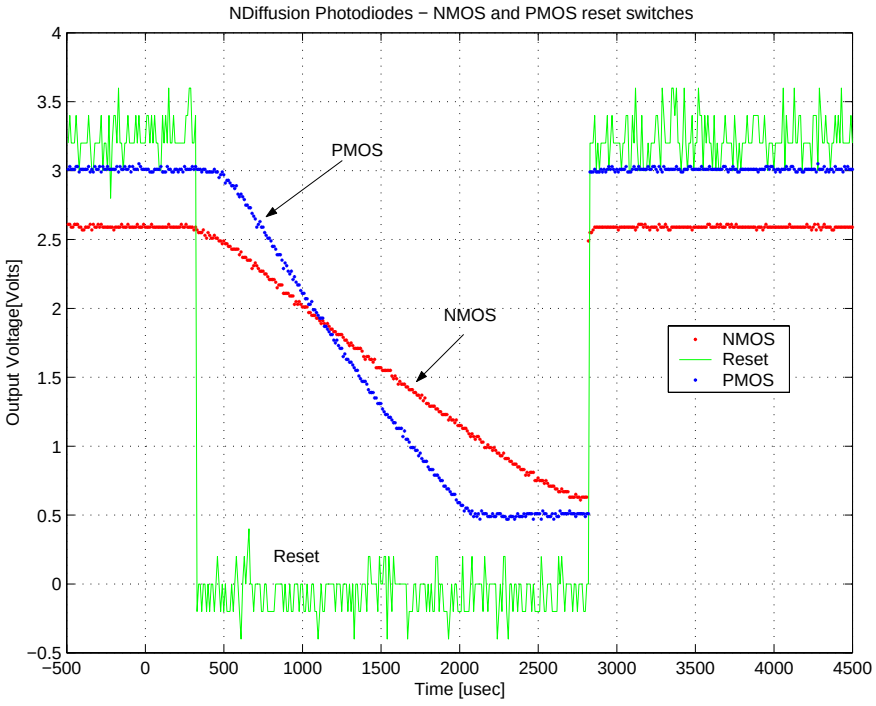



(b) Measured non-destructive readout (SPECTROMETER) timing

Figure 5.23: Array performance




(a) Nwell - Psubstrate photodiode




(b) Ndiff - Psubstrate photodiode

Figure 5.24: Photodiode response

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# Chapter 6

# Digital Interface Using On-Chip ADC

The output of the prototype imager chip described in the previous chapter is analog. To perform the digital signal processing on the output signal, it has to be first converted to an equivalent digital signal. Also, on-board analog signals are less immune to noise and signal integrity issues. Therefore digital interface for the imager chips is required. To implement a imager chip with full digital interface requires an on-chip analog to digital converter (ADC). The various considerations for the choice of the ADC architecture and implementation of a high resolution ADC in standard CMOS technology are presented next.

## 6.1 ADC Architecture Choice

There are many considerations for on-chip ADC. The ADC must support video rate data rates and the resolution required is at least 8 bits. The ADC must also have low integral non-linearity(INL) and differential non-linearity(DNL) to prevent the distortion of the image. Low power realization of the ADC is required to prevent the introduction of hot spots with excess dark current generation[1]. The substrate noise coupling from the ADC to the image

sensor would deteriorate the image quality and hence has to be minimized. There are many possibilities for implementation of on-chip ADC. The ADC can be implemented as single ADC or several ADCs, for example one per column or one per pixel. Single slope ADCs [1], Pixel level sigma delta ADCs [2] have been reported. But the pixel level approach reduces the fill factor and single slope ADCs are inadequate for high resolution and low to medium conversion rates. Also the analog output of the pulse modulated and hence pipelined ADC architecture is used in this research. The implementation of a pipelined ADC is presented in the following section.

## 6.2 Pipelined ADC

Pipeline is method of speeding up high volume processes in which a big task is divided into a number of steps, each requiring approximately equal amount of time to perform. In a pipelined ADC, the conversion operation is divided into a number if steps. The most significant bits are resolved in the first step and the least significant steps are resolved in the last step. The block diagram of a pipelined ADC is shown in figure 6.1 . The sample and hold amplifier is used to hold the analog input or the residue from the preceding stage. This enables the first stage of the pipeline to perform a coarse quantization on an sample of the signal while the second stage processes the previous sample. The residue is calculated by subtracting the appropriate reference value[1] from the analog input signal. The residue is amplified so that the comparison process may again be done with same set of references in order to generate the next most significant bits. This process is repeated until the desired accuracy is obtained. Traditionally, the sample and hold amplifier, residue amplifier and the gain block are implemented by a single switched capacitor amplifier [3], [4], [5] shown in figure 6.2 . Even though single ended implementation is shown, differential configuration is used in actual implementations. The sources of error in pipelined ADC with switched

[1] The reference value infact correponds to the analog equivalent of the digitized analog signal

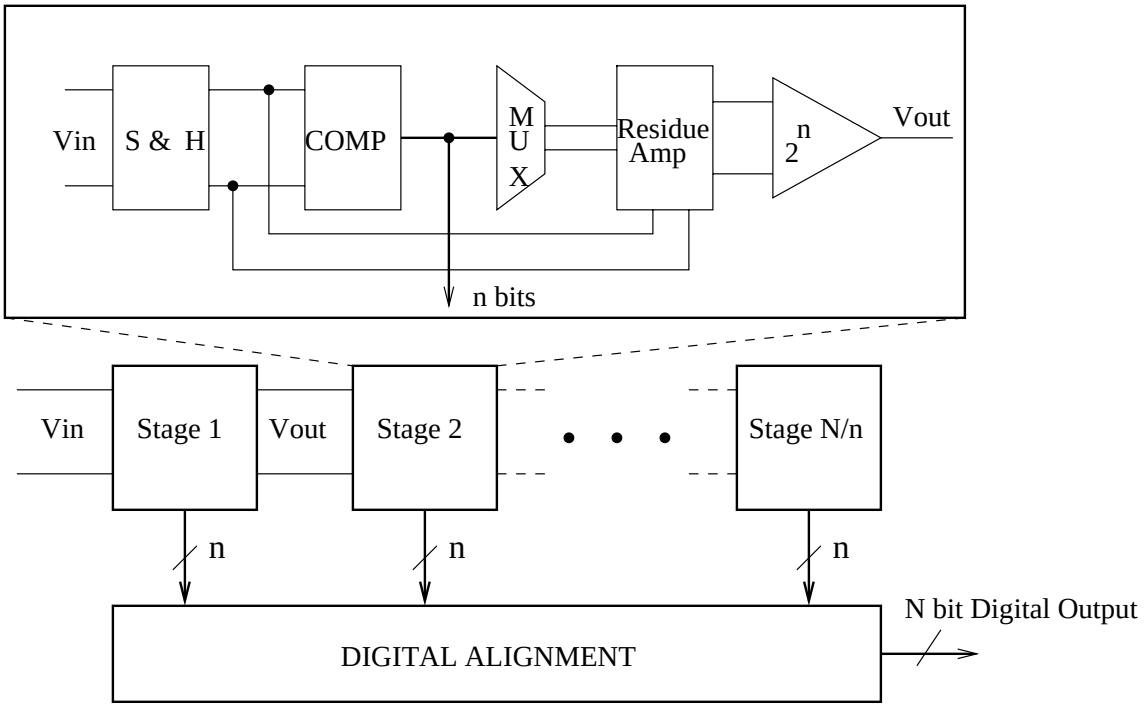



Figure 6.1: Block diagram of a pipelined ADC

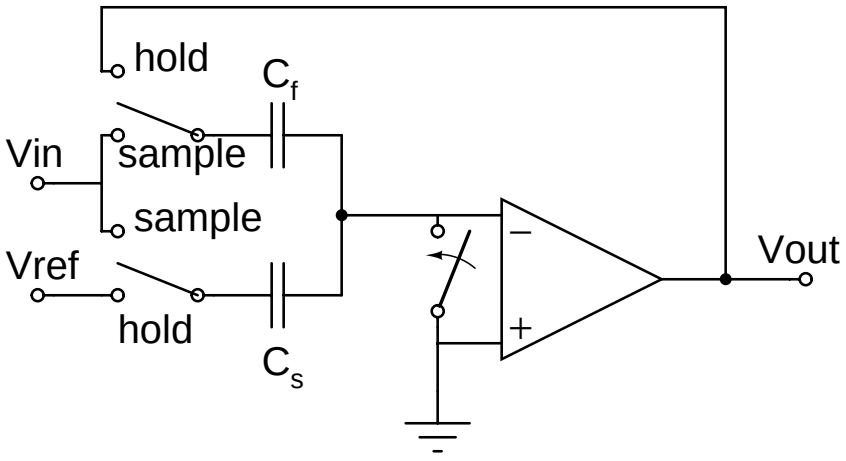



Figure 6.2: Switched capacitor implementation of residue amplifier

capacitor based residue amplifier is thoroughly investigated in [6]. The major source of error are listed below.

- Thermal noise from sampling switches and kT/C noise of the sample and hold amplifiers
- Comparator offsets
- Residue amplifier gain error resulting from the capacitor mismatch and finite gain opamp
- Non-uniform reference levels
- Incomplete settling of the sample and hold amplifier output

Thermal noise can be reduced by using large components. For a fixed input bandwidth, a trade-off exists between thermal noise, speed and power dissipation. The effect of comparator offsets can be reduced using digital correction [7]. The non-idealities due to non-uniform reference levels can be reduced using local bandgap reference circuits [8]. Errors due to incomplete settling of the sample and hold amplifier can be reduced by designing wide bandwidth opamps.

The effect of gain errors due to capacitor mismatch and finite opamp gain are analyzed using behavioral model for the ADC written in C programming language. The DNL and INL plots for various opamp gains and capacitor mismatches are presented in figures 6.3 and 6.4. It can be concluded from the simulation results that opamp gain in excess of 80dB and capacitor matching better than 0.1% is required to avoid missing codes. For better linearity (DNL/INL $<$ 0.5LSB) the constraints on matching are more stringent. So calibration techniques [9], [10], [11], [12], [13], [14], [15] are often used.

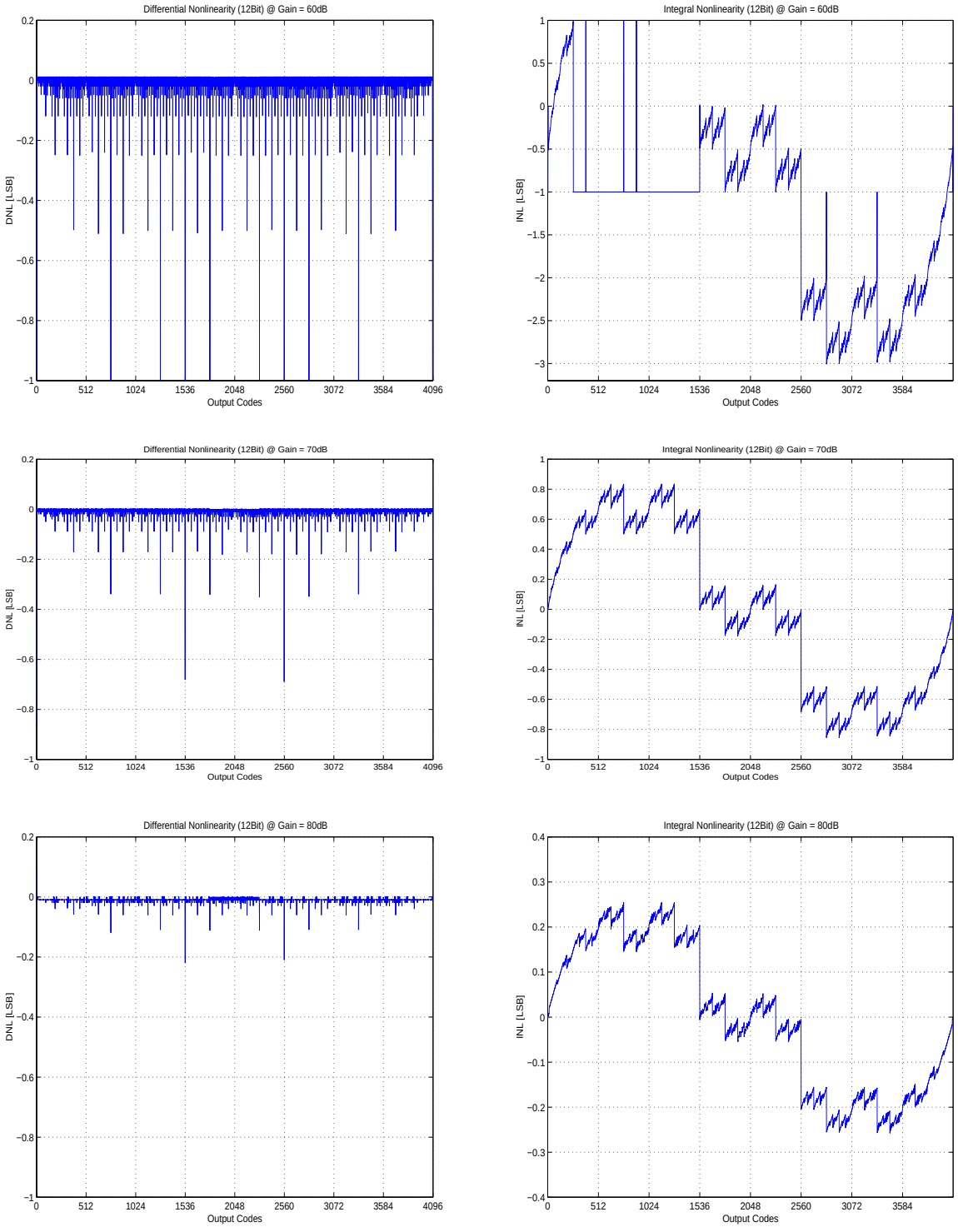



Figure 6.3: Effects of opamp finite gain on DNL and INL

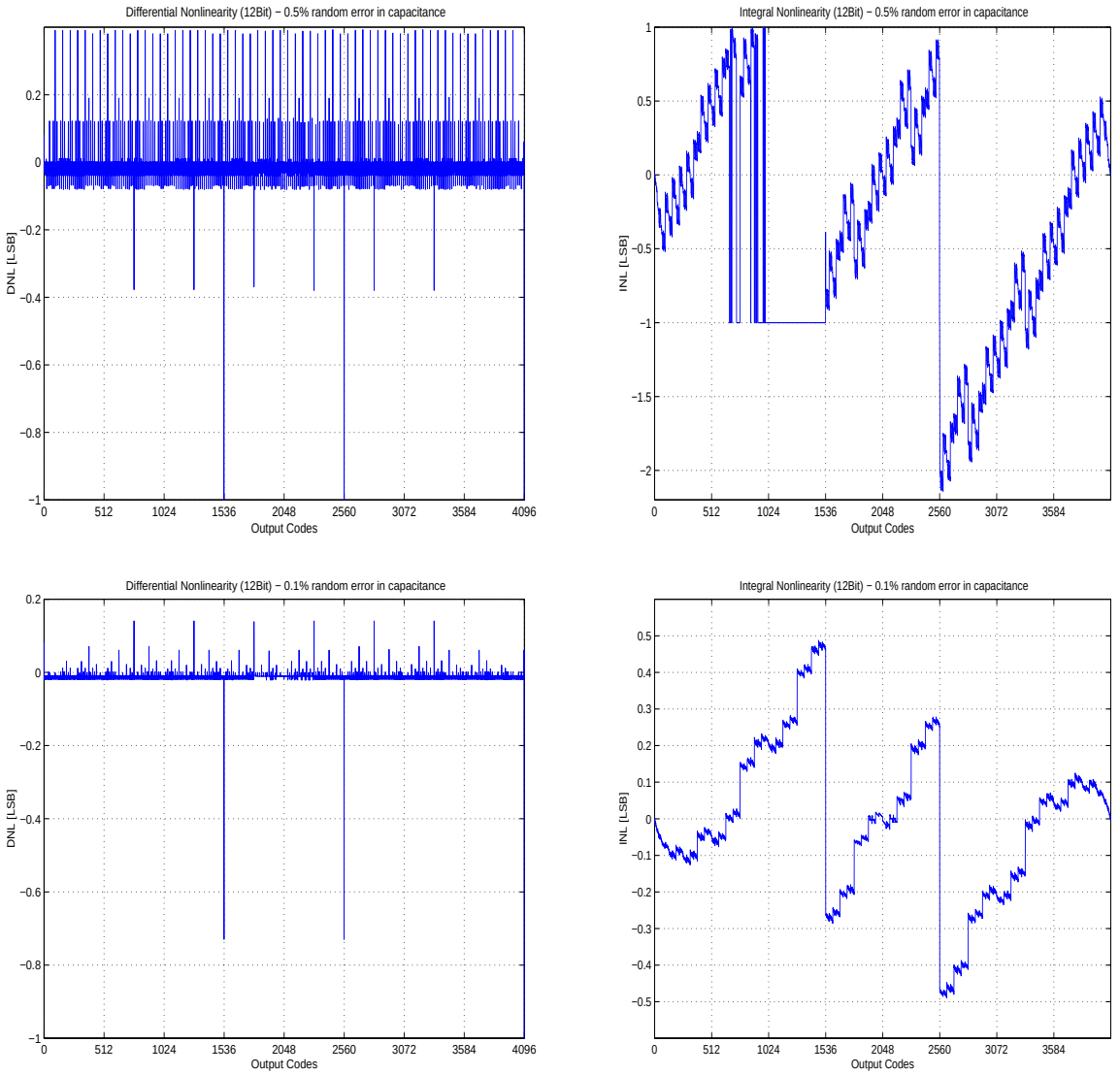



Figure 6.4: Effects of capacitor mismatch on DNL and INL (80 dB gain is used for opamp)

## 6.3 Circuit Design

The ADC is based on a commonly employed 1.5 bits/stage architecture shown in figure 6.5 . Each stage resolves two bits with a sub-ADC, subtracts this value from its input, and amplifies the resulting residue by a gain of two. Digital correction algorithm is implemented by overlapping and adding each bits. Latches are used to hold the bits. This architecture has been shown to be effective in achieving high throughput at low-power [4], [16]. The low number of bits per stage coupled with digital correction relaxes the constraints on comparator offset and dc opamp gain. The stages are implemented with switched capacitor residue amplifiers that provide sample and hold, differencing and amplifying operations as shown in figure 6.6 . The switched capacitor residue amplifier operates a two phase clock. During the first phase, the input signal $Vin$ is applied to the input of the sub-ADC, which has thresholds at +Vref/4 and -Vref/4. The input signal ranges from -Vref to +Vref. Simultaneously, $Vin$ is applied to sampling capacitors $C_s$ and $C_f$. At the end of the first clock phase, $Vin$ is sampled across $C_s$ and $C_f$, and the output of the sub-ADC is available. During the second clock phase, $C_f$ closes a negative feedback loop around the opamp, while the top plate of $C_s$ is switched to the appropriate reference using the output of the sub-ADC. The output of the stage can be mathematically expressed as,

$$V_o = \begin{cases} (1+\frac{C_s}{C_f})V_i - V_{ref} \ , & if \ V_i > V_{ref}/4 \\ (1+\frac{C_s}{C_f})V_i \ , & if \ -V_{ref}/4 \leq V_i \leq V_{ref}/4 \\ (1+\frac{C_s}{C_f})V_i + V_{ref} \ , & if \ V_i < -V_{ref}/4 \end{cases}$$

The gain of the residue amplifier can be set by choosing appropriate values of $C_s$ and $C_f$ capacitors. For the 1.5 bits/stage architecture, $C_s = C_f$ to achieve a gain of two. The design of various building blocks - comparator, Opamp will be presented in the next section.

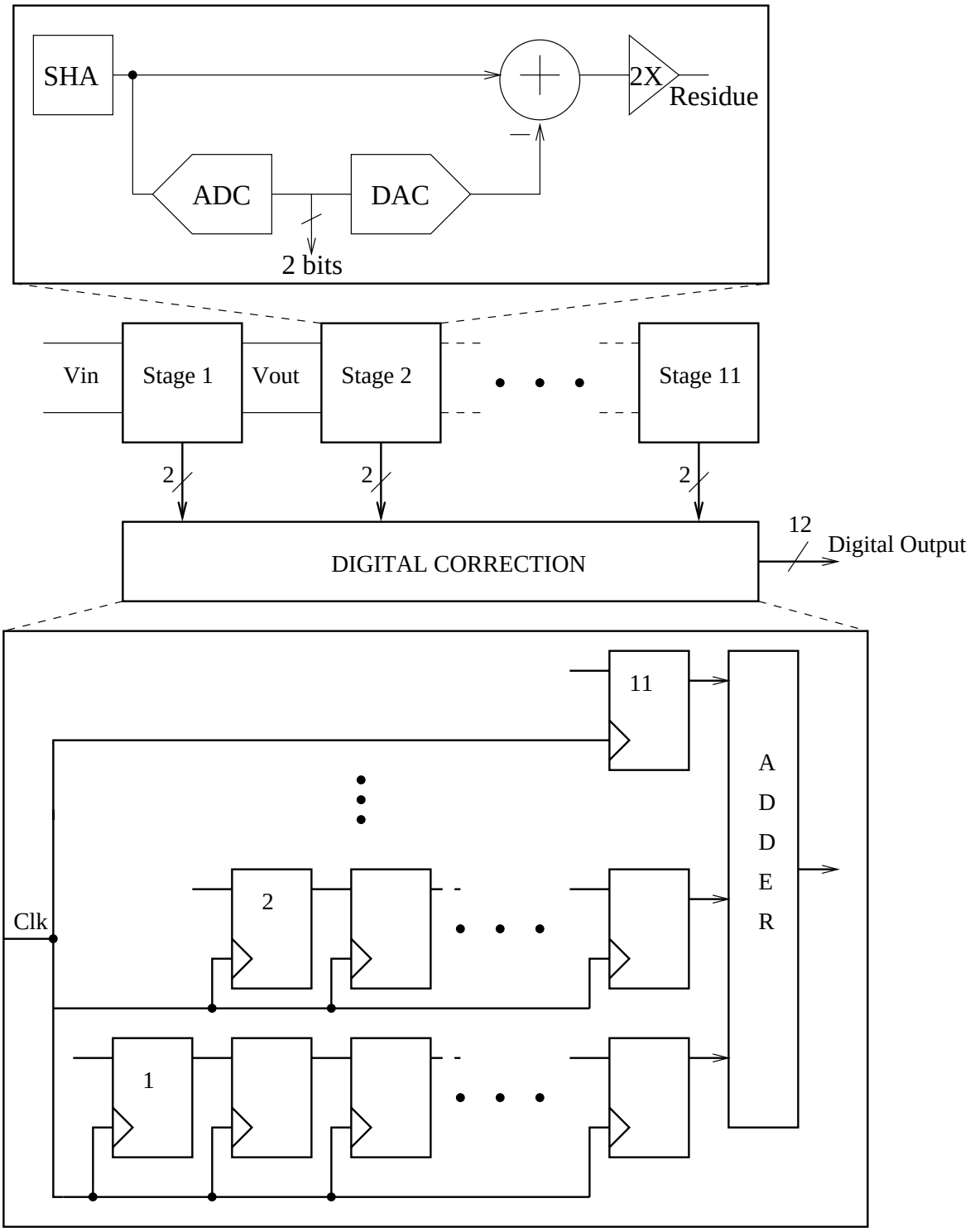



Figure 6.5: 1.5 bits/stage pipelined ADC architecture

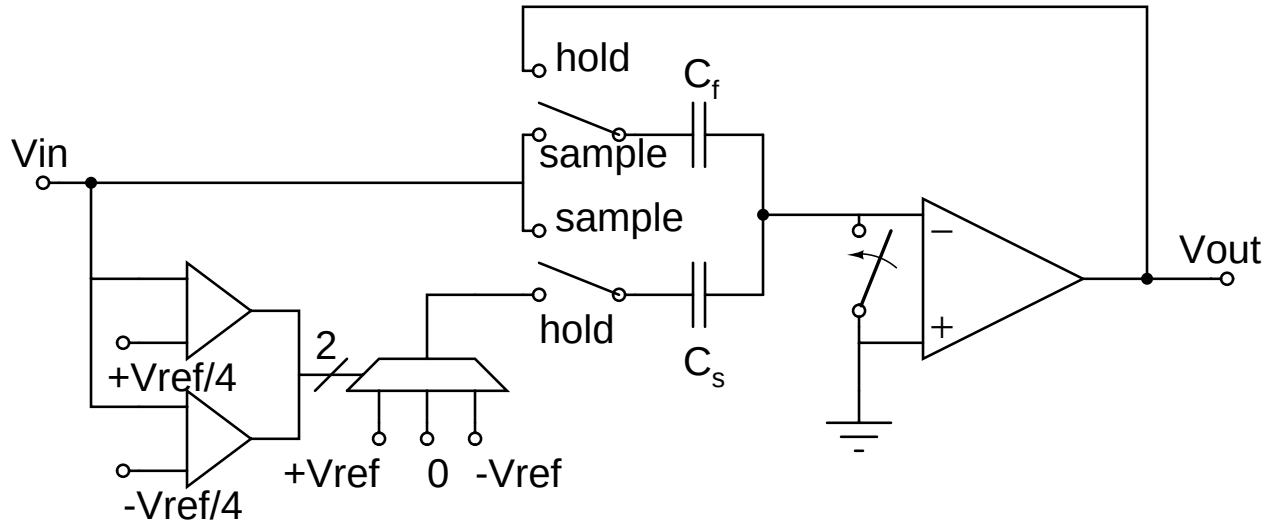



Figure 6.6: Implementation of each stage of the pipeline

### Comparator design

The schematic of the comparator is shown in figure 6.7 . The tail NMOS transistors are biased in triode region and they behave like voltage controlled resistors. The input voltage which causes the conductance of NMOS pairs is the comparator threshold voltage and is given by [4],

$$V_{in}\,|_{threshold} = \frac{W_2}{W_1} \cdot V_{ref}$$

where $V_{in} = V_{inp} - V_{inn}$ and $V_{ref} = V_{refp} - V_{refn}$. The uncritical comparator threshold can be set by choosing appropriate ratio of the widths $\frac{W_2}{W_1}$. For the 1.5 bits/stage architecture, $\frac{W_2}{W_1}$ is equal to 1/4. When clk is low, the input is read in and the comparison is made by the NMOS variable resistors. When the clk is high, the difference generated by the NMOS variable resistors is amplified to rail voltages by the regenerative amplifier. Figure 6.8 shows the DC response of the comparator with threshold voltage equal to $\pm V_{ref}/4$.

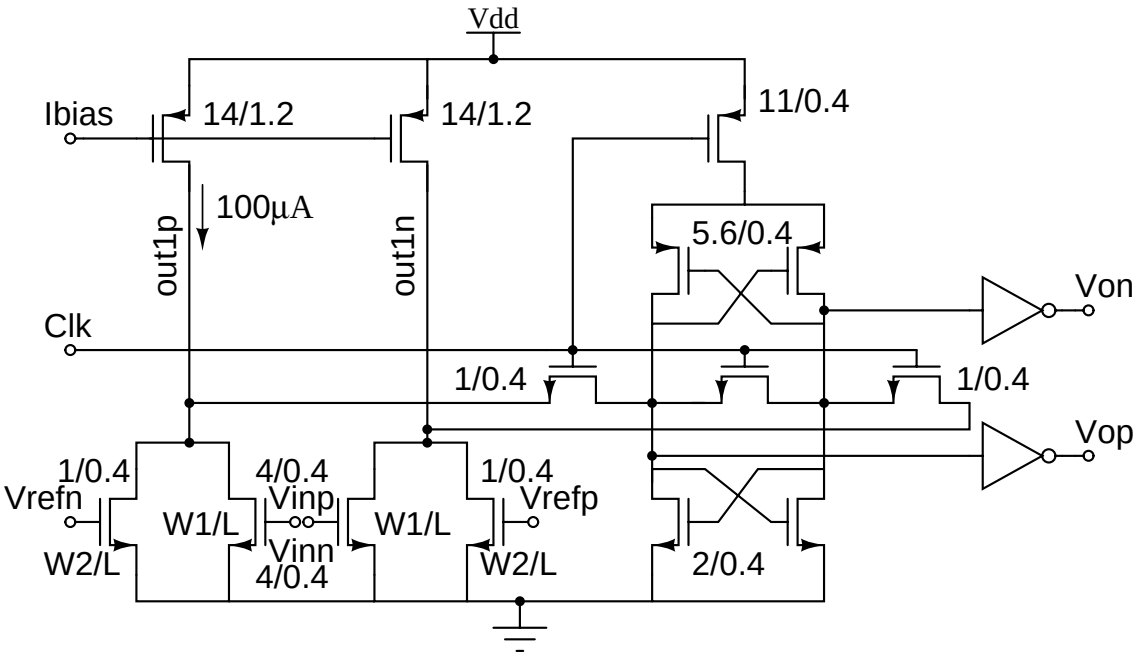
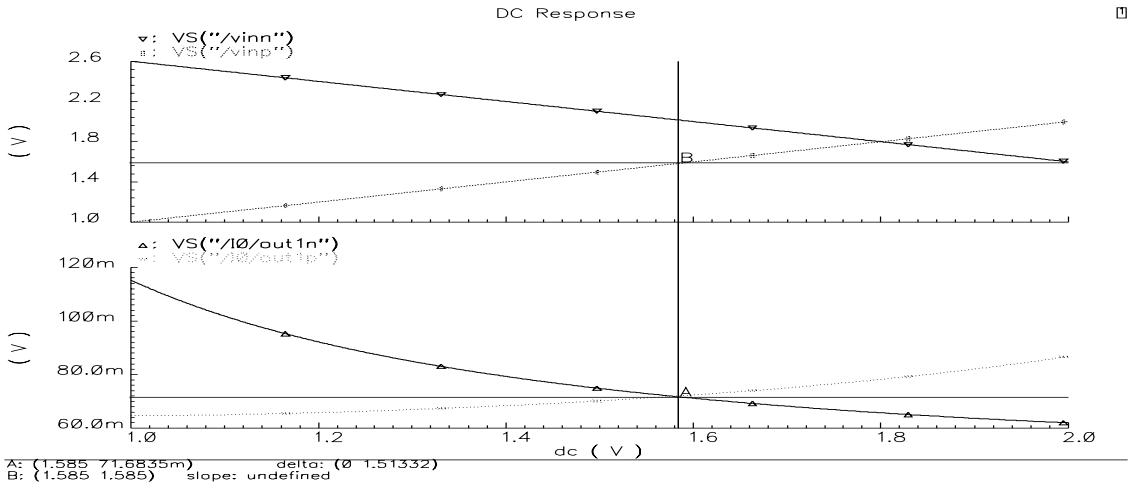



Figure 6.7: Comparator schematic (all sizes in $\mu m$)

### Opamp design

The schematic of the differential opamp is shown in figure 6.9. The first stage of the opamp is a folded cascode structure with NMOS input transistors. It is followed by a cascoded common source second stage. The opamp has a gain greater than 100 dB and unity gain bandwidth (UGB) of 65 MHz (see figure 6.10(a) ) which is much greater than the minimum required UGB of 28 MHz for 12 bit settling in 100ns for 5 MHz operation. The output swing of the opamp is greater than $1.6\,V_{peak-to-peak}$ (see figure 6.10(b)). The input transistors are sized for high $g_m$ and the cascode transistors and bias transistors are sized for high output swing. The output stage is designed to reduce resonant peaking due to high Q parasitic pole pairs [17]. The two stage opamp is compensated by a miller capacitor with out any series zero-nulling resistor. The compensation compensation capacitor is realized using voltage-coefficient compensated MOSCAPs biased in strong inversion. The voltage-coefficient compensation scheme is explained in the following section.




(a) Comparator with threshold voltage equal to -Vref/4

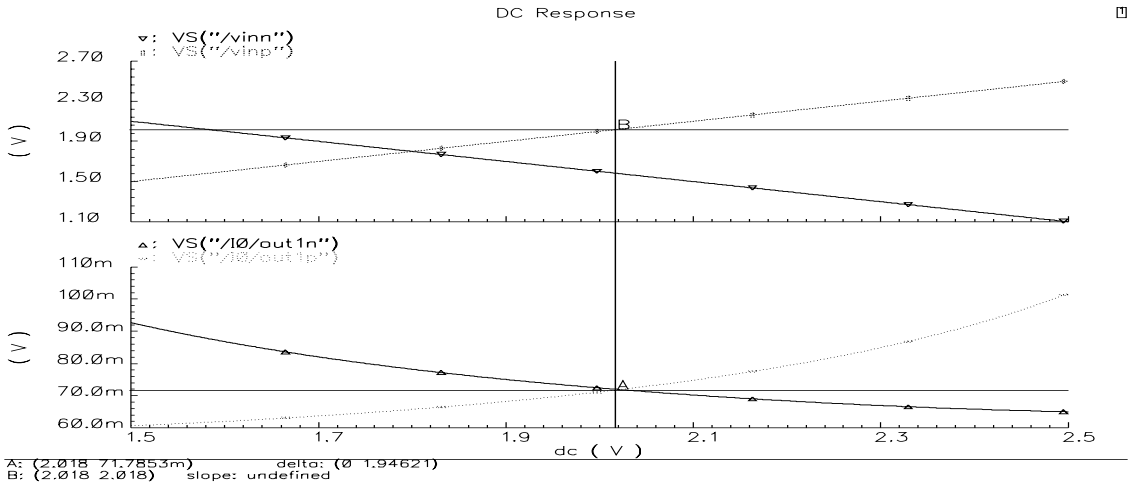



Figure 6.8: DC response of the comparator

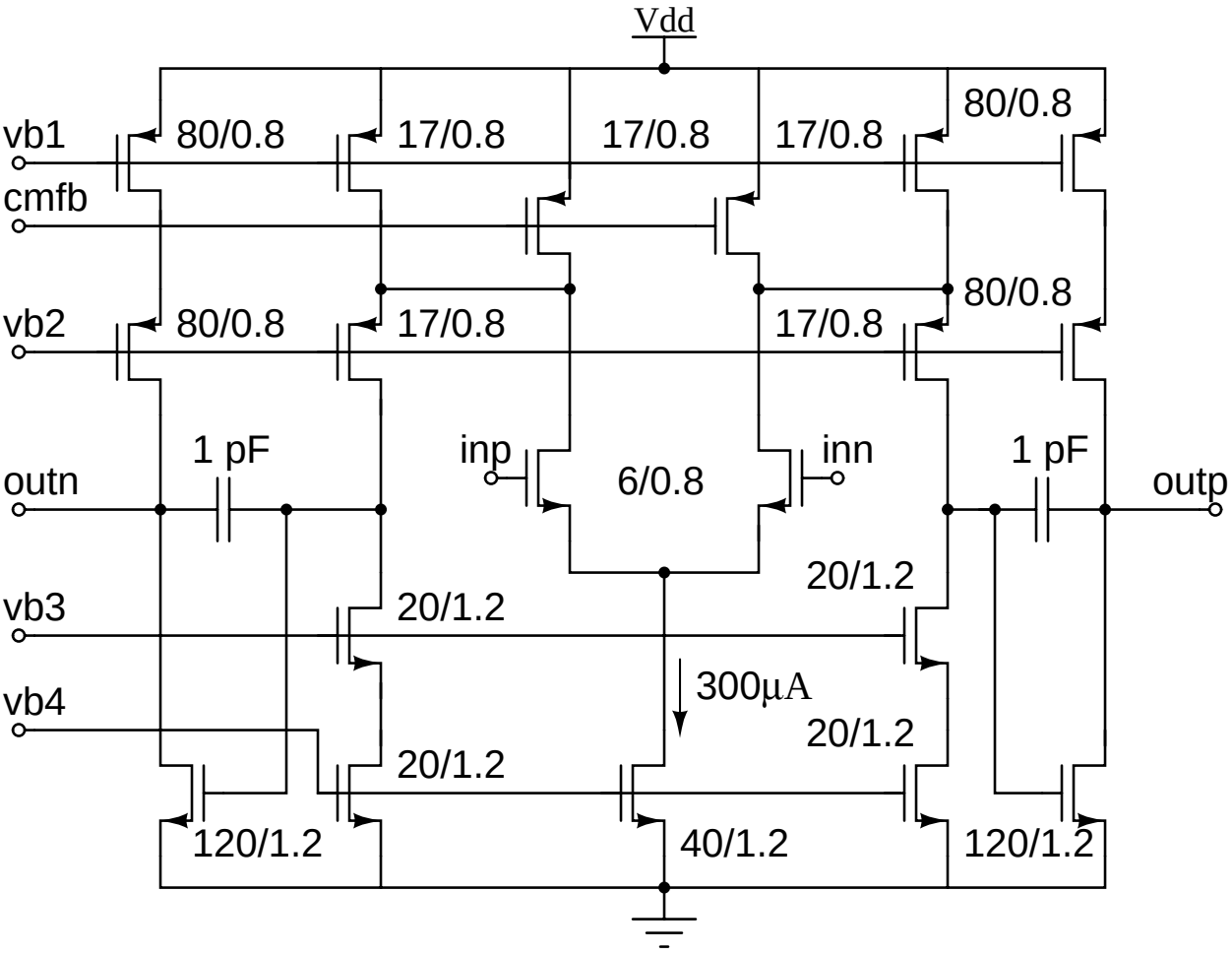
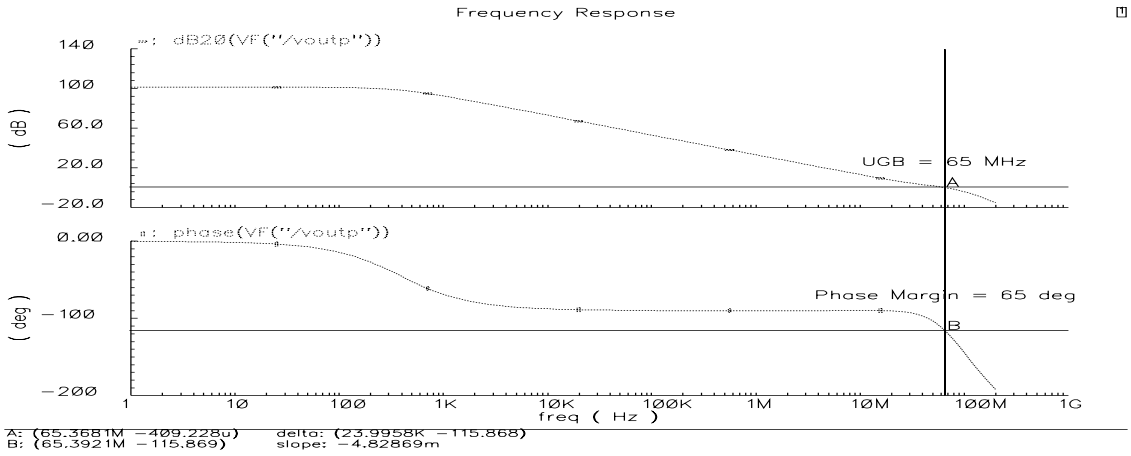
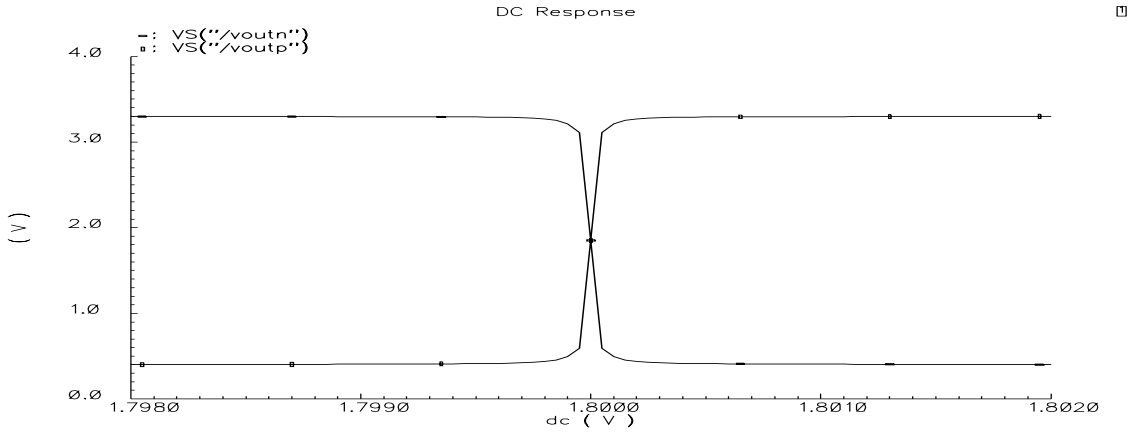



Figure 6.9: Two stage differential opamp (all sizes in $\mu m$)




(a) Frequency response with 3 pF load capacitance




(b) DC response of the opamp

Figure 6.10: Opamp performance

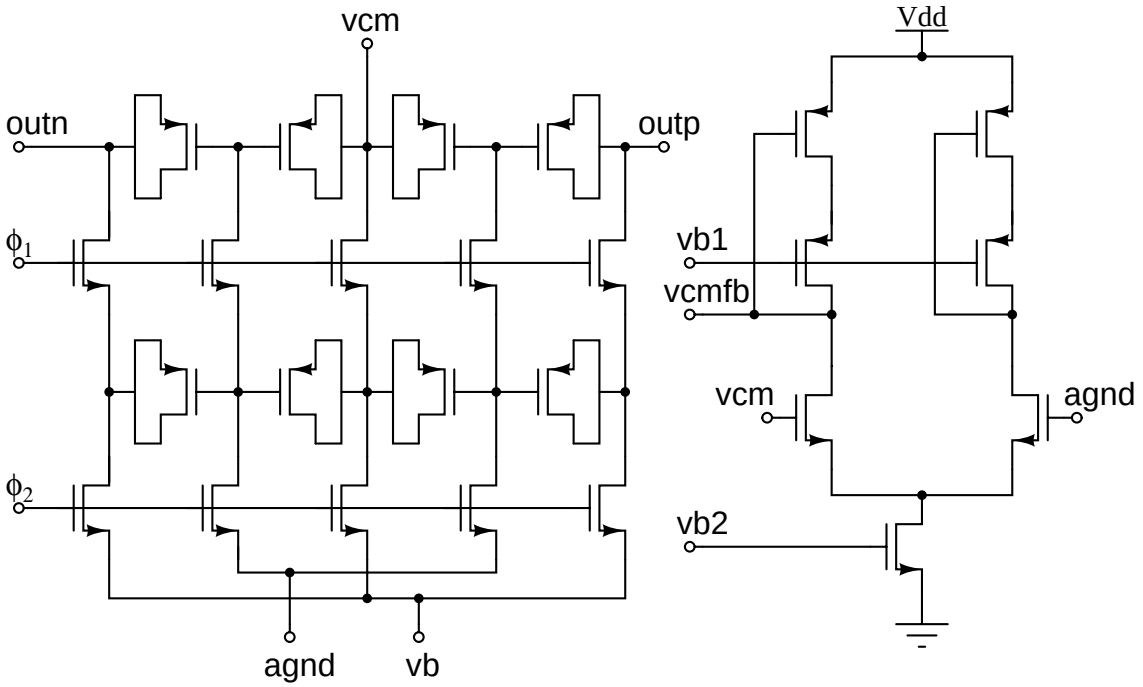



Figure 6.11: Switched capacitor CMFB circuit

In most differential opamps, the output swing is limited by the common mode feedback (CMFB) circuit. A switched capacitor CMFB circuit shown in figure 6.11 [18] is used. Again, MOSCAPs are used for capacitors. The output common mode voltage, $vcm$, is obtained by averaging the differential output. Then $v_{cm}$ is compared to the required common mode voltage, $agnd$, by the differential amplifier to generate the CMFB voltage $vcmfb$. The load transistors of the CMFB differential amplifier are cascoded to reduce the output offset voltage.

### Series Compensated MOSCAPs

The capacitance realized using the gate-to-channel capacitance is referred to as MOSCAP. There are several advantages of using MOSCAPs - larger capacitance per unit area, low random capacitance variation due to poly granularity. The main disadvantage of the MOSCAP device is the large voltage dependence of the capacitance realized. A series compensation

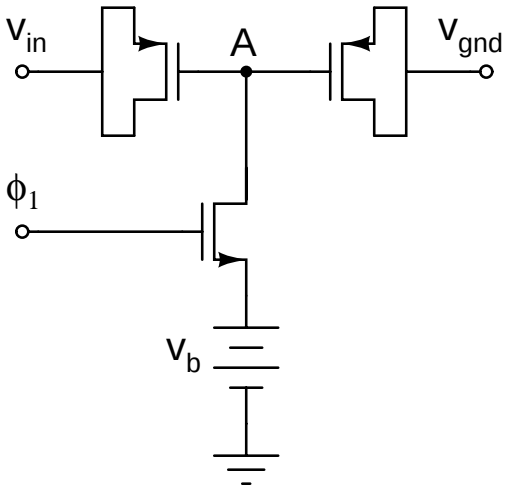



Figure 6.12: Series non-linearity compensation scheme

scheme [18] to counter the large voltage coefficients in MOSCAPs is presented. To realize floating capacitors, the well-embedded device is chosen. The MOSCAPs are biased in strong inversion to facilitate schematic simulations. Figure 6.12 illustrated the series non-linearity compensation technique. The top plates of two equal valued MOSCAPs $C_1$ and $C_2$ are connected in series, joined at their top plates. When $\phi_1$ goes high, the top plates are connected to the positive dc bias voltage $V_b$. The bias voltage biases both the capacitors in strong inversion. The bottom plates of $C_1$ and $C_2$ the are connected to ground and virtual ground respectively. In the next clock phase , $\phi_2$, the switch connecting the bias voltage to the top plate is open, and node A will be floating. Since the input is connected to the bottom plate of $C_1$, the potential of the floating node will be changed by approximately $V_{in}/2$. Then, one of the capacitances increases while the other decreases due to this voltage change. Since the two capacitors are connected in series, the non-linearity of their total capacitance will be cancelled to the first order approximation.

A potential problem with the series compensation scheme is that the voltage $v_A$ might swing below negative supply voltage. It it does, the p-n junction between the drain and substrate of the NMOS switch may become forward biases, and that will result in a leakage

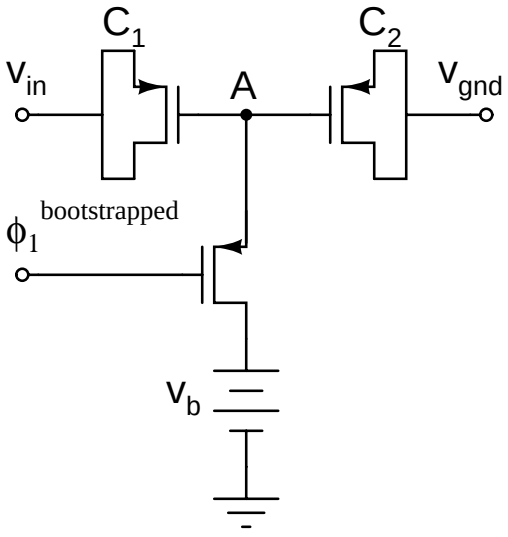



Figure 6.13: Improved series non-linearity compensation scheme

of charge. In order to circumvent this problem, a PMOS switch is used with bootstrapped clocking as shown in figure 6.13 .

### Digital Error Correction

Digital error correction is used to ease the requirements on the comparator design. For example, in a 1.5 bits/stage architecture, the offset of the comparator with digital error correction can be as high as $V_{ref}/4$. In a pipelined ADC, the odd stages are sampling when even stages are evaluating and vice versa. So for a given input sample, the output of each stage is present at half clock cycle interval and progresses down the pipeline. When the output from the first stage is ready, the second stage output will be ready half clock cycle after. Therefore, the sampled input signal can not be corrected until the last stage has finished the conversion. In order to perform the digital correction, the output from stage N is delayed until the output from the last stage is available. The correction is done by taking (N+1)th stage output and adding to the Nth stage output with one bit overlap from the LSB. The carry will propagate in the direction of MSB. Since the maximum code from each

stage is 10, for a full scale input, the output of the pipelined ADC with digital correction is one less the maximum code of the overall ADC.

### Capacitor mismatch minimization

The capacitor ratio errors cause non-linearity errors in the transfer characteristic from the input to the output of the pipelined ADC [6]. Capacitors in MOS technology are subjected to errors from two sources. One is the systematic error, which affects adjacent elements with identical geometries similarly. It can thus be reduced by proper matching techniques. The other is the random error, which differs from element to element, and therefore cannot be corrected by improved matching [19], [20], [21].

The major sources of systematic capacitance mismatch are mismatched perimeter ratios, proximity effects in unit capacitor photo lithography, mismatched long range fringe capacitance, mismatched interconnect capacitance and parasitic interconnect capacitance. As mentioned earlier, these systematic errors can be minimized by various layout techniques. A list of improved layout rules for matched capacitors are listed below [22] -

- The perimeter ratios of matched capacitors should be identical to the area ratios
- The structure surrounding each unit capacitor should be identical out to a distance of at least $30 - 50\mu m$ depending the feature size of the process
- Unit capacitors should be covered by a grounded metal layer where allowed
- Each external interconnect line in a capacitance must be paired with another external interconnect line running in the opposite direction

The major sources of random capacitance mismatch are random edge effects and random oxide effects. The random edge effect is due to the local and global random variations of the ideally straight edges of the capacitor. The random oxide effect is due to the local and global fluctuations of the oxide thickness and permitivity in the capacitor. Explicit

formulae are derived using the statistical methods for the random errors in [23]. They give the dependence of each error source on the physical dimensions, the standard deviations of the fabrication parameters.

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# Chapter 7

# Conclusions

This research identified Fixed Pattern Noise sources (FPN) in CMOS image sensors. Gain mismatch in the pixel amplifier, $k$TC noise and the offset mismatch in the sample and hold amplifier of the correlated double sampling circuitry are the major FPN sources. Gain mismatch is reduced by using closed loop opamps. The $k$TC noise is reduced using large hold capacitors. The use of closed loop opamps to increase the saturation voltage is also demonstrated. Two types of readout modes - sequential and non-destructive - are successfully implemented in the same chip. Timing signals for readout, CDS and power down are generated using pixel level control units. Power consumption is reduced by powering down all the columns except the column that is being accessed.

A $128 \times 1$ pixel test chip is fabricated in $0.4\mu m$, 1P4M standard CMOS process. The test results indicated 2 V saturation voltage and FPN of 20 mV. The main cause for the FPN is the offset of the sample and hold amplifier. The measured SNR is 54 dB and dark current is 200 mV/sec at room temperature.

Finally, a 12 bit pipelined ADC architecture to provide the digital interface for the imager chip is presented . Due to the non availability of linear capacitors, MOSCAPs are used. A series compensation technique is presented to bias the MOSCAP in strong inversion and hence reduce the voltage dependence of the capacitor.