ECE3204 Lecture 25

A/D Converters

Exam 3 Preview

Tomorrow:
Exam 3
Hand in all late HW/Lab

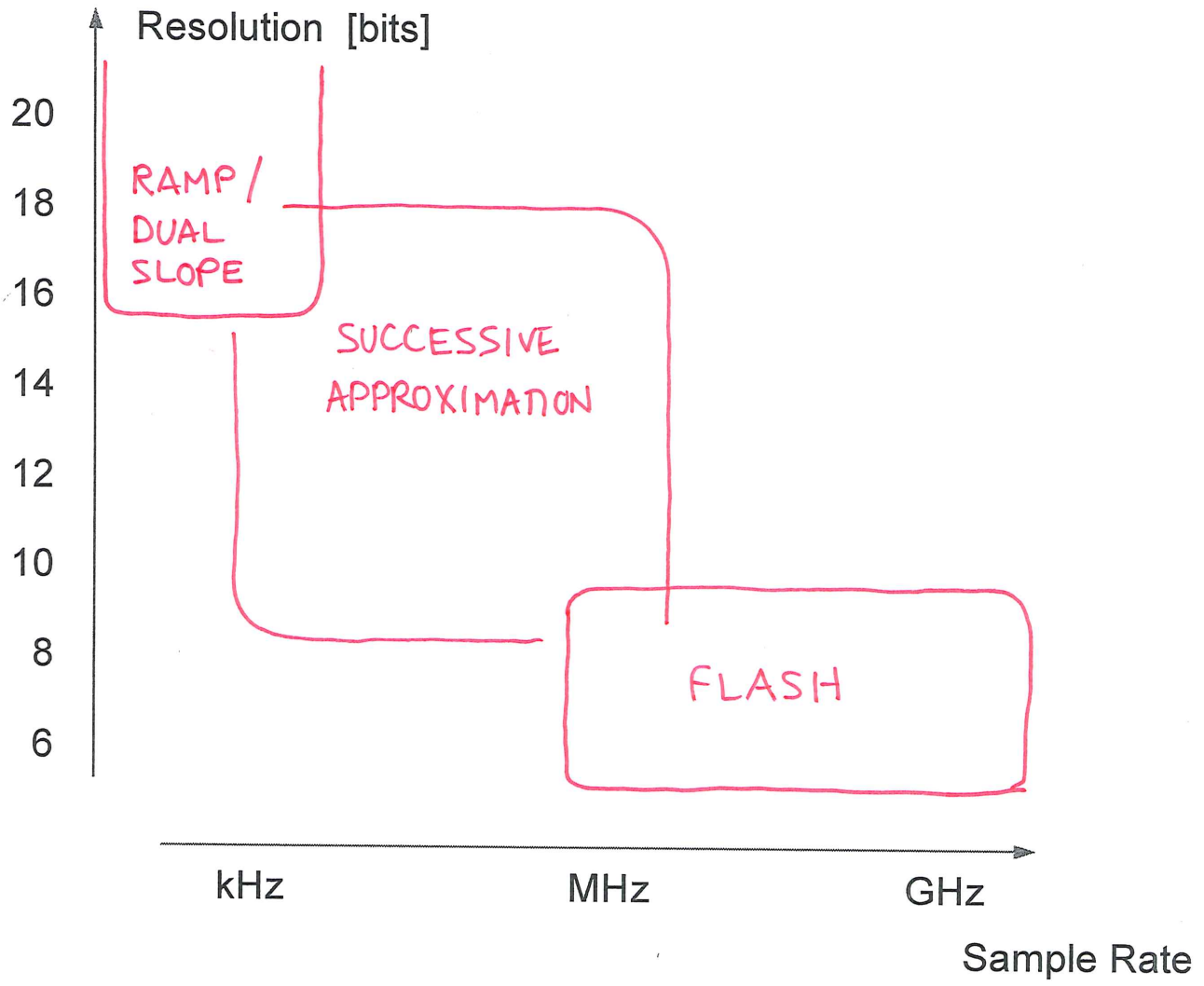
TEST TOMORROW

EMPHASIS

- FILTER CONCEPT
- S-PLANE
  - SPECIFY T(s)
  - MAP OF WAVEFORMS
- STABILITY
  - S-PLANE
  - LOOP GAIN
  - PHASE MARGIN
  - INSTABILITY FROM β

PLUS A LITTLE:
- S/H
- D/A

ADC Architecture Tradeoff: Sample Rate vs. Resolution

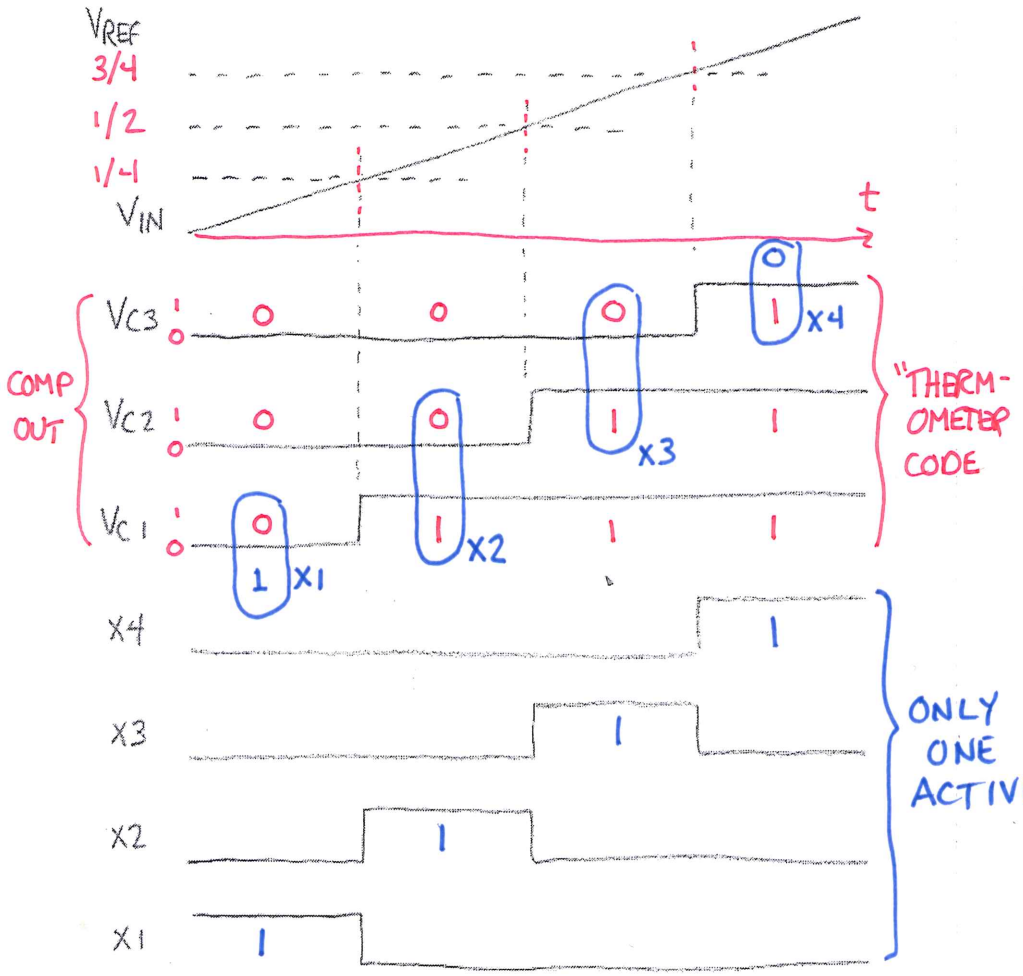


Flash ADC

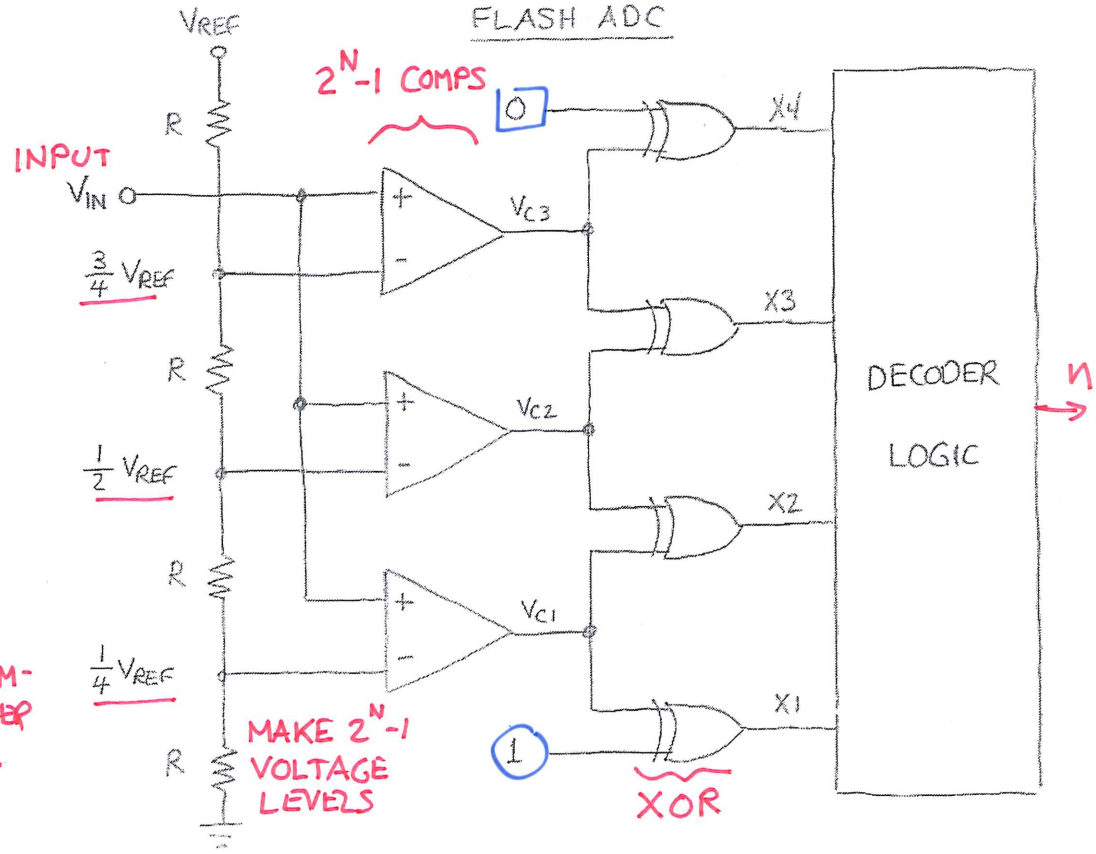
√ FAST 100s MHz → GHz

× COMPLEXITY 2^N-1 COMPS

4-8 BITS



"REFERENCE LADDER"

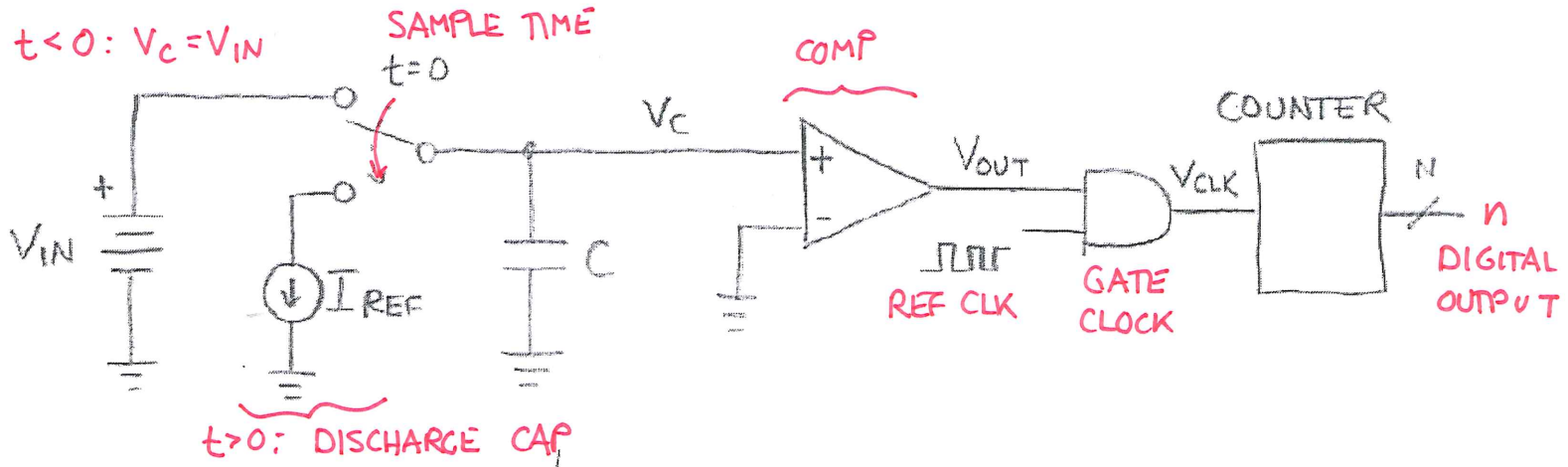


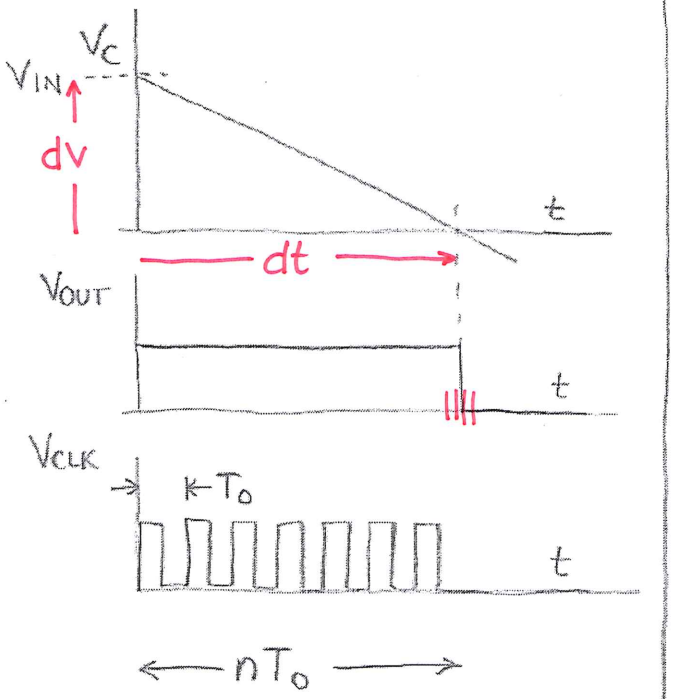
n OUTPUT
11
10
01
00

XOR

A	B	Y	
0	0	0	
0	1	1	} INPUTS DIFFERENT
1	0	1	
1	1	0	

Ramp ADC





FOR CAPACITOR

$$\frac{I}{C} = \frac{dV}{dt}$$

$$\frac{I_{REF}}{C} = \frac{V_{IN}}{nT_0}$$

$$n = V_{IN}\left[\frac{C}{I_{REF}\,T_0}\right]$$

STABLE

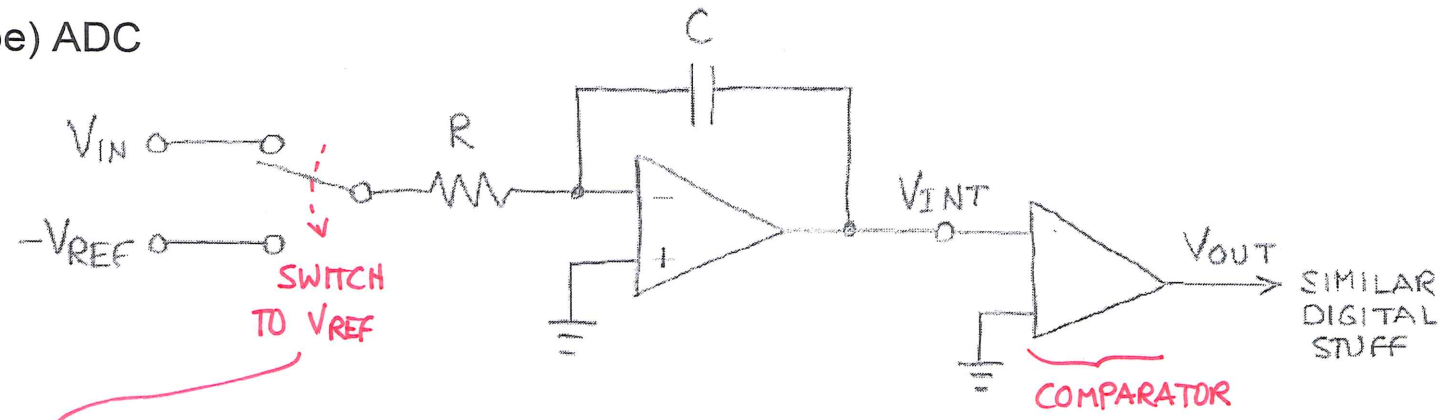
STABLE KNOWN

✓GOOD: $n \propto V_{IN}$

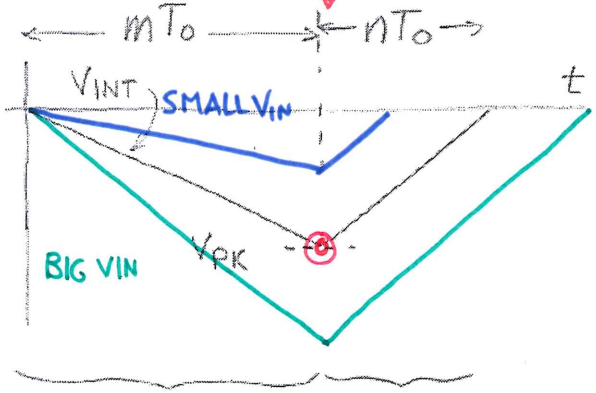
BAD: PROPORTIONALITY FACTOR DEPENDS ON I_{REF}, T_0, C

Integrating (Dual-Slope) ADC

✓ SIMPLE
✓ SCALABLE
× SLOW



INTEGRATE V_{IN} FOR FIXED TIME mT_0



INTEGRATE V_{IN} FOR mT_0
$m = 2^N$
N-BIT ADC

INTEGRATE $-V_{REF}$ UNTIL $V_{INT} = 0$ AFTER TIME nT_0

$$V_{INT} = \frac{-1}{RC}\int_{t_0}^{t} V_{IN}\,dt + V_{INT}(t_0)$$

FOR INTEGRATOR

$$V_{PK} = -RC\,V_{IN}\,\underbrace{mT_0}_{\text{FIXED}}$$

⊙ INITIAL CONDITION FOR 2nd INTEGRATION

ALSO

$$-V_{PK} = -RC(-V_{REF})nT_0$$

GET BACK TO ZERO: DEPENDS ON V_{PK}

SOLVE FOR n

$$-\cancel{RC}\,V_{IN}\,\cancel{mT_0} = -\cancel{RC}\,V_{REF}\,\cancel{nT_0}$$

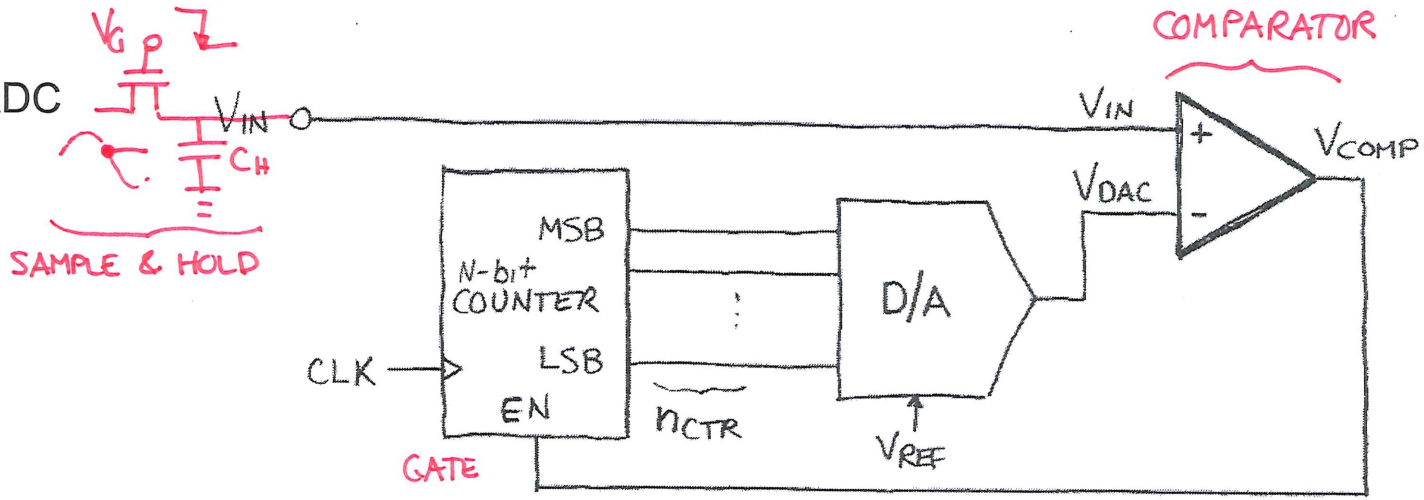
$$n = V_{IN}\left[\frac{m}{V_{REF}}\right]$$

FIXED

ONLY 1 THING NEEDS TO BE STABLE!

NICE: NOW PROPORTIONALITY FACTOR DEPENDS ONLY ON V_{REF}
VALUES OF R, C, T_0 UNIMPORTANT (AS LONG AS THEY ARE STABLE DURING THE CONVERSION TIME)

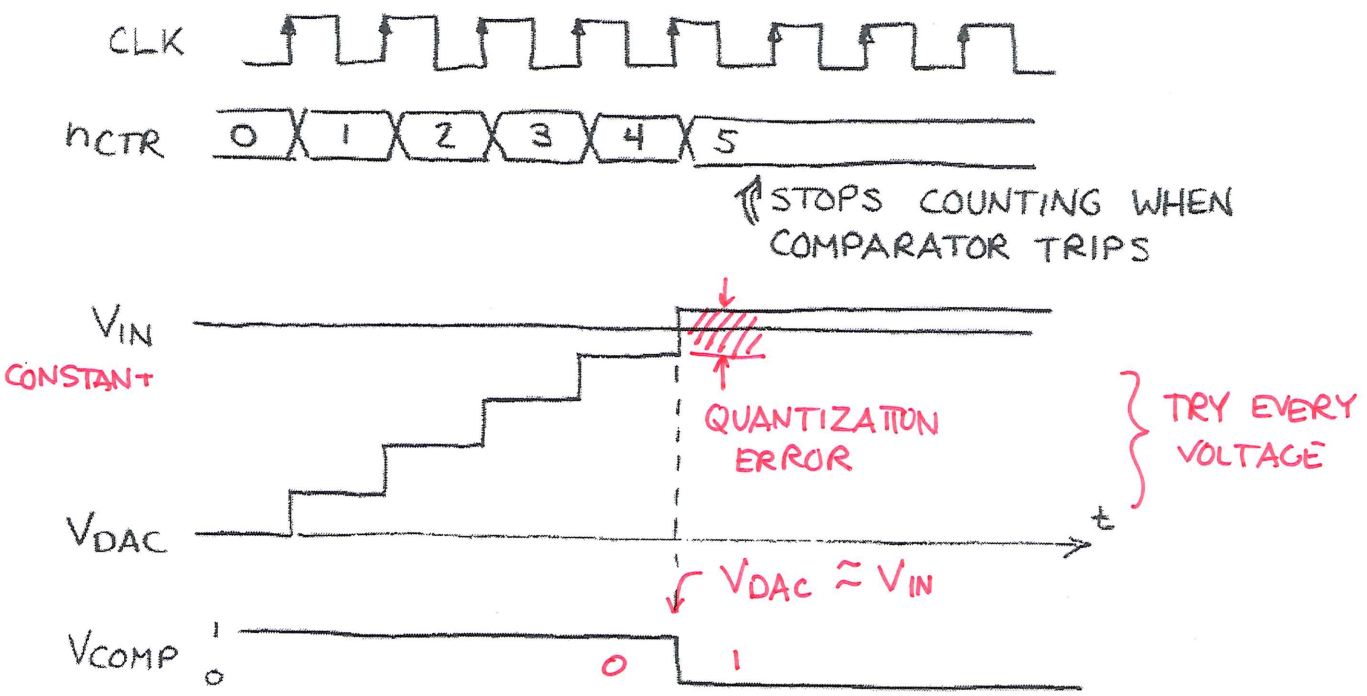
Counter (Feedback) ADC



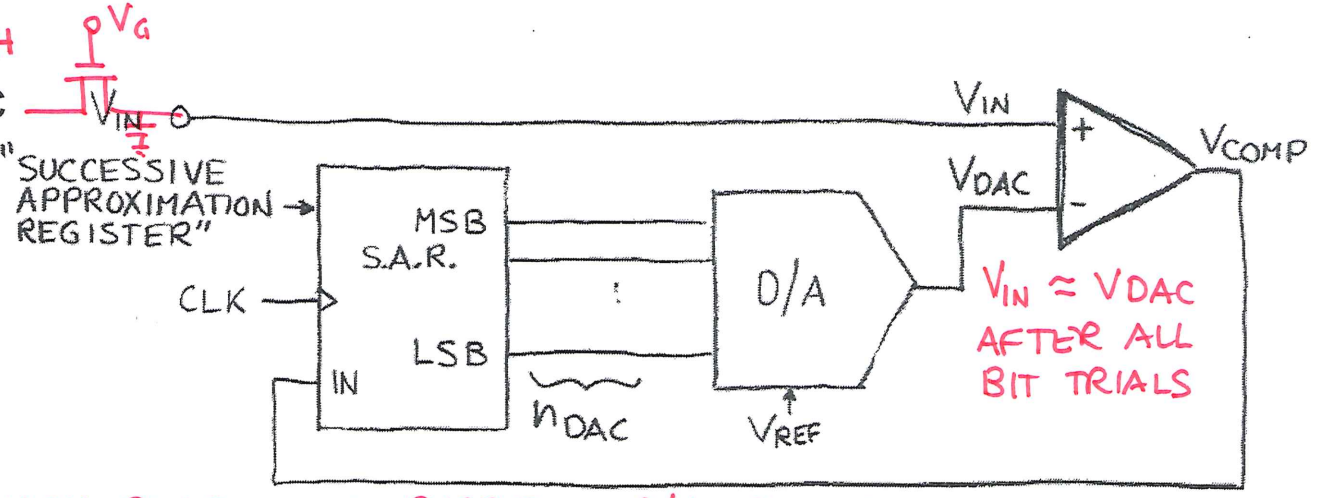
X TAKES TOO LONG!

N-BIT ADC

2^N COMPARISONS



Successive Approximation ADC



√ SPEED: N COMPARISONS

NEED N BIT D/A

BINARY SEARCH OF POSSIBLE D/A VALUES