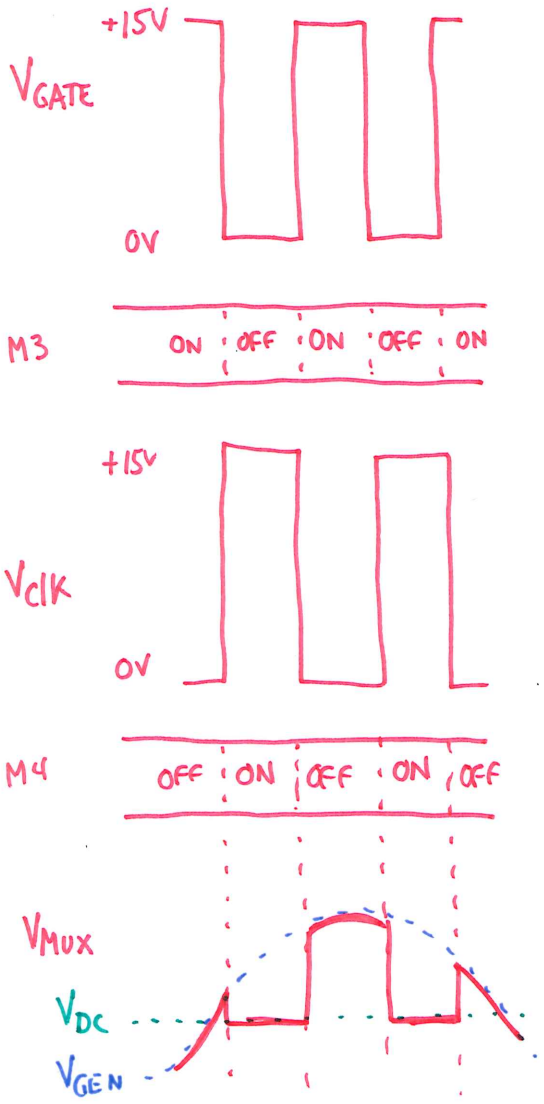
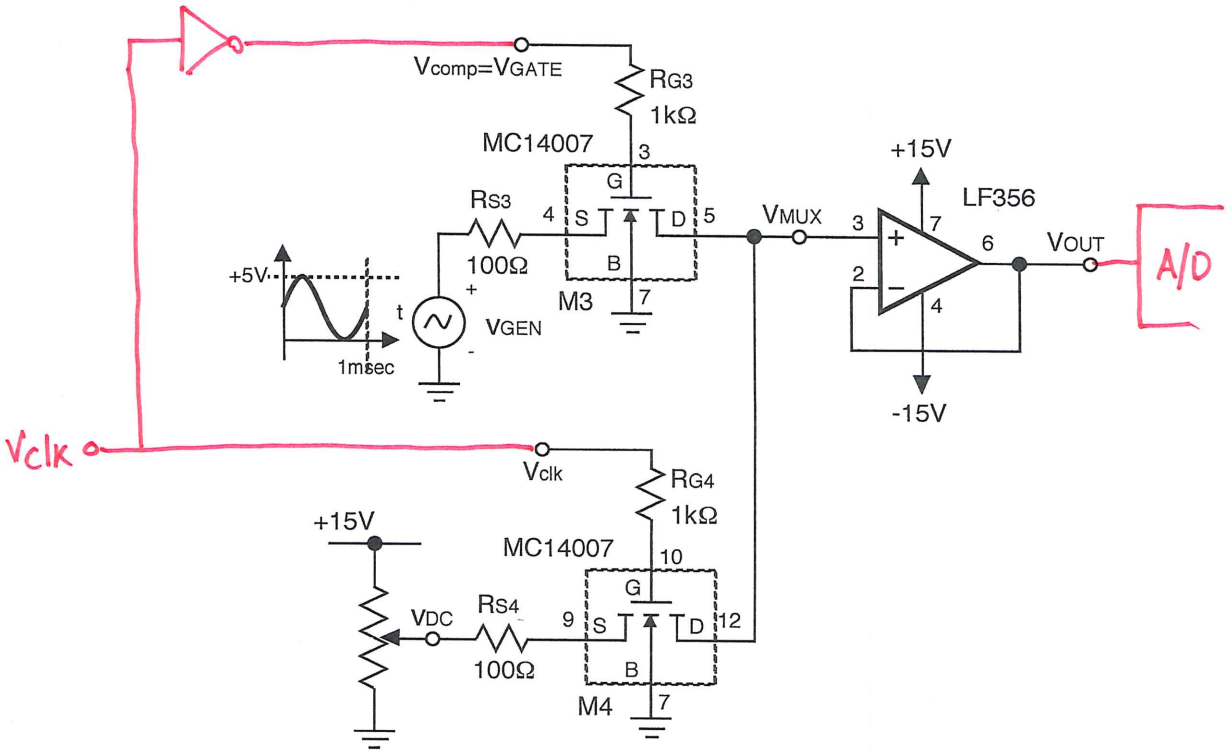
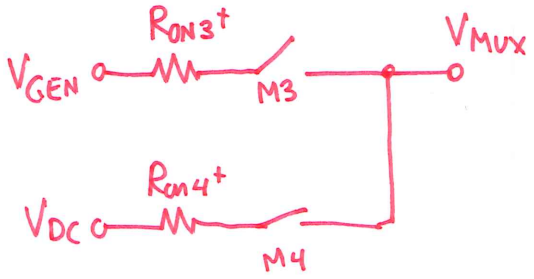
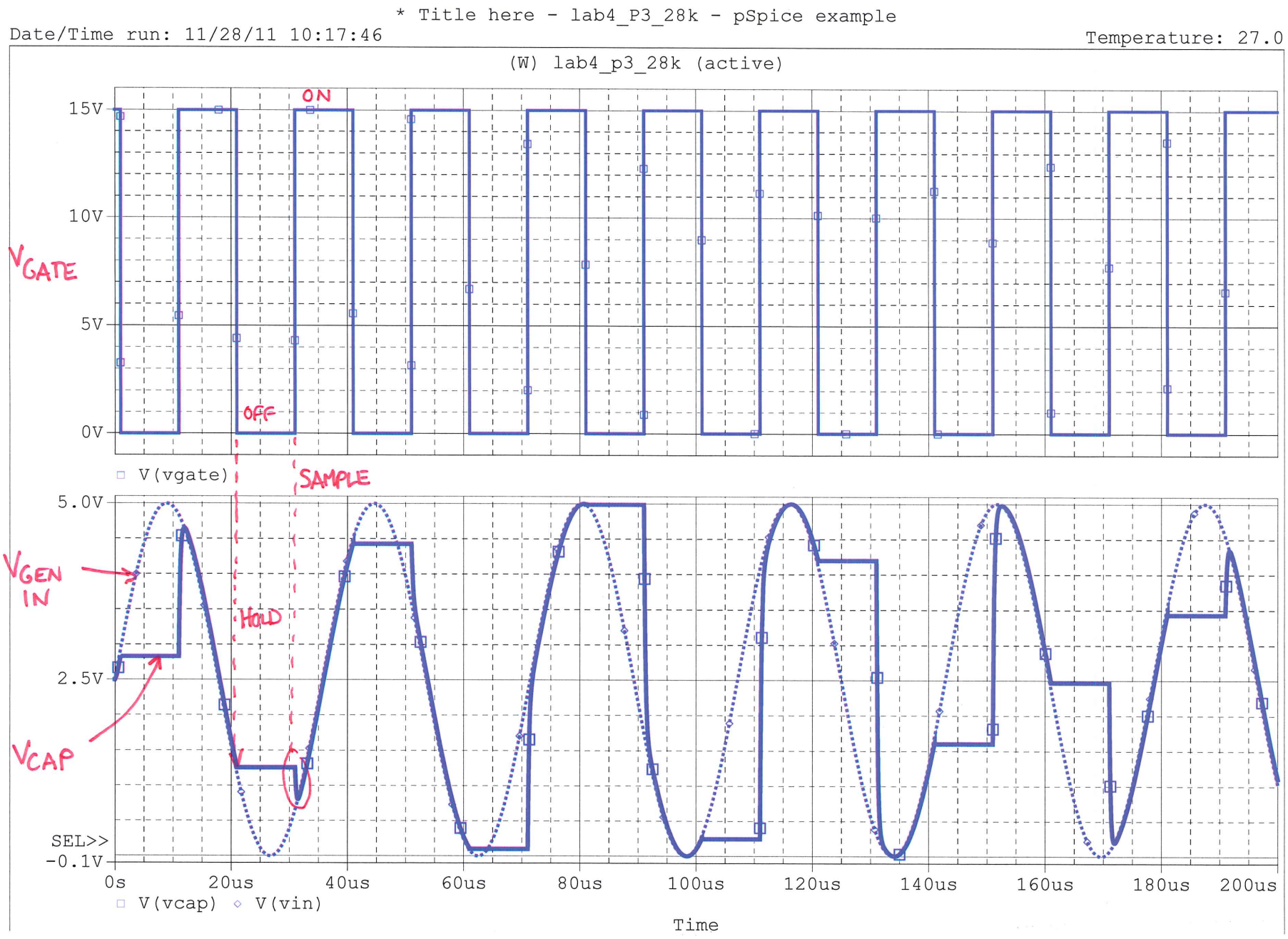
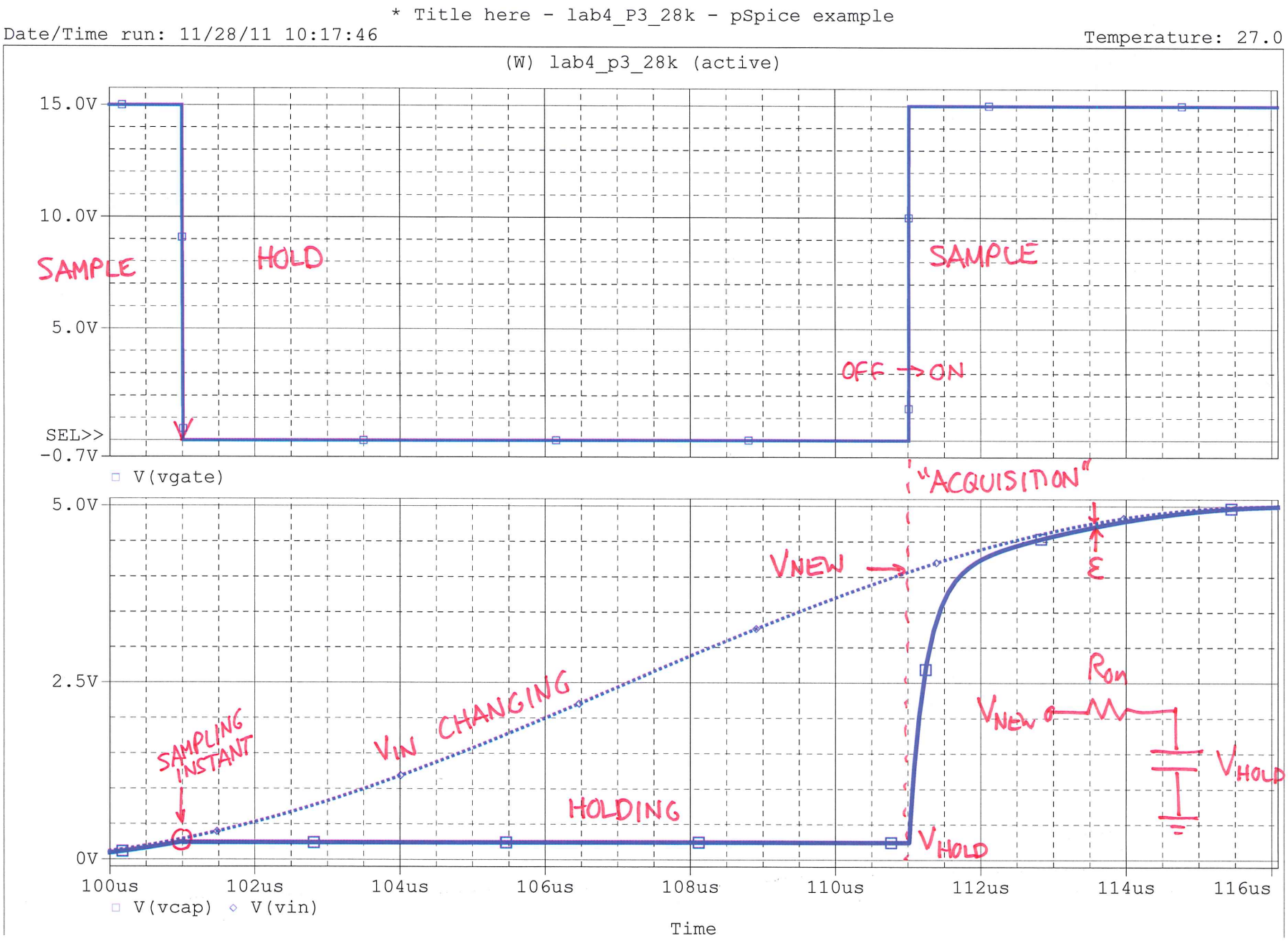
P4. Analog Multiplexer

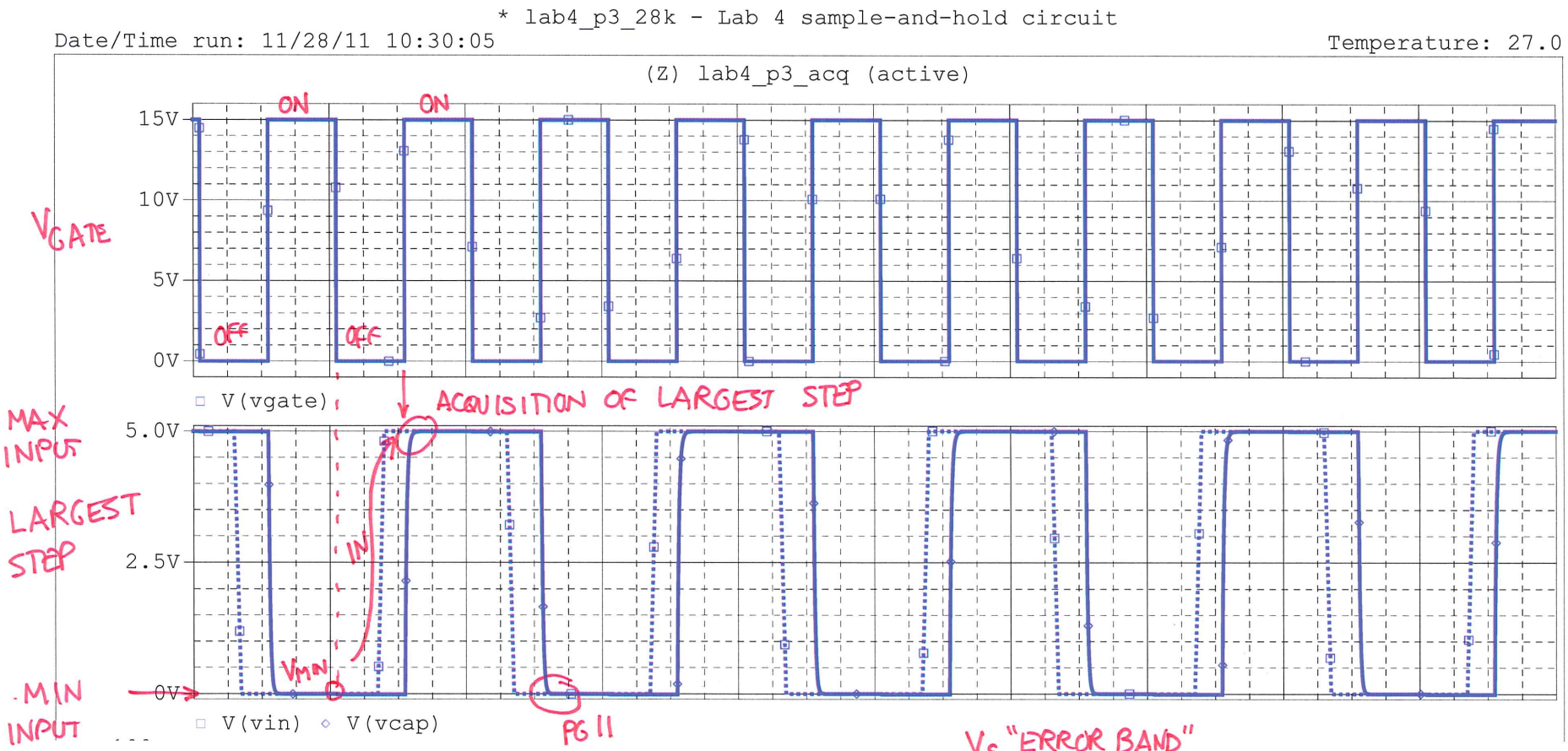




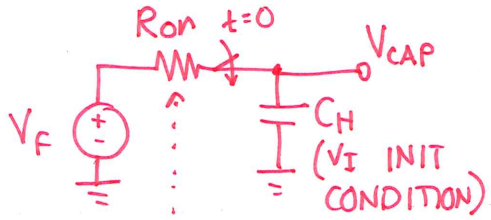



* Title here - lab4_P3_28k - pSpice example
Date/Time run: 11/28/11 10:17:46
Temperature: 27.0
(W) lab4_p3_28k (active)
15V
10V
5V
0V
ON
OFF
SAMPLE
V(vgate)
VGATE
5.0V
2.5V
SEL>>
-0.1V
VGEN IN
HOLD
VCAP
0s
20us
40us
60us
80us
100us
120us
140us
160us
180us
200us
V(vcap)
V(vin)
Time

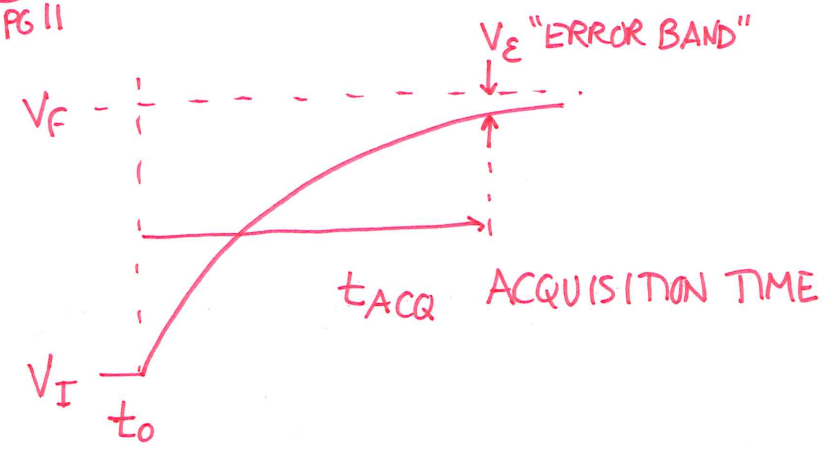

* Title here - lab4_P3_28k - pSpice example
Date/Time run: 11/28/11 10:17:46
Temperature: 27.0
(W) lab4_p3_28k (active)
15.0V
10.0V
5.0V
SEL>>
-0.7V
V(vgate)
SAMPLE
HOLD
SAMPLE
OFF -> ON
"ACQUISITION"
5.0V
2.5V
0V
VNEW
ε
Ron
VNEW
VHOLD
SAMPLING INSTANT
VIN CHANGING
HOLDING
VHOLD
100us
102us
104us
106us
108us
110us
112us
114us
116us
V(vcap)
V(vin)
Time

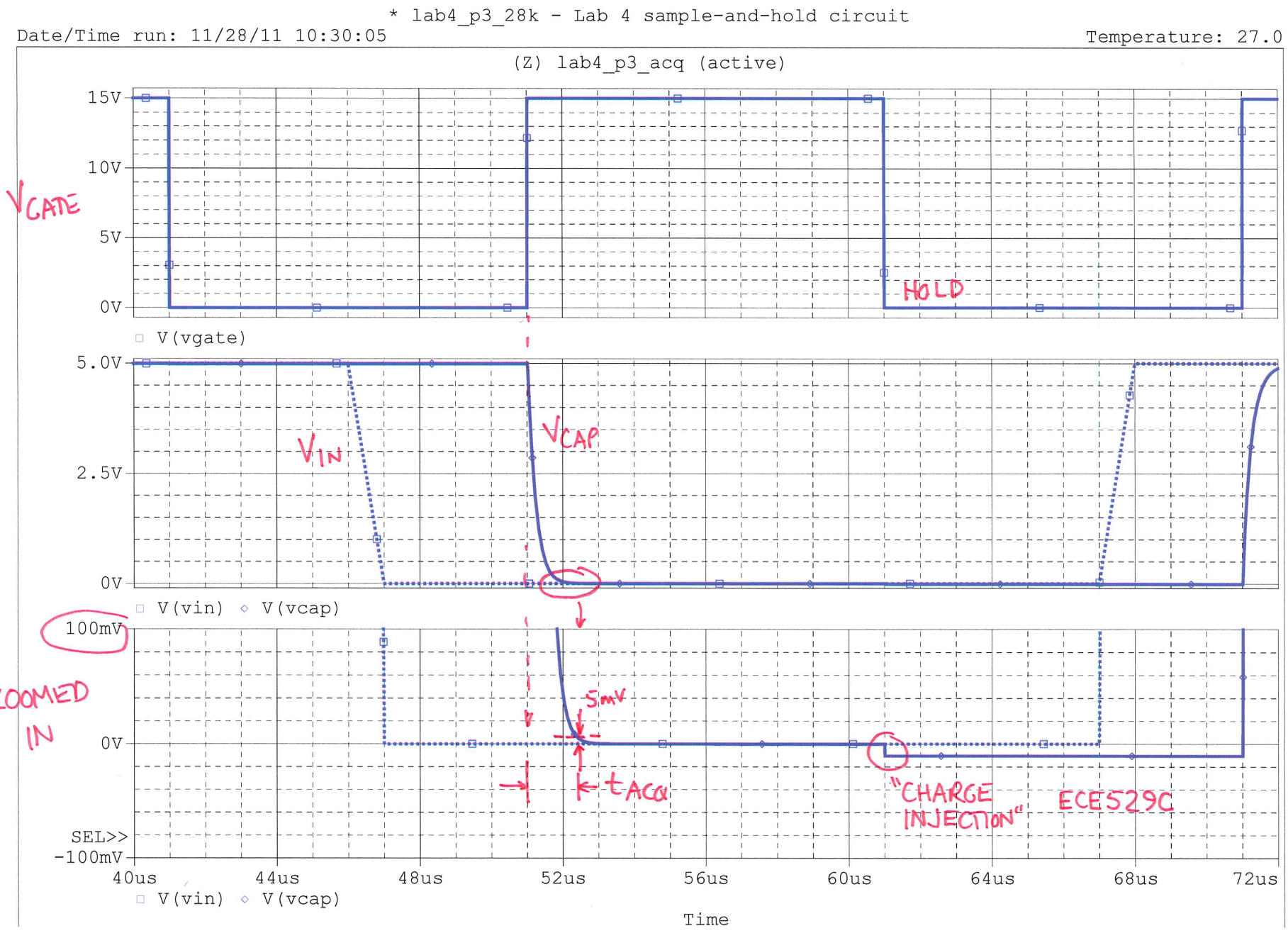


MODEL FOR ACQUISITION

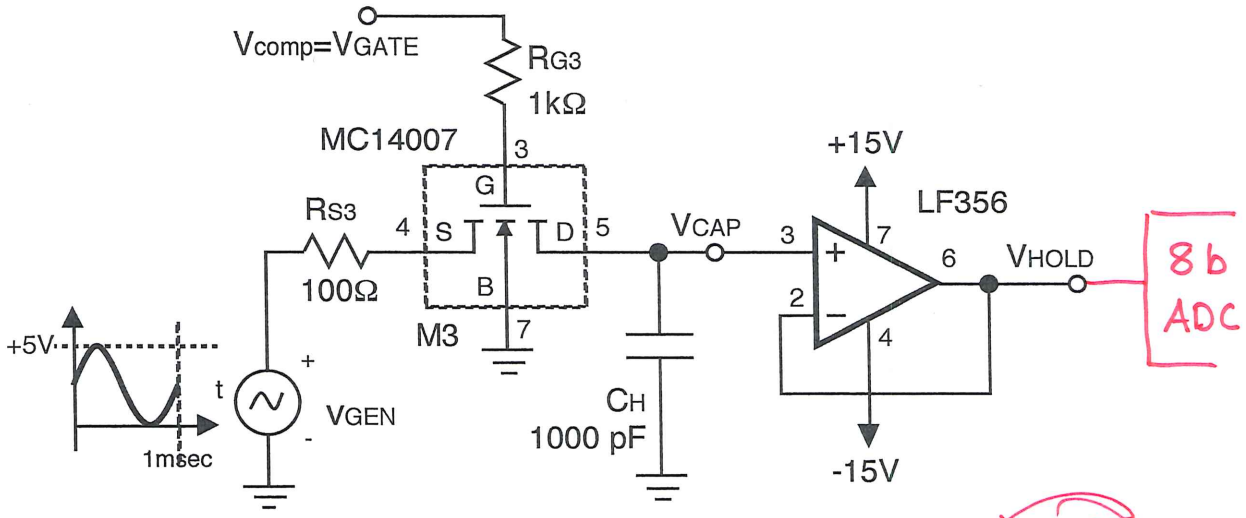


USE WORST CASE (LARGEST) Ron OVER SIGNAL RANGE




* lab4_p3_28k - Lab 4 sample-and-hold circuit
Date/Time run: 11/28/11 10:30:05
Temperature: 27.0
(Z) lab4_p3_acq (active)
15V
10V
5V
0V
V(vgate)
VGATE
HOLD
5.0V
2.5V
0V
V(vin) V(vcap)
VIN
VCAP
100mV
0V
SEL>>
-100mV
ZOOMED IN
5mV
tACQ
"CHARGE INJECTION"
ECE529C
40us
44us
48us
52us
56us
60us
64us
68us
72us
V(vin) V(vcap)
Time

Sample-and-Hold Analysis / Design Example



System parameters:

- ADC 8 bit resolution
- MOSFET "on" resistance 500Ω
- LF 356: f_T = 5MHz, SR = 12 V/μsec

SR FAST ENOUGH!

a) What is the acquisition time at V_{CAP} to within 1/2 LSB?
"Acquisition time": For worst-case step, how long after transitioning from hold to sample at time t=0 for voltage to settle within error band (1/2 LSB in this case) of ideal (t→∞) final value

b) Will the output at V_{HOLD} be slew rate limited?

c) Choose a new value of C_H for an acquisition time of 1μsec

Sample-and-Hold Analysis / Design Example

$1\ \text{LSB} = \frac{5\text{V}}{256} = 19.5\ \text{mV}$

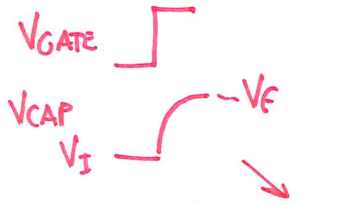
$\frac{1}{2}\ \text{LSB} = 9.8\ \text{mV}$

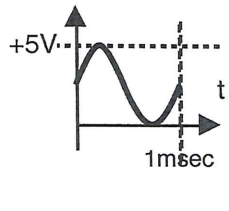
System parameters:

- ADC 8 bit resolution
- MOSFET "on" resistance 500Ω
- LF 356: f_T = 5MHz, SR = 12 V/μsec ✓

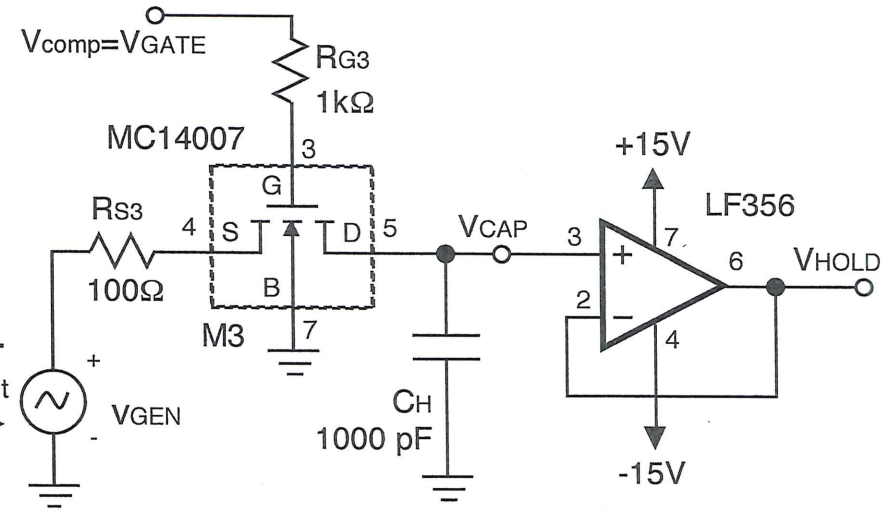
$2^8 = 256$ LEVELS

$\left.\frac{dV}{dt}\right|_{MAX} = 8.3\ \frac{\text{V}}{\mu\text{sec}} < \text{SR}$





5V ↑ ≡
↓ ≡



a) What is the acquisition time at V_{CAP} to within 1/2 LSB? 3.74μs

b) Will the output at V_{HOLD} be slew rate limited? NO!

a) GEN'L EXP

$V(t) = V_F - (V_F - V_I)e^{-t/\tau}$

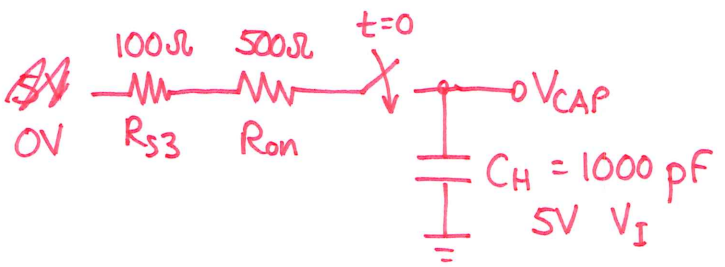
$V(t) = 5\text{V}\,e^{-t/\tau}$

AT $t = t_{ACQ}$

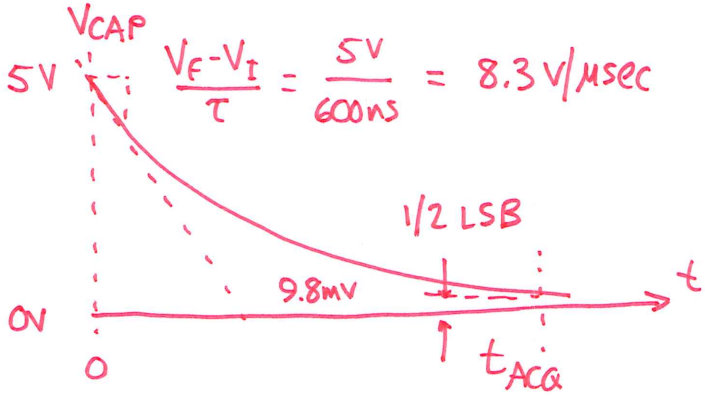
$9.8\text{mV} = 5\text{V}\,e^{-t_{ACQ}/\tau}$

$t_{ACQ} = \underbrace{\ln\left(\frac{5\text{V}}{9.8\text{mV}}\right)}_{6.24}\tau = (6.24)(600\text{nsec}) = 3.74\ \mu\text{sec}$

$\ln\left(\frac{2^8}{1/2}\right)$ FULL SCALE ERROR BAND



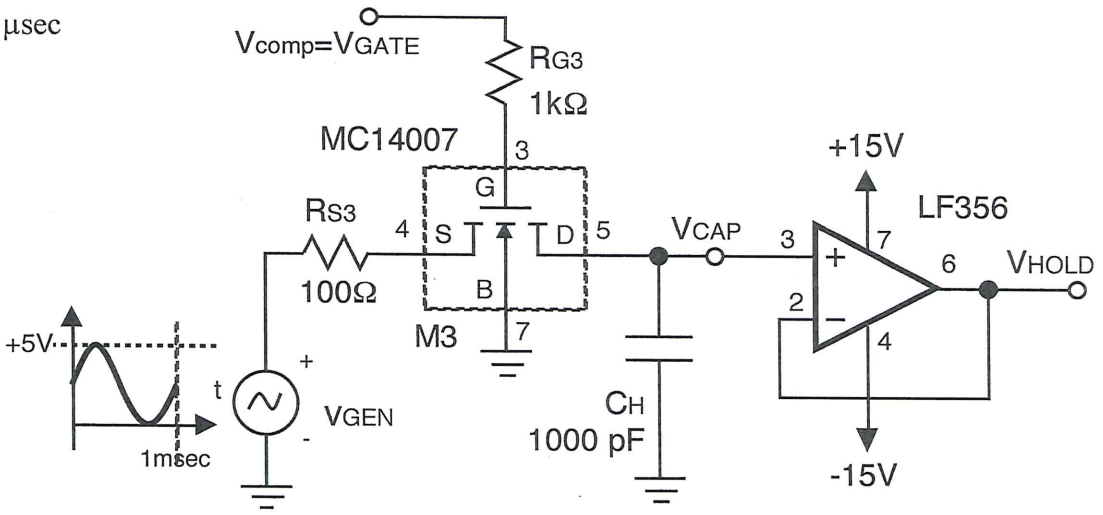
$\tau = (R_{S3} + R_{on})C_H = (600\Omega)(1000\text{pF}) = 600\text{ns}$



b) DOES $\left.\frac{dV_{CAP}}{dt}\right|_{MAX} > \text{SR}$? ON

$\frac{dV_{CAP}}{dt} = \frac{V_F - V_I}{\tau}e^{-t/\tau}$

c) Choose a new value of C_H for an acquisition time of 1µsec



½ LSB AT 8b level

$t_{ACQ} = 6.24\ \tau$

WANT ↓

$1\mu sec = 6.24\ \tau$

$\tau_{NEED} = \frac{1\mu sec}{6.24}$

$= 160\ nsec$

$(600\Omega)\ C_H$

NEED FOR C_H:

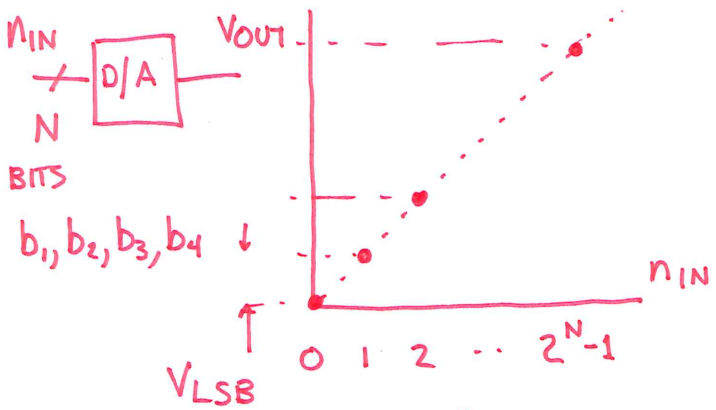
$160\ nsec = 600\Omega\ C_H$

$C_H = \frac{160\ nsec}{600\Omega} = 265\ pF$

SAME MODEL

D/A Converter (I)

WANT

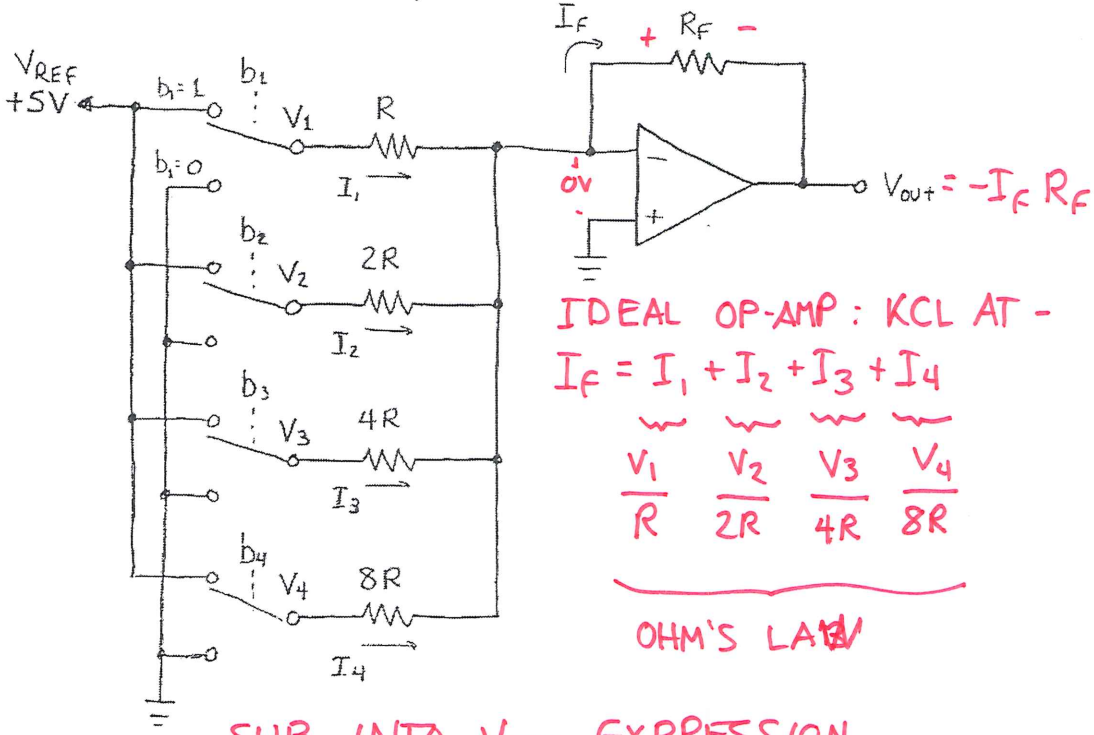


"LEAST SIGNIFICANT BIT"

DIGITAL WORD INPUT (4 BIT EXAMPLE)

MSB			LSB		
b_1	b_2	b_3	b_4	n_{IN}	
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
		:			
1	1	1	1	15	F

"BINARY WEIGHTED R"



IDEAL OP-AMP: KCL AT −

$I_F = I_1 + I_2 + I_3 + I_4$

$\frac{V_1}{R} \quad \frac{V_2}{2R} \quad \frac{V_3}{4R} \quad \frac{V_4}{8R}$

OHM'S LAW

SUB INTO V_{OUT} EXPRESSION

$$V_{OUT} = -\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \frac{V_4}{8R}\right) R_F$$

FACTOR OUT R, MULTIPLY 8/8

$$V_{OUT} = \frac{-R_F}{8R}\left(8V_1 + 4V_2 + 2V_3 + V_4\right)$$

USE $V_i = b_i V_{REF}$; FACTOR OUT V_{REF}

$$V_{OUT} = \underbrace{\left[\frac{-R_F}{8R} V_{REF}\right]}_{V_{LSB}\text{ STEP SIZE}} \underbrace{\left(8b_1 + 4b_2 + 2b_3 + b_4\right)}_{\text{BINARY NUMBER!}}$$