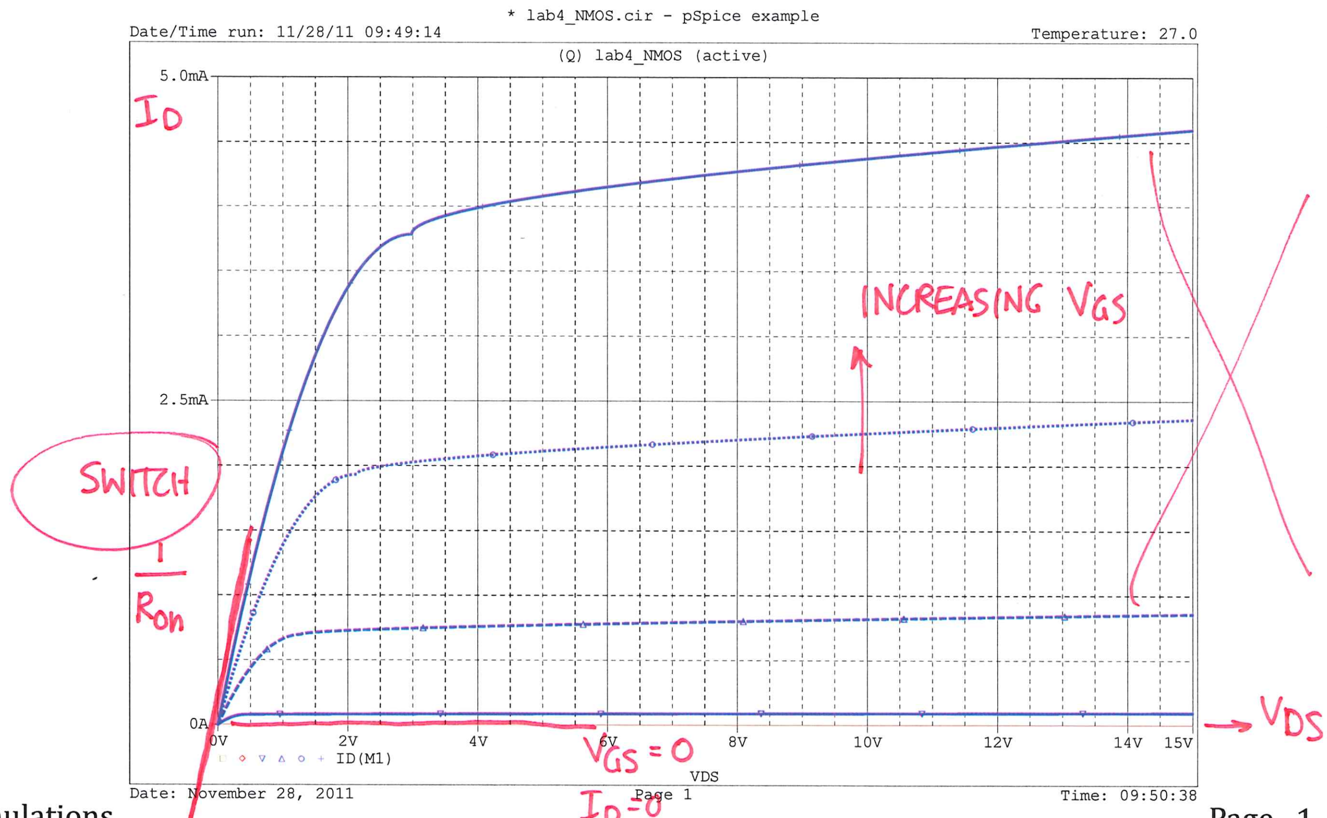
```
* lab4 NMOS.cir - pSpice example
* Show V-I characteristics for MOSFETs

* N-channel MOSFET
M1       vd     vg     0    0    MC14007N

* VGS
VGS      vg     0               DC 5

* VDS
VDS      vd     0               DC 5


* MOSFET models (See ECE4902 for meaning of parameters)
.model   MC14007N  NMOS   LEVEL=3   W=350u L=10u VTO= 1.5  UO=600  TOX=1E-7  NSUB=1E+15
.model   MC14007P  PMOS   LEVEL=3   W=900u L=10u VTO=-1.5  UO=200  TOX=1E-7  NSUB=3E+15


* DC Analysis
* Sweep VDS at each value of VGS
.dc      VDS    0    15    0.01

* Different values of VGS
.STEP    VGS    0     5    1

* Write .dat file for use by probe
.probe
```

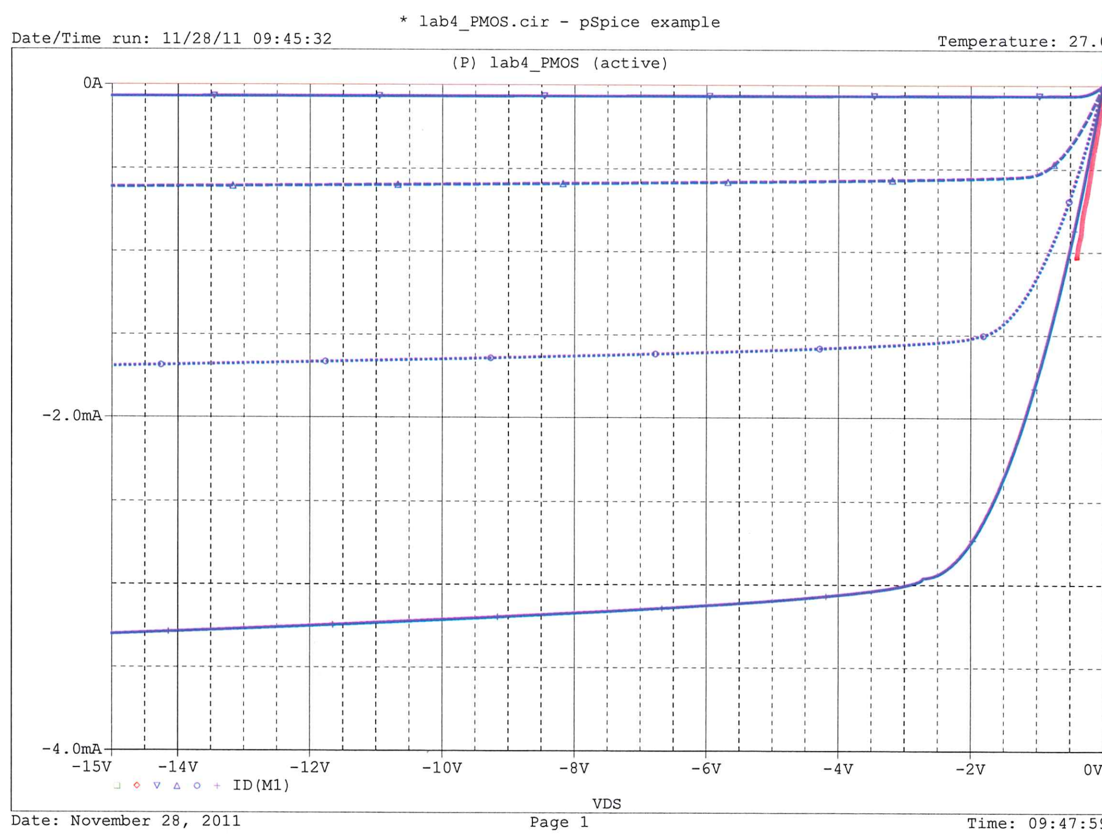
NMOS



```
* lab4 PMOS.cir - pSpice example
* Show V-I characteristics for MOSFETs

* P-channel MOSFET
M1       vd     vg     0    0    MC14007P

* VGS
VGS      vg     0               DC -5

* VDS
VDS      vd     0               DC -5


* MOSFET models (See ECE4902 for meaning of parameters)
.model   MC14007N  NMOS   LEVEL=3   W=350u L=10u VTO= 1.5  UO=600  TOX=1E-7  NSUB=1E+15
.model   MC14007P  PMOS   LEVEL=3   W=900u L=10u VTO=-1.5  UO=200  TOX=1E-7  NSUB=3E+15

* DC Analysis
* Sweep VDS at each value of VGS
.dc      VDS    0    -15    -0.01

* Different values of VGS
.STEP    VGS    0     -5    -1

* Write .dat file for use by probe
.probe
```

PMOS

$\frac{1}{R_{on}}$



M:\Courses\ece3204\3204_pspice\lab4_p2_CMOS_inverter.cir

```
* lab4_p2_CMOS_inverter.cir - pSpice example

* P-channel MOSFET
M1      vcomp   vclk  14   14    MC14007P

* N-channel MOSFET
M2      vcomp   vclk   0    0    MC14007N

* Load capacitance (model scope, breadboard parasitics)
CL      vcomp   0                30pF

* Voltage source at input
* DC value for sweep of inverter DC characteristic
* PULSE for square wave response in TRANsient analysis
VIN     vclk    0    DC   0      PULSE (0  15  1u  10n  10n  10u  20u )

* Power supply
VDD     14      0    DC   +15

* MOSFET models (See ECE4902 for meaning of parameters)
.model  MC14007N  NMOS  LEVEL=3  W=350u L=10u VTO= 1.5  UO=600  TOX=1E-7  NSUB=1E+15
.model  MC14007P  PMOS  LEVEL=3  W=900u L=10u VTO=-1.5  UO=200  TOX=1E-7  NSUB=3E+15


* DC Analysis
* Sweep VIN over 15V range
.dc     VIN   0   15   0.01

* TRANsient simulation
* Start at t=0, force 100nsec time step
.tran  100n   200u   0    100n


* Write .dat file for use by probe
.probe
```

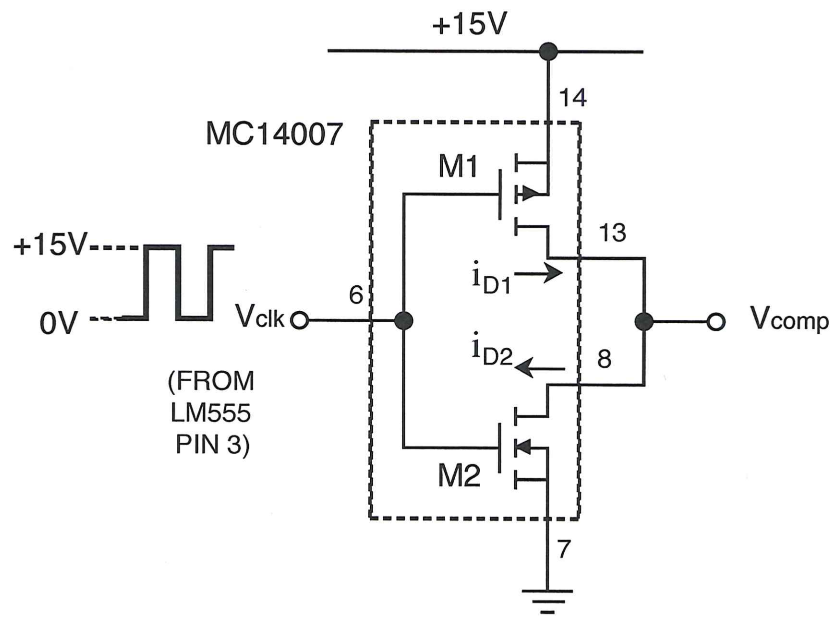
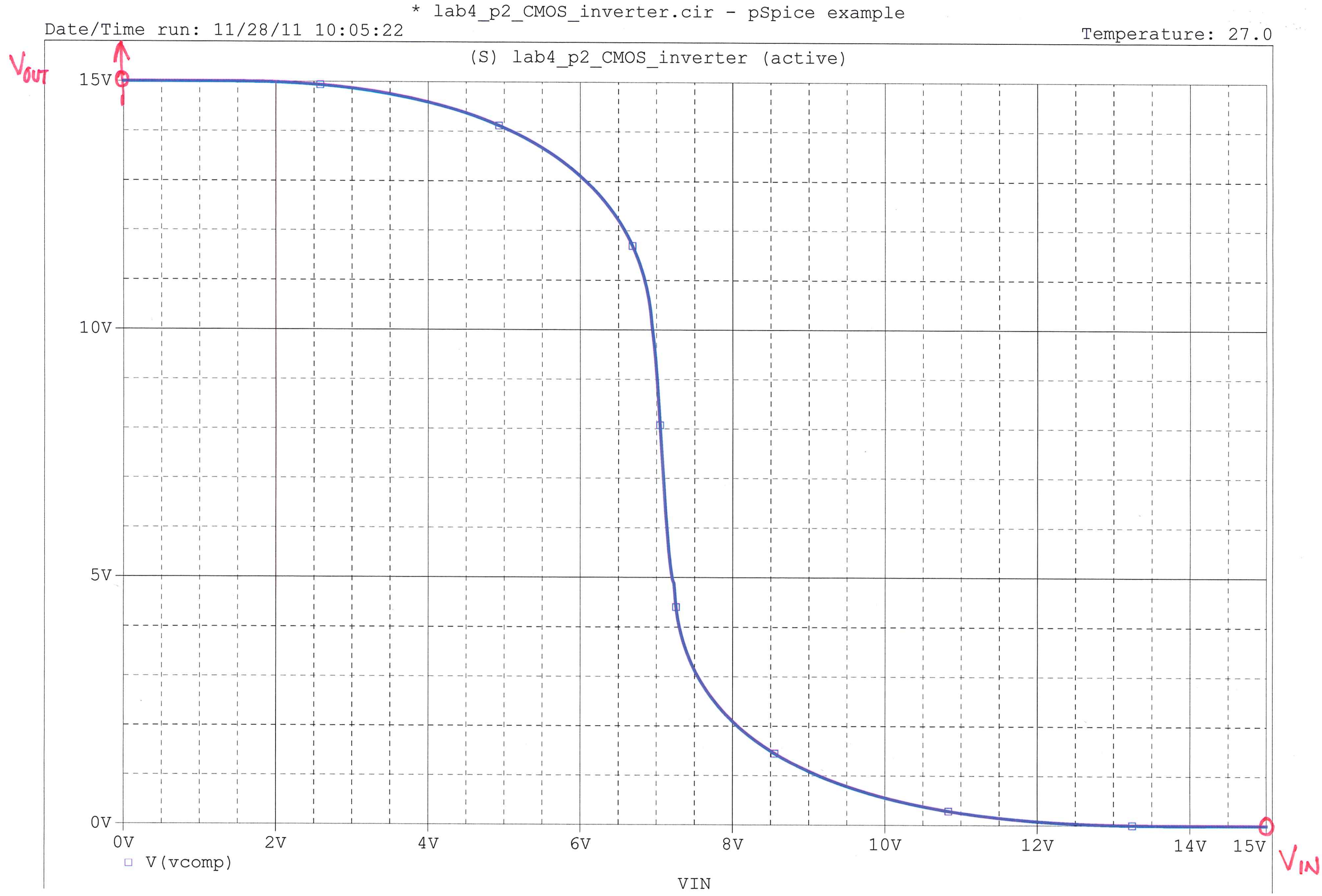


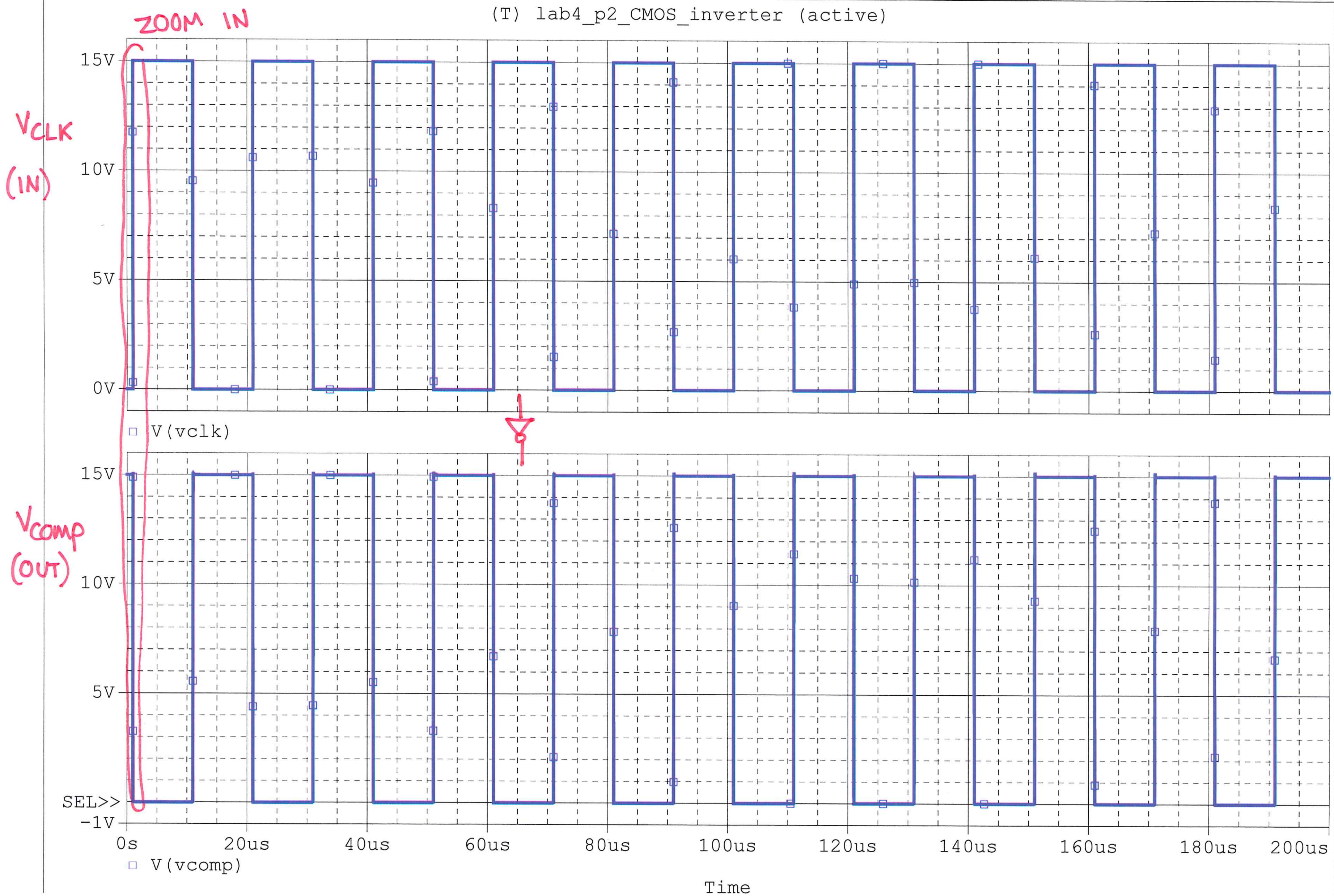
Figure 4.2

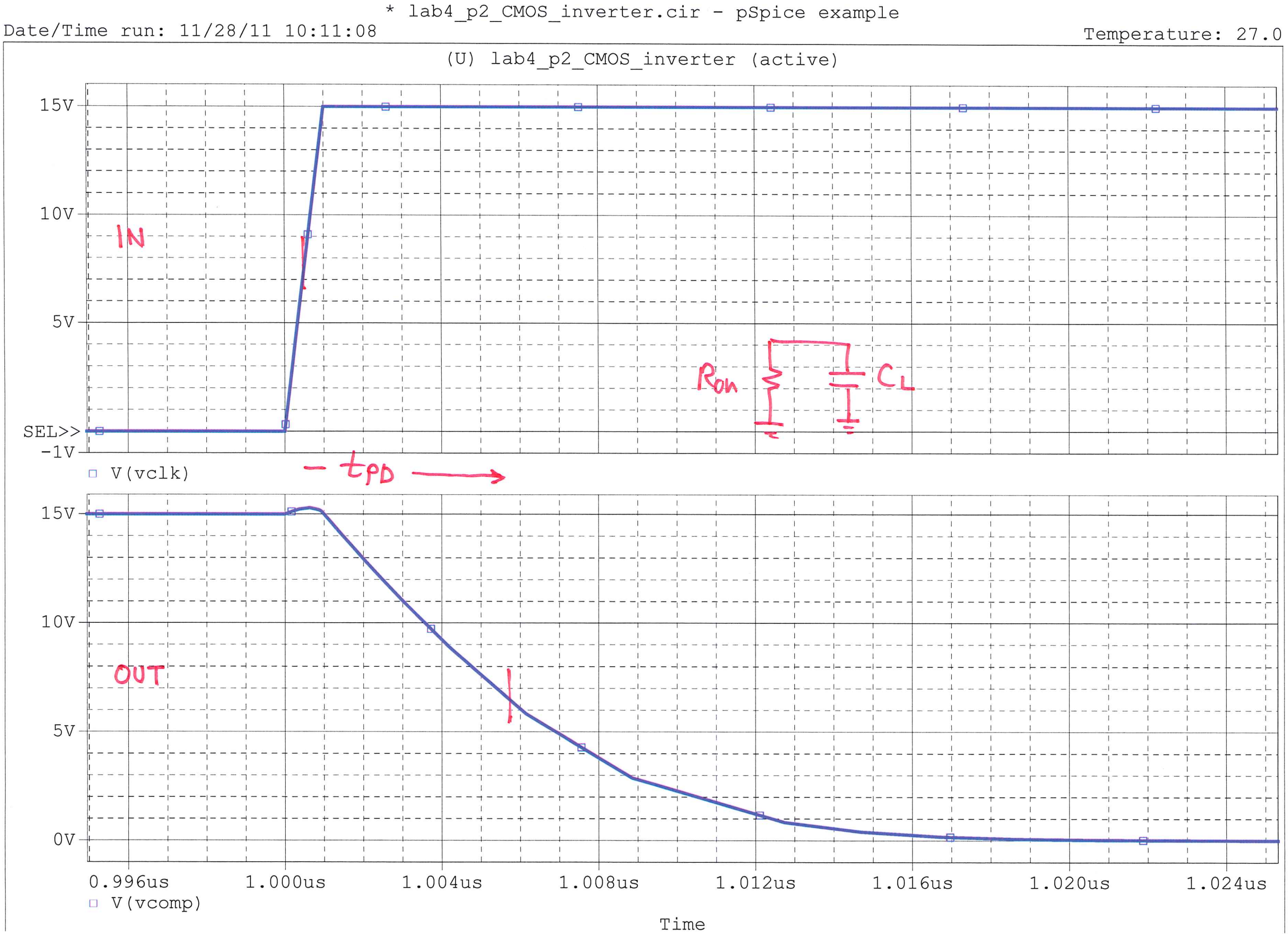

* lab4_p2_CMOS_inverter.cir - pSpice example
Date/Time run: 11/28/11 10:05:22
Temperature: 27.0
(S) lab4_p2_CMOS_inverter (active)
VOUT
15V
10V
5V
0V
0V
2V
4V
6V
8V
10V
12V
14V
15V
VIN
V(vcomp)
VIN

* lab4_p2_CMOS_inverter.cir - pSpice example

Date/Time run: 11/28/11 10:05:22

Temperature: 27.0




* lab4_p2_CMOS_inverter.cir - pSpice example
Date/Time run: 11/28/11 10:11:08
Temperature: 27.0
(U) lab4_p2_CMOS_inverter (active)
15V
10V
5V
SEL>>
-1V
IN
R_{on}
C_L
V(vclk)
t_{PD}
15V
10V
5V
0V
OUT
0.996us
1.000us
1.004us
1.008us
1.012us
1.016us
1.020us
1.024us
V(vcomp)
Time

```
* lab4 p3 28k - Lab 4 sample-and-hold circuit
* 28kHz sine wave input

* Voltage source at input
Vcomp    vgate    0    PULSE (15   0   1u   10n   10n   10u   20u )

* Series protection resistor for gate
Rg3      vgate    3    1K

* MOSFET
M3       vcap   3    4    0   MC14007N

* "Hold" capacitor
CH       vcap    0     1000pF

* Input signal source 28kHz
Vgen     vin     0      SIN (2.5   2.5   28kHz   0   0   0)

* Series protection resistor for input
Rs3      vin    4      100

* MOSFET models
.model   MC14007N   NMOS   LEVEL=3   W=350u L=10u VTO= 1.5   UO=600   TOX=1E-7   NSUB=1E+15
.model   MC14007P   PMOS   LEVEL=3   W=900u L=10u VTO=-1.5   UO=200   TOX=1E-7   NSUB=3E+15


* TRANsient simulation
* Start at t=0, force 100nsec time step
.tran  100n   200u   0    100n

* Write .dat file for use by probe
.probe
```

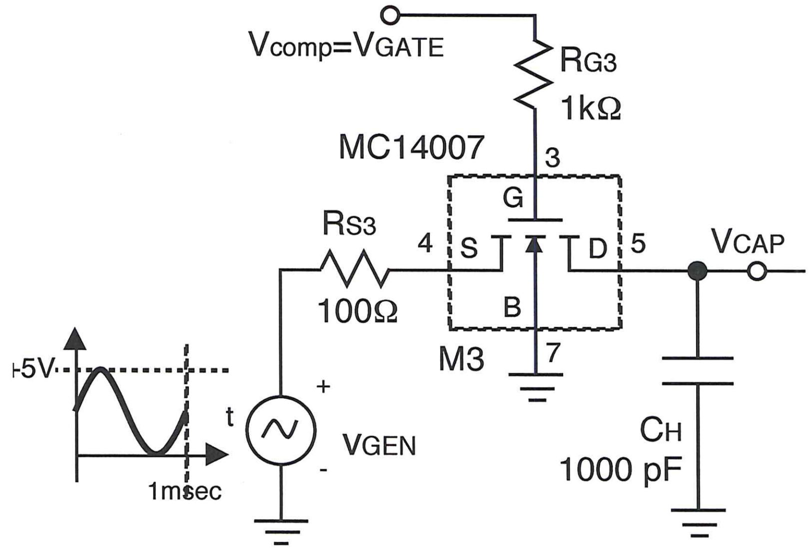
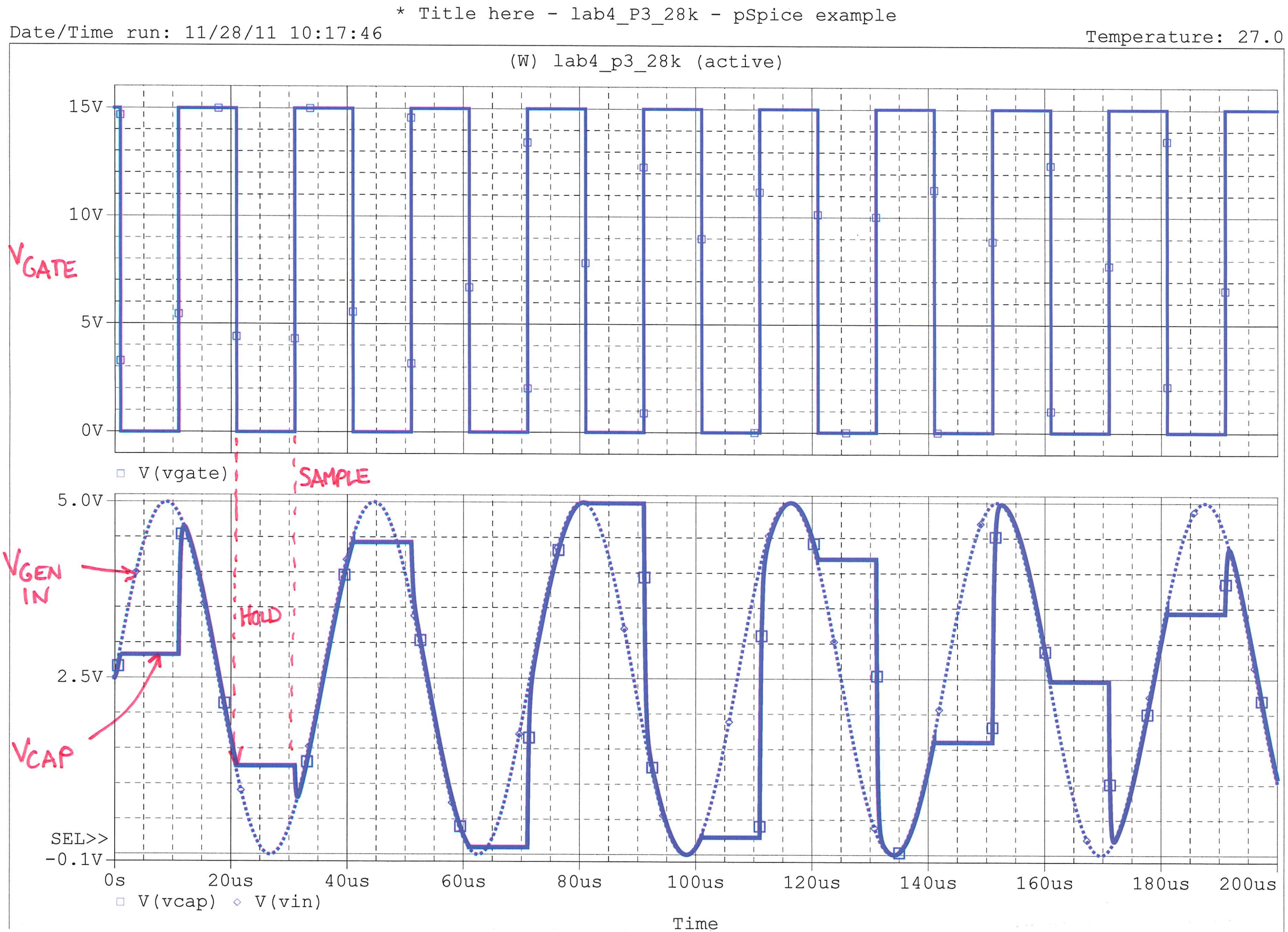
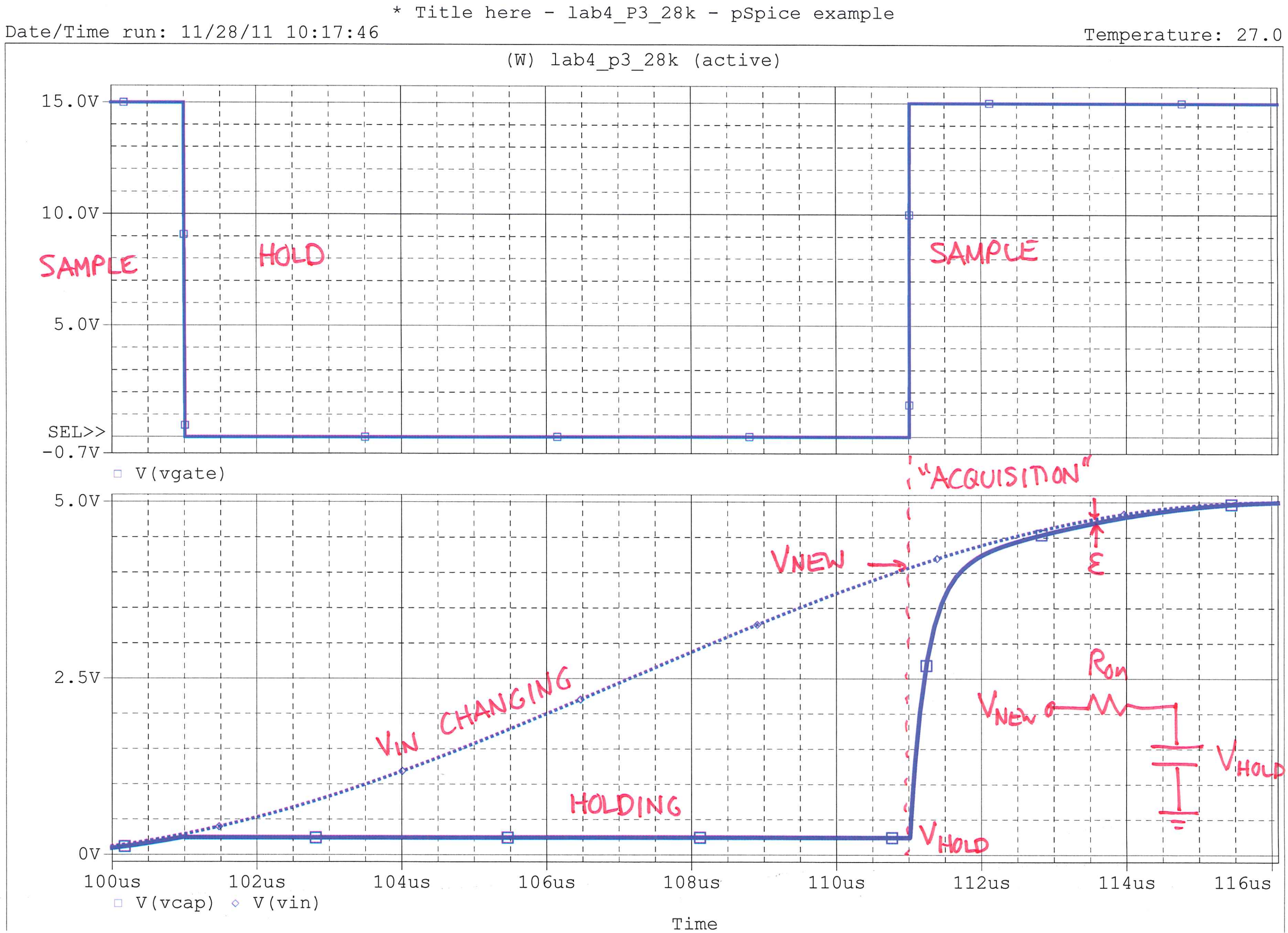


Figure 4.3



* Title here - lab4_P3_28k - pSpice example
Date/Time run: 11/28/11 10:17:46
Temperature: 27.0
(W) lab4_p3_28k (active)
15V
10V
5V
0V
V(vgate)
VGATE
SAMPLE
HOLD
VGEN IN
VCAP
5.0V
2.5V
SEL>>
-0.1V
0s
20us
40us
60us
80us
100us
120us
140us
160us
180us
200us
V(vcap)
V(vin)
Time


* Title here - lab4_P3_28k - pSpice example
Date/Time run: 11/28/11 10:17:46
Temperature: 27.0
(W) lab4_p3_28k (active)
15.0V
10.0V
5.0V
SEL>>
-0.7V
V(vgate)
SAMPLE
HOLD
SAMPLE
"ACQUISITION"
5.0V
2.5V
0V
VNEW
ε
Ron
VNEW
VHOLD
VIN CHANGING
HOLDING
VHOLD
100us
102us
104us
106us
108us
110us
112us
114us
116us
V(vcap)
V(vin)
Time