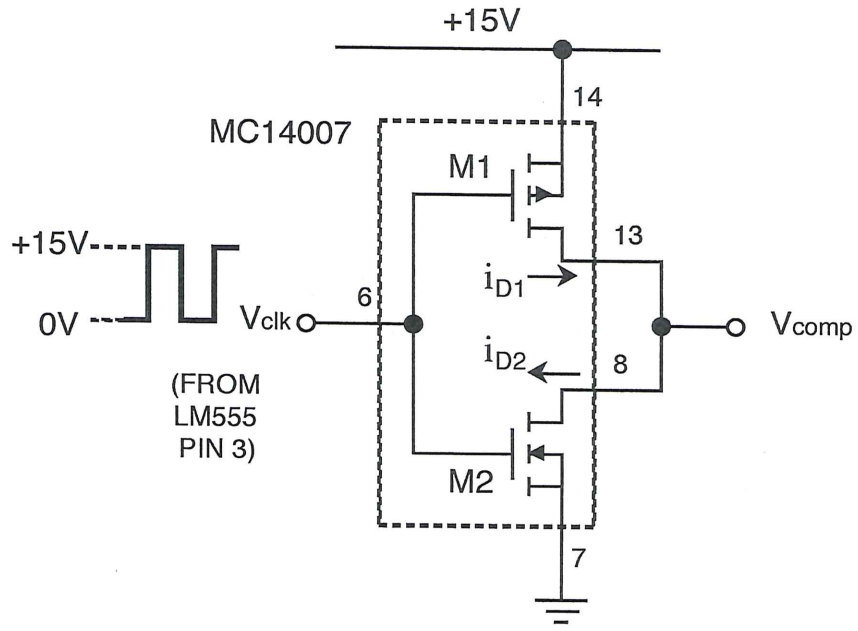
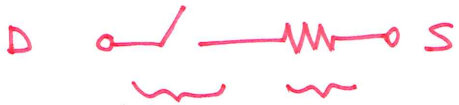
P2. CMOS Inverter

Lab 4 Circuits
CMOS Inverter
MOSFET Switch (13.1)
Sample-and-Hold
Analog Multiplexer



MOSFET MODEL:



STATE CONTROLLED BY V_{GS} RELATIVE TO THRESHOLD VOLTAGE V_{TH}

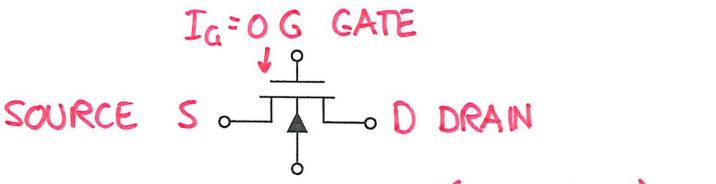
R_{on} "ON RESISTANCE"

$|V_{GS}| \uparrow \Rightarrow R_{on} \downarrow$

MOSFET Review

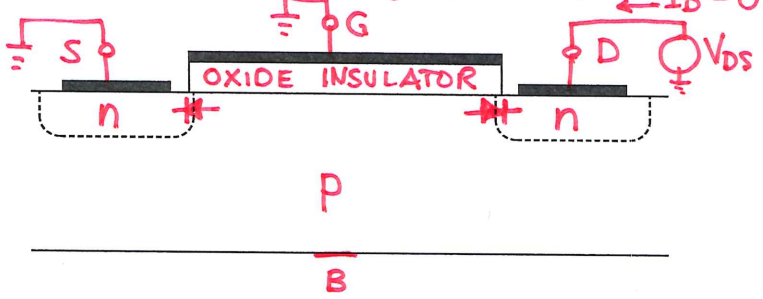
N-CHANNEL (NMOS)

CIRCUIT SYMBOL

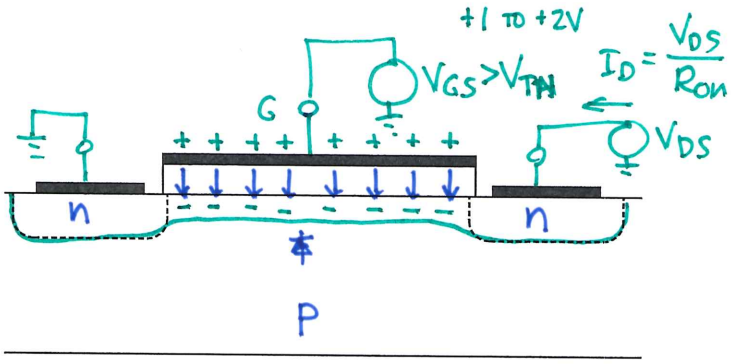


$V_{GS} = 0$ OFF

BACK-TO-BACK DIODES IN D-S PATH!



NMOS $V_{GS} > V_{TH}$ ON



E FIELD ATTRACTS e^-

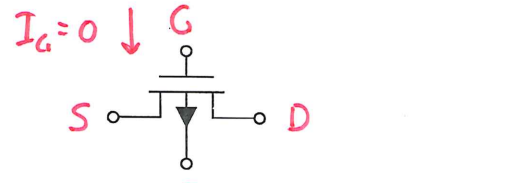
CONTINUOUS n-TYPE S → D

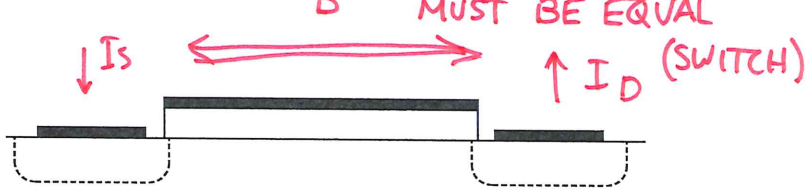
S —/\/\/— D

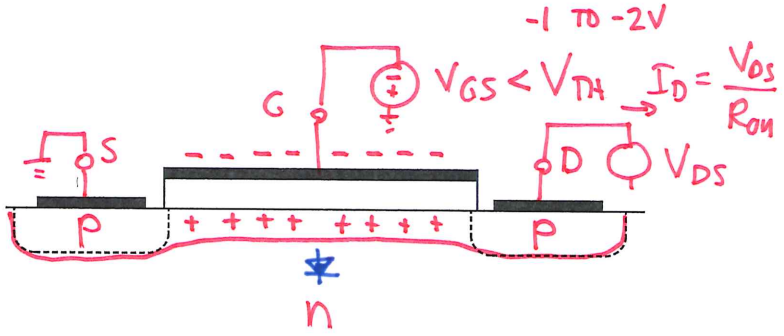
"R_{on}"

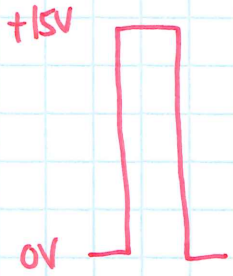
B TO MOST − VOLTAGE ← $I_B = 0$ KEEP S-B, D-B JUNCTIONS REVERSE BIASED → B TO MOST + VOLTAGE

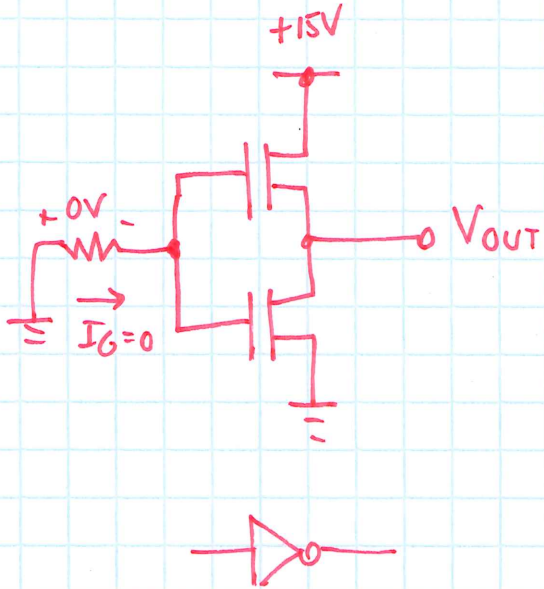
P-CHANNEL (PMOS)

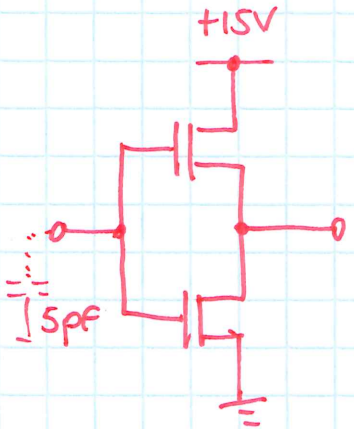




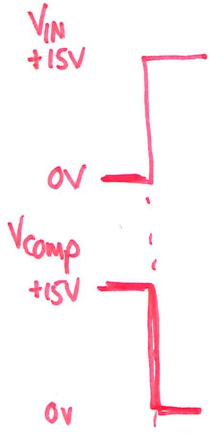


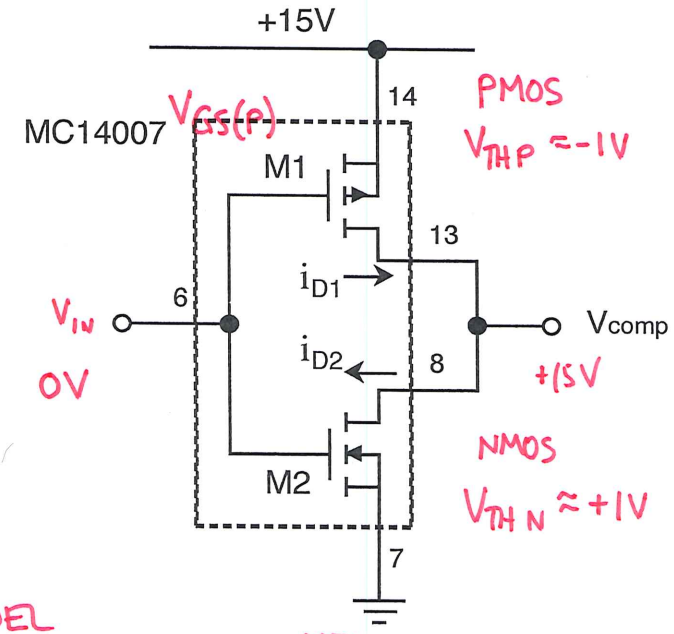

+15V
0V


+15V
+0V -
$I_G = 0$
V_{OUT}


+15V
5pf

CMOS Inverter





$V_{GS(P)}$

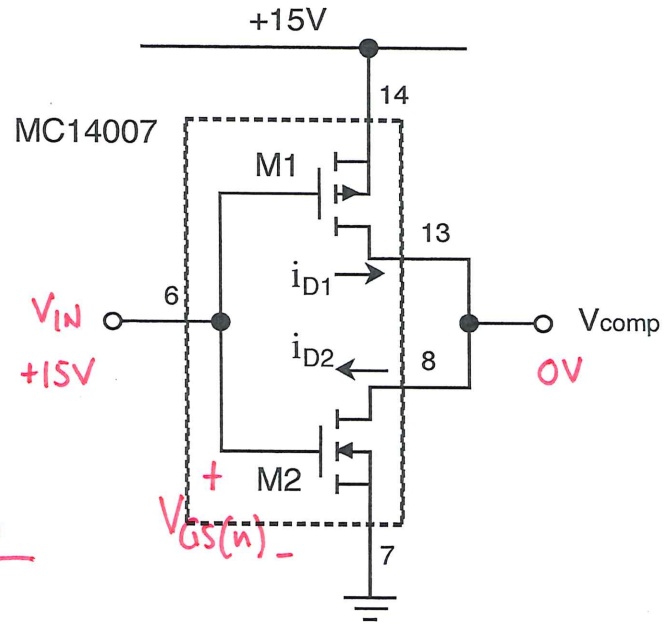
PMOS

$V_{THP} \approx -1V$

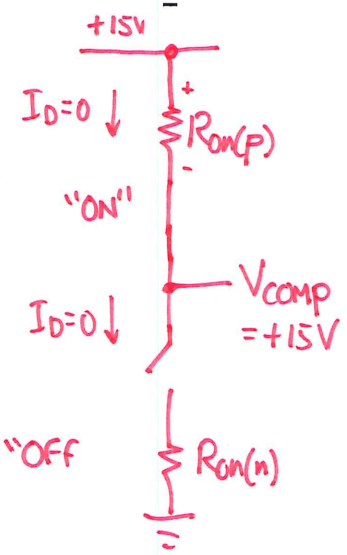
NMOS

$V_{TH\,N} \approx +1V$

V_{IN}	V_{comp}
0V	+15V
+15V	0V



MODEL

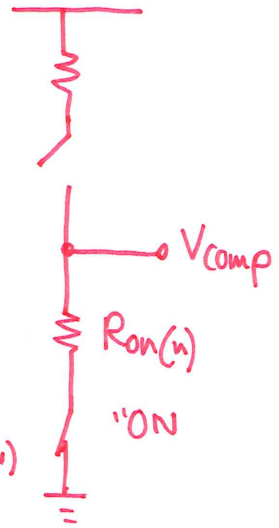


$V_{GS(P)} = 0 - (+15)$ $V_{TH(P)}$

$= -15V << -1V$

$V_{GS(N)} = 0-0 = 0V$

$< V_{TH(N)}$



$V_{GS(P)} = 0$

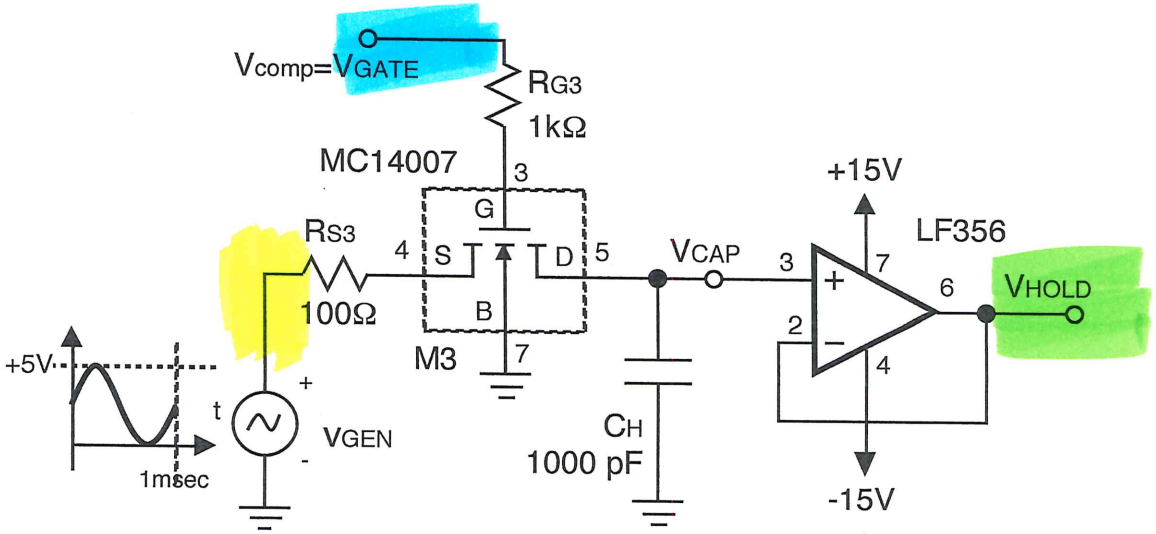
OFF

$V_{GS(N)} = +15V - 0$

$= +15V > V_{TH(N)}$

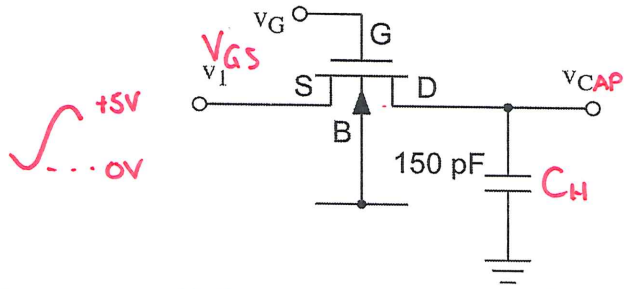
P3. Sample-and-hold

The sample and hold circuit of Figure 4.3 uses one of the MC14007 N-channel MOSFETs as analog switch M3. Note that V_{GEN} is a 1kHz, 5V peak-to-peak sine wave with a +2.5V DC offset: the voltage swings from 0V to +5V. Resistors R_{G3} and R_{S3} are for protection of the analog switch.



Sample-and-Hold Development

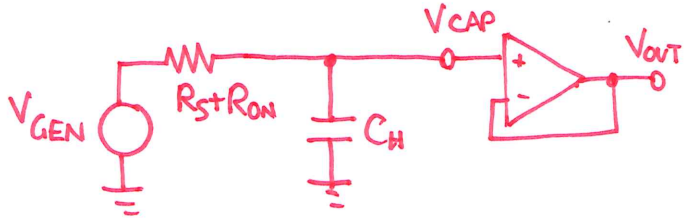
$V_G = +15V$ "SAMPLE" MODE



$V_{GS(MIN)} = +10V$ $V_{GS(MAX)} = +15V$

ALWAYS $> V_{TH(N)}$: NMOS "ON"

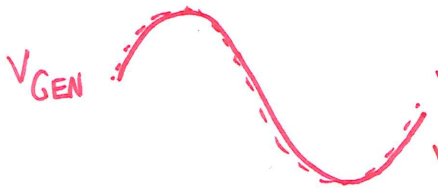
EQUIVALENT CIRCUIT



LOWPASS FILTER

CHOOSE C_H, R_{on} : $f_{3dB} = \frac{1}{2\pi R_{TOTAL} C_H}$

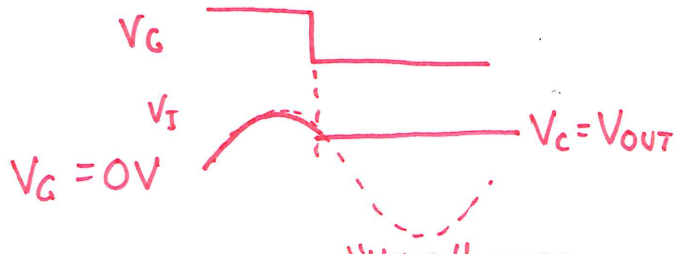
$\gg f_{MAX}$ OF INPUT



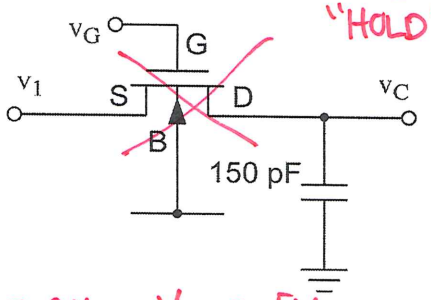
$V_{CAP} \approx V_{GEN}$

V_{CAP} TRACKS V_{GEN}

V_{CAP} SAMPLES V_{GEN}



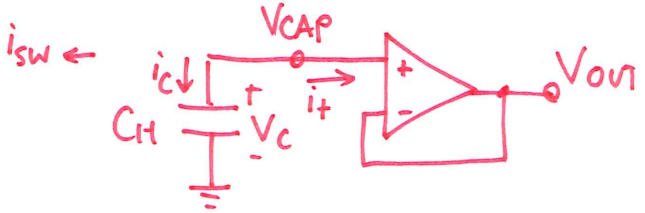
"HOLD" MODE



$V_{GS} = 0V$ $V_{GS} = -5V$

ALWAYS $< V_{TH(N)}$: NMOS OFF

EQUIVALENT CIRCUIT



KCL FOR CAP:

$0 \leftarrow i_{SW} + i_+ + i_C = 0 \rightarrow i_C = 0$ (0)

$i_C = C\frac{dV_C}{dt}$ CHANGE IN C_H VOLTAGE IS ZERO

$\neq 0$ $\neq 0$ 0

C_H WILL HOLD WHATEVER VOLTAGE IT HAD WHEN NMOS TURNED OFF