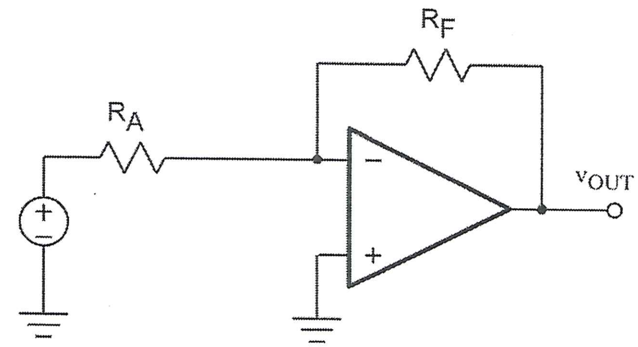
ECE3204 Lecture 8

Finish Op-Amp Design Example



Handouts:
DC Errors: Offset Voltage, Bias Current
Slew Rate Limiting

GRAPHICAL REPRESENTATION

$$\frac{V_{out}}{V_{in}} = \frac{-100}{1 + j\left(\frac{f}{9.9kHz}\right)} \qquad \frac{NUM}{DEN}$$

$$\text{DC GAIN} = -100$$

$$\left|\frac{V_{out}}{V_{in}}\right|_{DC} = 100$$

$$20\log(100) = +40\,dB$$

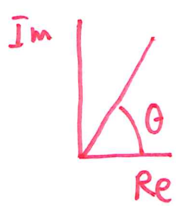
UNITY GAIN

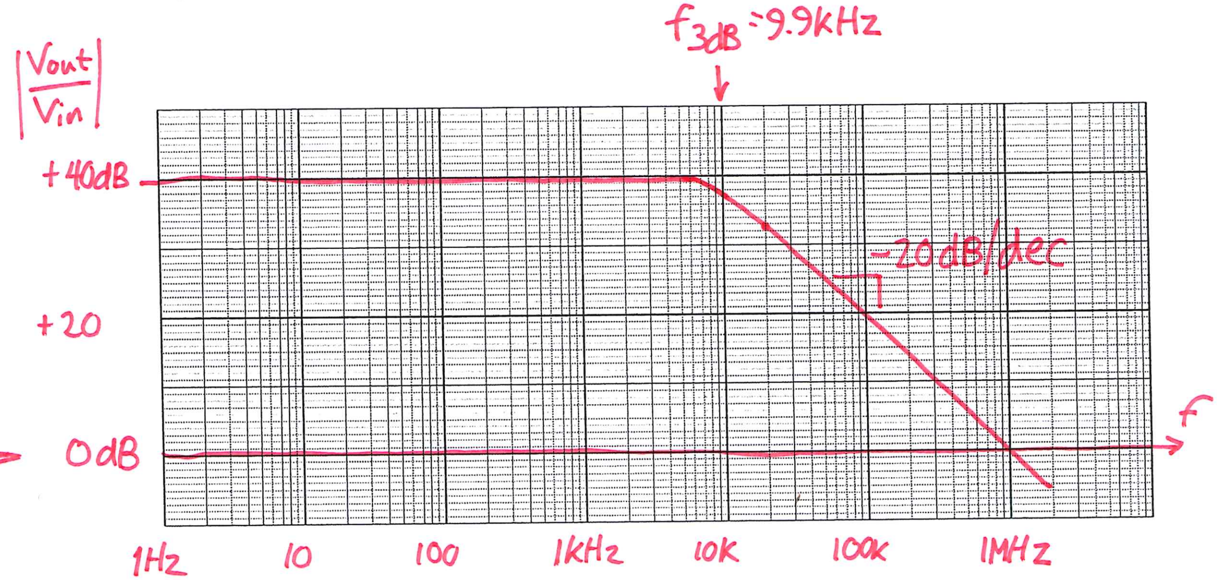
$$20\log(1) = 0\,dB$$

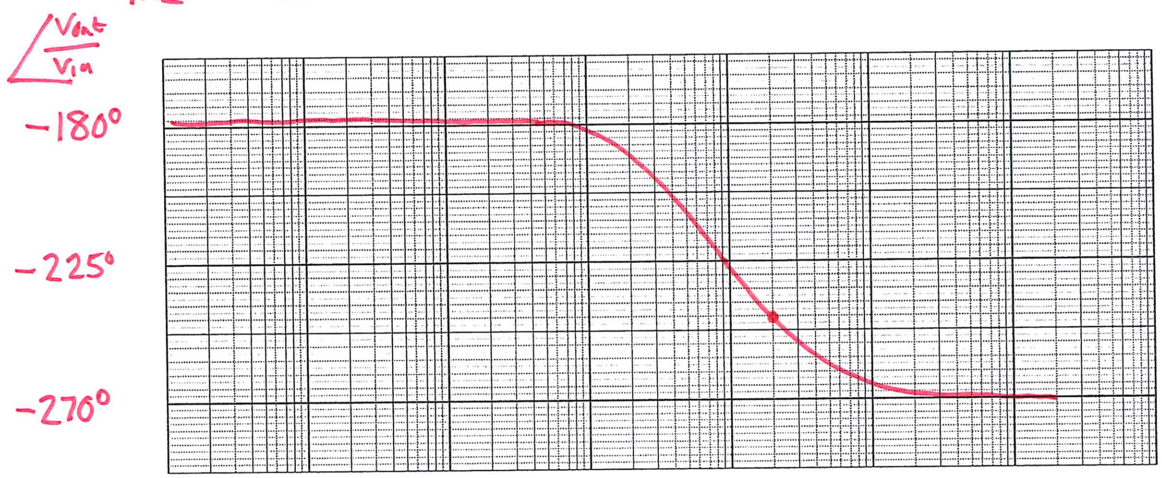
$$\angle\frac{V_{out}}{V_{in}} = \angle NUM - \angle DEN$$

$$\underbrace{-180^\circ}_{\substack{\text{FROM} \\ -\text{ SIGN}}} - \underbrace{\tan^{-1}\left(\frac{f}{9.9kHz}\right)}$$

$$\angle x + jy = \tan^{-1}\left(\frac{y}{x}\right) \quad \frac{Im}{Re}$$

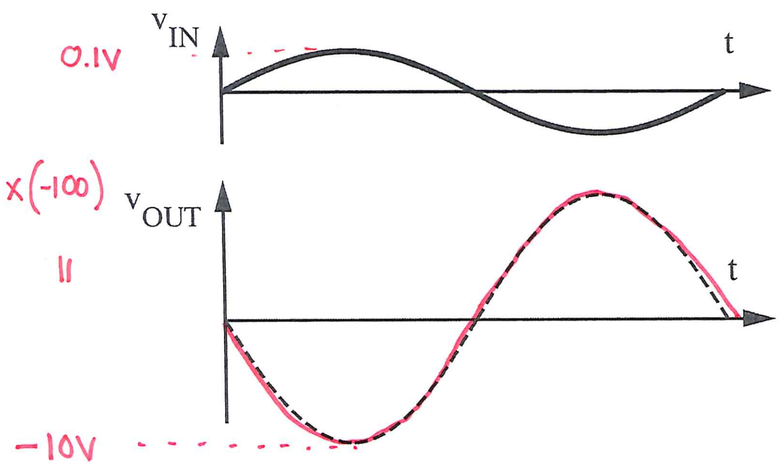






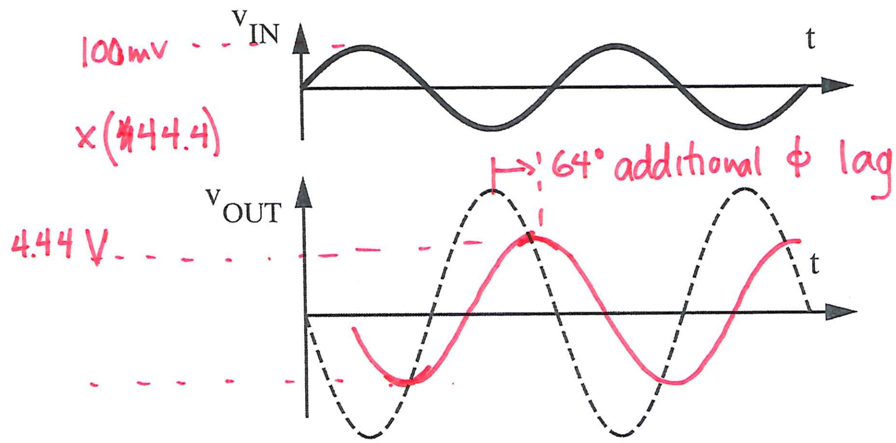
d) Determine $v_{OUT}(t)$ for an input sine wave of (100mV)sin(2π[100Hz]t)

WELL BELOW f_{3dB}
FULL GAIN -100



e) Determine $v_{OUT}(t)$ for an input sine wave at the upper edge of the audio frequency range (100mV)sin(2π[20kHz]t)

BODE PLOT: 20kHz > f_{3dB}



GAIN ≈ 33dB? PHASE ~ -240°? } FROM BODE PLOT

USE TRANSFER FUNCTION

$$\left|\frac{V_{out}}{V_{in}}\right|_{f=20kHz} = \left|\frac{-100}{1+j\left(\frac{20kHz}{9.9kHz}\right)}\right| = \frac{100}{\sqrt{1^2+\left(\frac{20kHz}{9.9kHz}\right)^2}} = 44.4$$

$$20\log_{10}(44.4) = 32.9\text{ dB}$$

PHASE

$$\angle\frac{V_{out}}{V_{in}}\Big|_{f=20kHz} = \angle\frac{-100}{1+j\left(\frac{20kHz}{9.9kHz}\right)} = -180^\circ - \underbrace{\tan^{-1}\left(\frac{20kHz}{9.9kHz}\right)}_{64^\circ}$$

f) If we want a closed loop 3-dB frequency (bandwidth) f_{3dB} = 20kHz for an audio application, determine the op-amp unity gain frequency f_T required

GBWP RELATIONSHIP

$$\underbrace{\left(\frac{1}{101}\right)}_{\beta} f_T = 20 \text{ kHz}$$

$$f_T = (20 \text{ kHz})\, 101 = 2.02 \text{ MHz} \quad > f_T \text{ } \cancel{\text{LM741}}$$

What about f_T (unity gain bandwidth) variability?

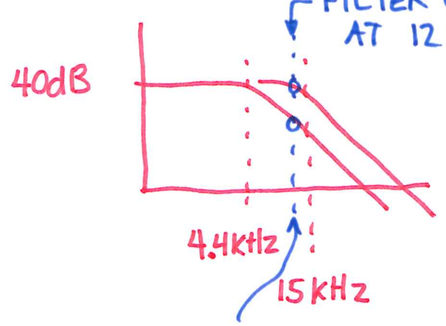
Electrical Characteristics (Note 5) (Continued)											
Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth (Note 6)	$T_A = 25°C$	0.437	1.5	?							MHz

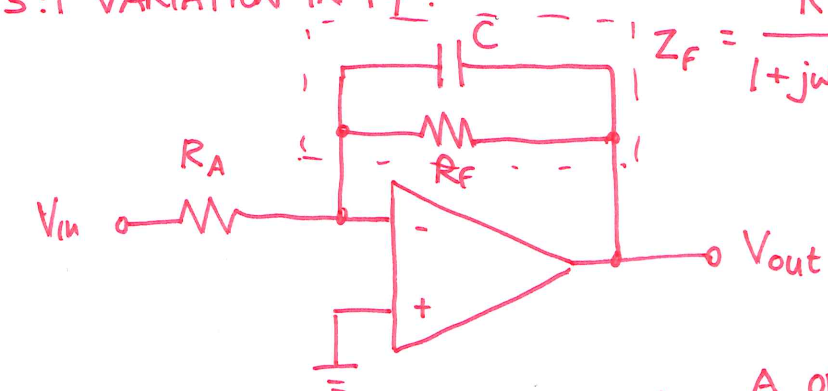
LM741

440 kHz 1.5 MHz

If you need to depend on closed loop f_{3dB}, get it from (better controlled) passive element values

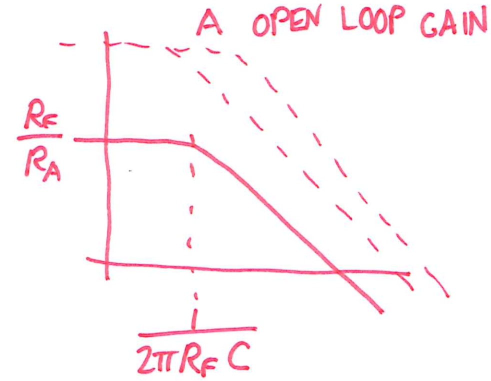
3:1 VARIATION IN f_T!





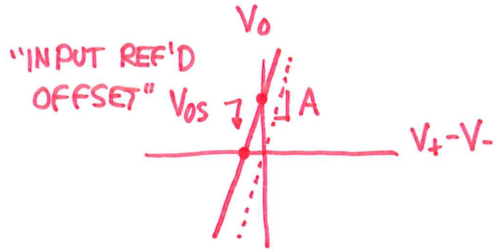
$$Z_F = \frac{R_F}{1 + j\omega R_F C}$$

$$\frac{V_{out}}{V_{in}} = \frac{-Z_F}{R_A} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{\left(\frac{-R_F}{R_A}\right)}{1 + j\omega R_F C}$$



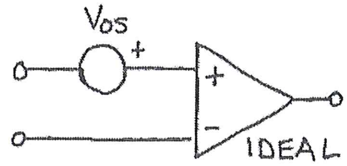
EE3204

DC ERRORS

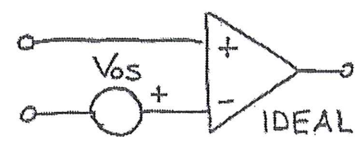


OFFSET VOLTAGE

Model as a source in series with either input of an ideal op-amp:



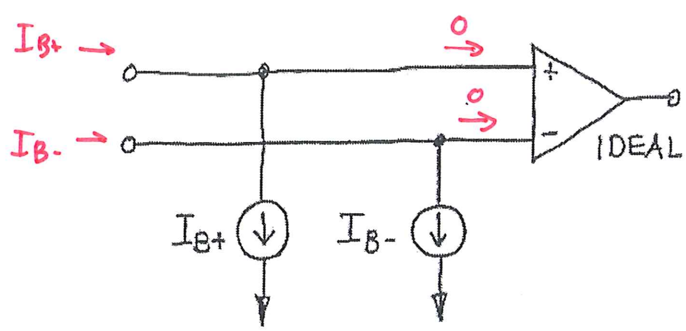
OR



V_{OS} can be of either + or − sign

BIAS CURRENT

Model as a current source in parallel with each input of an ideal op-amp:

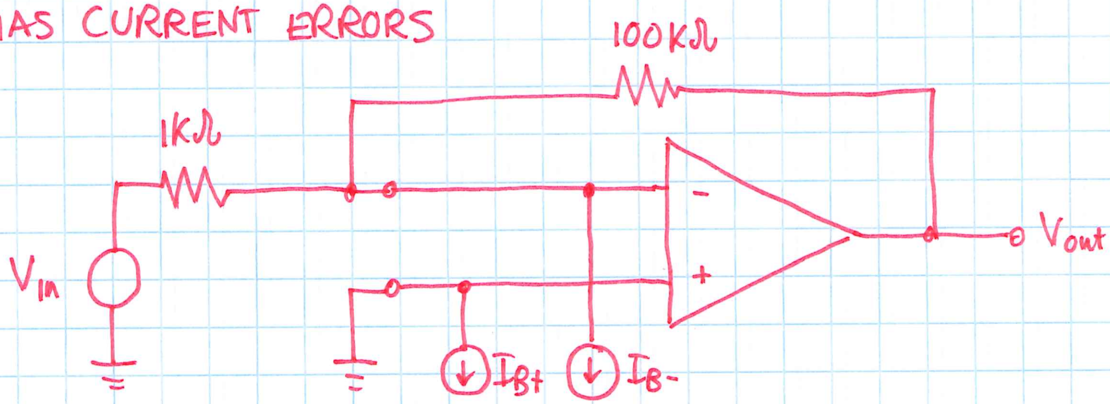


Polarity of I_B is usually known (depends on type of transistors in op-amp input stage)

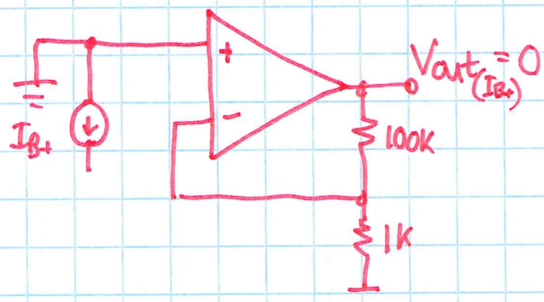
ANALYSIS

Use superposition and ideal op-amp assumptions to simplify analysis.

BIAS CURRENT ERRORS



BY SUPERPOSITION: I_{B+}

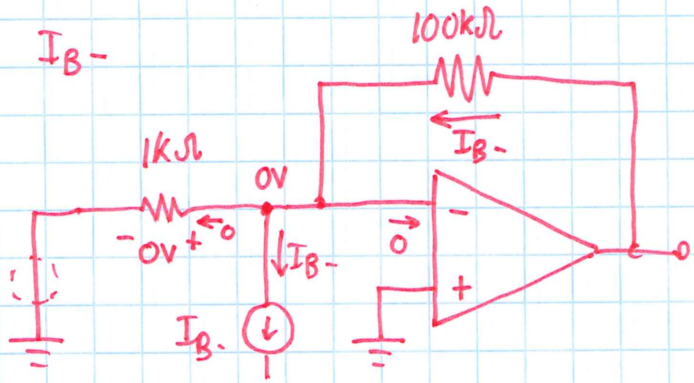


I_{B-}

LM741

UP TO 1.5 μA

↓



$V_{out}(I_{B-}) = I_{B-}(100K\Omega)$

V_- VIRTUAL GROUND: 0V FORCES $I = 0$ IN 1KΩ

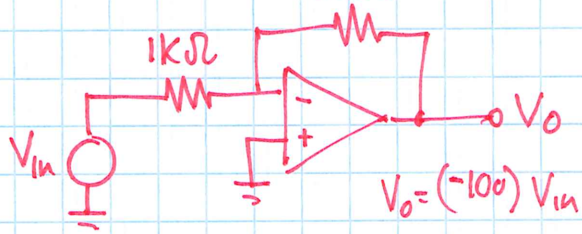
ALL OF I_{B-} FLOWS IN 100KΩ

$V_{OUT}(I_{B-}) = 150\,mV$

PROBLEM WITH LARGE RESISTANCE VALUES

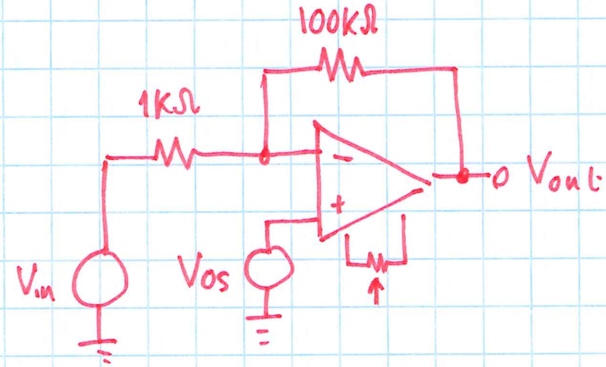
- FET INPUT; pA

OFFSET ERROR OF GAIN = −100 AMPLIFIER

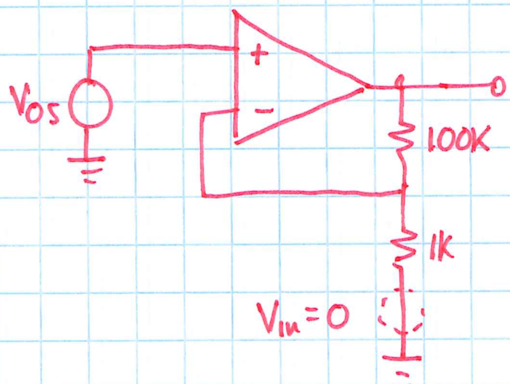


$V_o = (-100)\, V_{in}$

PUT IN SERIES WITH + INPUT →



SUPERPOSITION & REDRAW:



$V_{out}(V_{os}) = 101\, V_{os}$

TOTAL OUTPUT
(ADD BY SUPERPOSITION)

$$V_{out} = (-100)\, V_{in} + \underbrace{(101)\, V_{os}}_{\text{OFFSET}}$$

$V_{os} = \pm 7.5\,mV$

$\pm 758\ mV$

TENDS TO BE PROBLEM IN CIRCUITS WITH HIGH DC GAIN

- BETTER OP-AMP
- ADJUST / CALIBRATE
- DON'T DO HIGH DC GAIN IF NOT NEEDED