# ECE3204 D2015 Lab 6

**Stability: Differentiator**
**Stability: Wien Bridge Oscillator**
**Automatic Gain Control (AGC)**

## Objective

The purpose of this lab is to understand the role of phase in transfer functions and op-amp stability. The first part of the lab investigates the differentiator as an example of a marginally stable circuit. The second part investigates stability by designing an intentionally unstable circuit: an oscillator. After observing the difficulty of maintaining sinusoidal oscillation, an automatic gain circuit is used to keep the oscillator amplitude stable.

Note: This lab requires careful preparation in both the prelab and for the lab itself - particularly the automatic gain control circuit in lab section 4.

**Prelab**

P1. Differentiator

The basic differentiator topology is shown in Figure 6.1. This topology is rarely (if ever) used in practice - you will see why when you build this circuit in the lab.

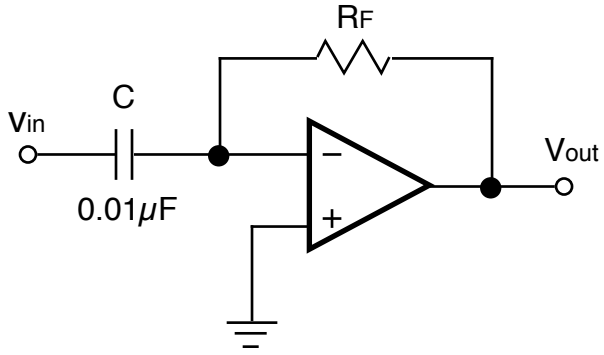


Figure 6.1
Differentiator.

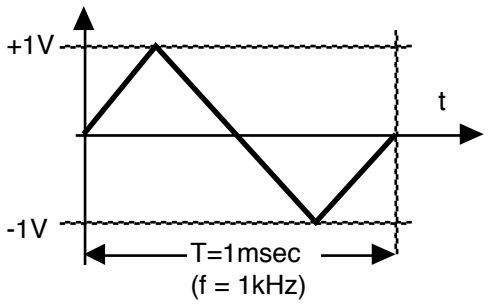


Figure 6.2
Input voltage.

P1.1 Show that the input and output of the differentiator are related by

$$V_{out} = -(R_F\, C)\,\frac{d}{dt}\,V_{in}$$

P1.2 Design a differentiator circuit that will realize the following function:

$$V_{out} = -(1\ \text{msec})\,\frac{d}{dt}\,V_{in}$$

Use a capacitor value of C = 0.01μF.

P1.3 If the differentiator $V_{in}$ is a 1kHz, 1V peak triangle wave as shown in Figure 6.2, what will $V_{out}$ be?

P2. Wien Bridge Oscillator

A popular topology for achieving sinusoidal oscillation in the audio frequency range is the Wien bridge oscillator, shown in Figure 6.3.

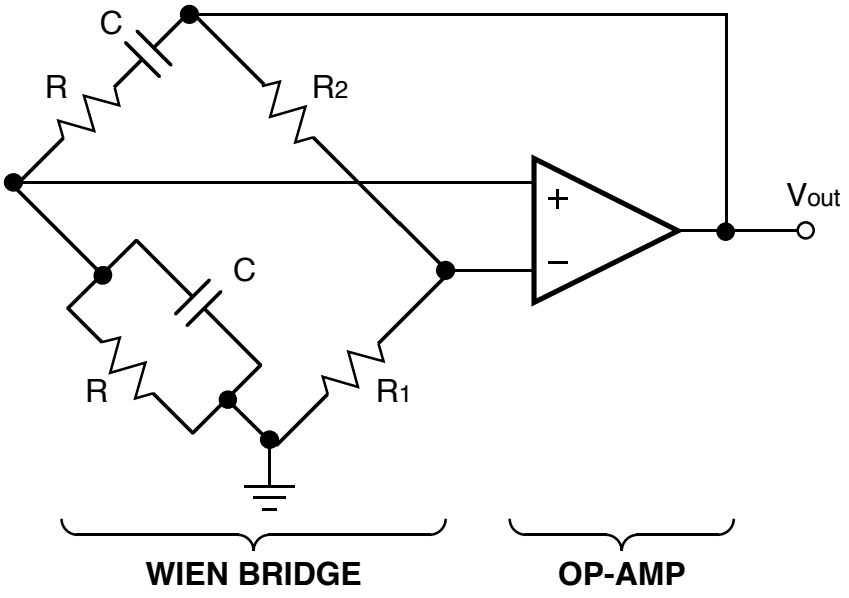


Figure 6.3

Note that this circuit uses positive feedback. For negative feedback (e.g. the op-amp), we have seen that the closed loop gain is

$$A_{CL} = \frac{A}{1 + A\beta}$$

where A is the op-amp open loop gain, and β is the transfer function of the negative feedback network. Frequency stability requires that the condition Aβ = -1 be avoided.

For positive feedback circuits, the closed loop gain is

$$A_{CL} = \frac{A}{1 - A\beta}$$

and the circuit is unstable if Aβ = +1. To make a sinusoidal oscillator, we place the poles of the circuit on the jω axis by making Aβ = +1.

The Wien bridge circuit will oscillate at that frequency (and only that frequency) at which Aβ = +1. Using this criterion, analyze the circuit to determine:

P2.1 The frequency of oscillation $f_o$ in terms of RC.

P2.2 The required gain of the op-amp/R1/R2 network to achieve unity gain around the loop.

Hint: The circuit can be redrawn as shown in Figure 6.4. The β-network is a frequency selective attenuator that achieves a purely real attenuation at one specific frequency $f_o$. The op-amp provides a purely real gain to counteract the attenuation so at $f_o$ the overall gain around the loop is unity. Note that the forward gain A now represents the closed loop gain of the op-amp/R1/R2 network, not the open loop gain of the op-amp.

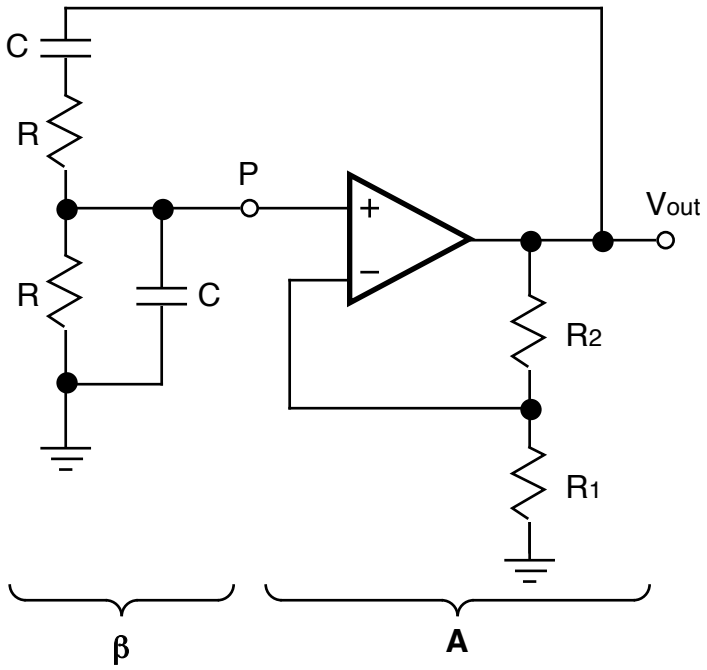


Figure 6.4

To analyze the circuit:

- break the loop at point P,
- determine the transfer function of the β-network from $V_{out}$ to P,
- find the frequency at which the β-network transfer function is purely real,
- determine the magnitude attenuation through the β-network at this frequency, and
- the required op-amp closed-loop gain (determined by R1 and R2) to "undo" the attenuation and make the loop gain unity.

P2.3 Design a Wien-bridge oscillator to the following specifications:

a) Op-amp: LM348

b) ±15V power supplies

c) C = 0.01μF

d) R2 = 1kΩ

e) Output $f_o \approx$ 1kHz, ≈ 5V peak.

## Lab

### 1. Differentiator

Construct your design from prelab section 1.2

1.1 Record the output of your circuit when the input is the triangle wave of Figure 6.2. How does it compare with your prediction of prelab section 1.3? Explain.

### Practical Differentiator

The circuit of Figure 6.1 can be made more stable by inserting a resistor in series with the capacitor, as shown in Figure 6.5.

1.2. Try a range of different values for $R_S$ : 1kΩ, 2kΩ, 5.1kΩ, 10kΩ. How does the output change from lab section 1.1? Note how stability changes from underdamped to critically damped to overdamped ("too stable" – response at $v_{out}$ is slow).

1.3. In your lab notes, explain why the circuit is more stable. Hint: consider comparing the Bode plots for the transfer function of each circuit, as well as the stability plot of Aβ. Over what frequency range does the practical differentiator "look like" an ideal differentiator?

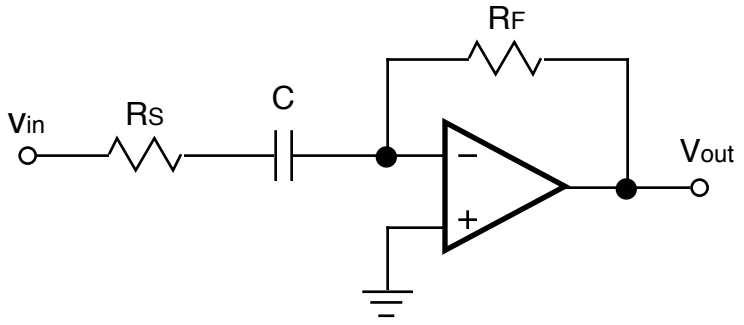


Figure 6.5

Practical Differentiator.

## 2. Wien Bridge Oscillator

Construct the circuit you designed in prelab 2.3. **Be sure to place the circuit components and wiring so that you can easily break the feedback loop at point P in Fig. 6.4**.

2.1 To check that you have designed for the proper loop transmission, break the loop (at point P in Fig. 6.4). Inject a 1kHz sine wave at the op-amp input, and verify that the signal returned around the loop at point P on the Wien bridge has approximately the same amplitude and phase.

2.2 Close the loop, and try to achieve a stable sinusoid at the oscillator output. Note that R1 will have to be "trimmed" (adjusted with a larger parallel resistance, or an external potentiometer) to achieve a loop gain of exactly unity. Don't spend a lot of time on this part - the key is to appreciate the difficulty (impossibility!) in making the loop gain **exactly** unity.

## 3. Oscillator with Automatic Gain Control ("AGC")

The problem with the basic Wien bridge is that if the loop gain is not **exactly** unity, the poles are not **exactly** on the jω axis. Then the output sinusoid either dies away (poles in the left half plane) or grows until saturation occurs (right half plane).

The automatic gain control circuit solves this problem by monitoring the output amplitude and adjusting the loop gain so the sinusoid amplitude is stable. It uses negative feedback just like op-amp circuits, but the controlled variable is the sine wave amplitude rather than voltage.

Consider the circuit shown in Figure 6.6.

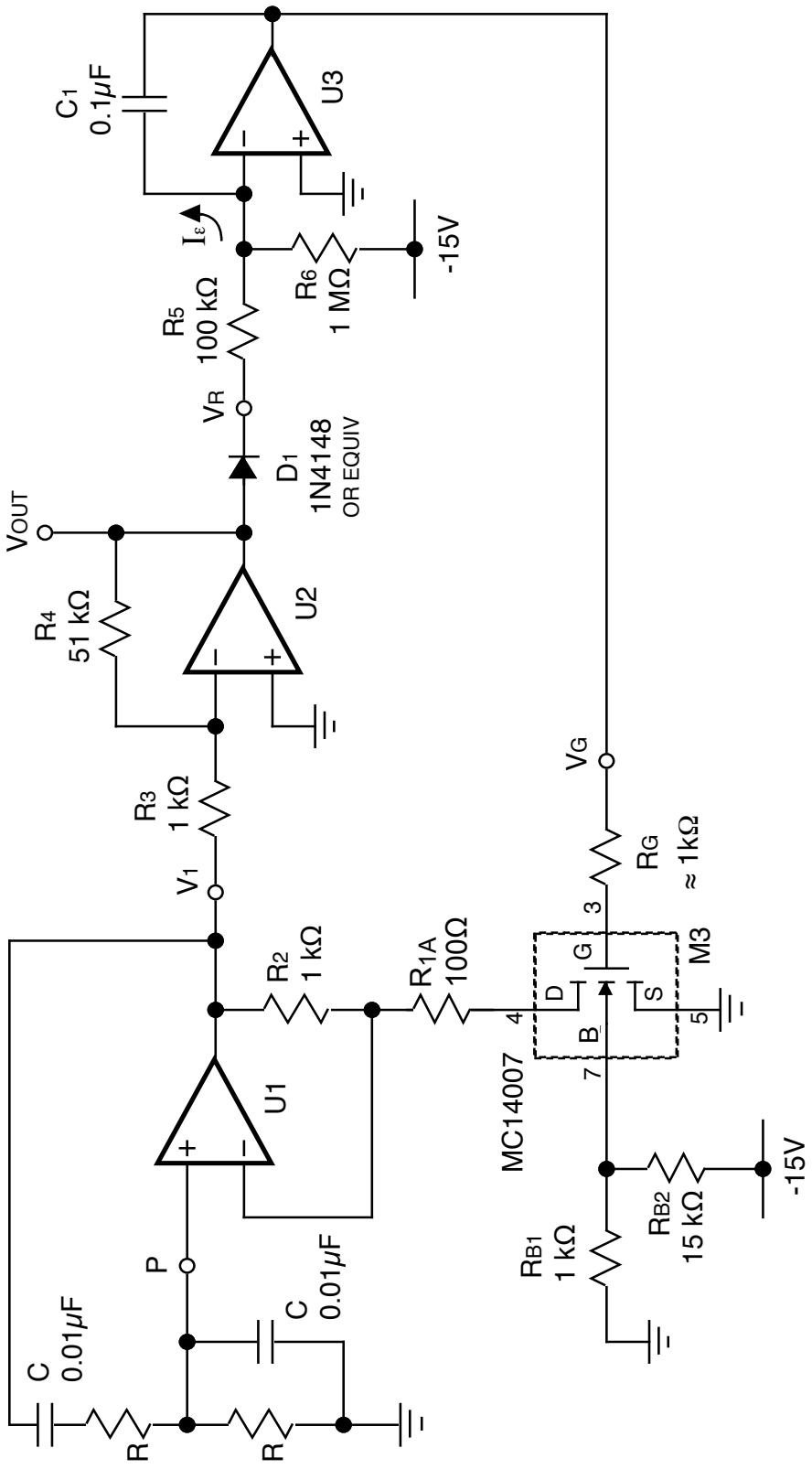
C1
0.1μF
U3
Iε
R5
100 kΩ
R6
1 MΩ
-15V
VR
D1
1N4148
OR EQUIV
VOUT
R4
51 kΩ
U2
R3
1 kΩ
V1
VG
RG
≈ 1kΩ
R2
1 kΩ
R1A
100Ω
U1
MC14007
M3
G
D
S
B
3
4
5
7
P
C
0.01μF
C
0.01μF
R
R
RB1
1 kΩ
RB2
15 kΩ
-15V

Figure 6.6

Resistor R1 is replaced by the series combination of $R_{1A} = 100\Omega$ and a MOSFET from the MC14007 array. The MOSFET is being used in the triode region as a voltage controlled resistor. A typical plot of channel resistance $R_{on}$ vs. gate control voltage $V_{GS}$ is shown in Figure 6.7. Note that as gate voltage increases, $R_{on}$ decreases, which increases the noninverting gain of the U1 op-amp circuit. (You may need to use a smaller value of $R_{1A}$ if your MOSFET has a different $R_{on}$ vs. $V_{GS}$ characteristic.)

Op-amp U2 is configured as an inverting stage with gain = -51. This allows the output $V_{out}$ to be reasonably large (of order 5V peak) while keeping the $V_1$ output of op-amp U1 (and, more importantly, the drain-source voltage $V_{DS}$ on the MOSFET) small. $R_{B1}$ and $R_{B2}$ form a voltage divider that biases the MOSFET substrate at -1V, which is a more negative voltage than either the S or D terminal of the MOSFET.

Diode D1 rectifies $V_{out}$, which (we hope!) will be a sinusoid. $V_R$ is then a half-wave rectified sine wave, which drops across R5 to inject a current into the summing point (inverting input) of op-amp U3. Resistor R6 draws a constant 15uA out of the summing point. The difference current $I_\varepsilon$ is integrated on capacitor C1 to give the MOSFET gate voltage $V_G$. Resistor $R_G$ is for protection of the MOSFET.

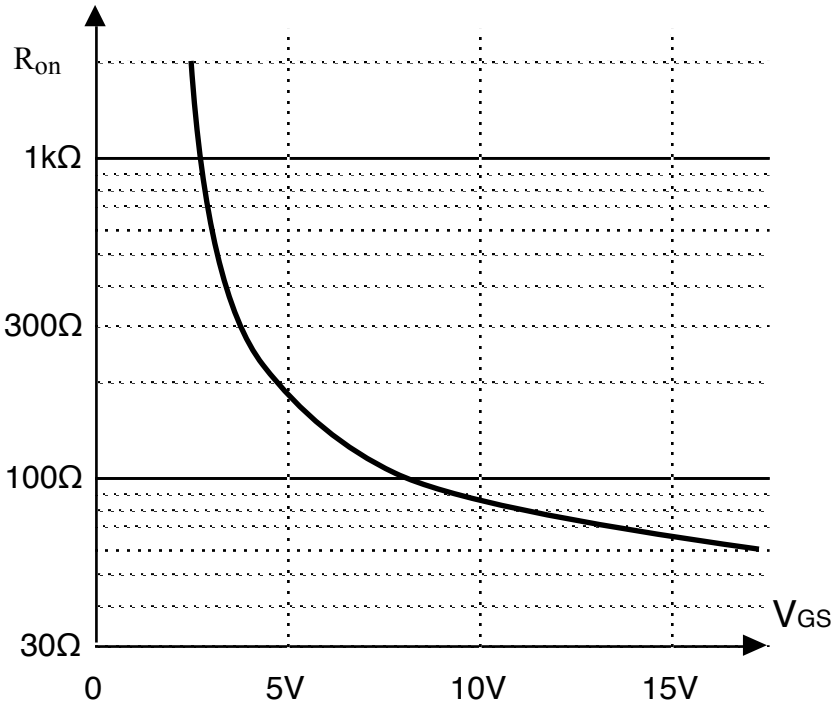


Figure 6.7

Convince yourself of the negative feedback aspect of sine wave amplitude control as follows:

If the amplitude of $V_{out}$ is "too big," $I_\varepsilon$ will be positive (as shown), $V_G$ will decrease, increasing the $R_{on}$, decreasing the gain of op-amp circuit U1, and reducing the amplitude.

If the amplitude of $V_{out}$ is "too small," $I_\varepsilon$ will be negative, $V_G$ will increase, decreasing the $R_{on}$, increasing the gain of op-amp circuit U1, and increasing the amplitude.

3.1 From your condition for oscillation in prelab 2.2, what will be the value of $R_{on}$ when the AGC loop is stabilized?

3.2 From the $R_{on}$ vs. $V_{GS}$ curve in Figure 6.7, approximately what gate drive voltage do you expect will produce this $R_{on}$? (Your MOSFET may have a different curve).

3.3 When the loop is stabilized, the U3 integrator output is (averaged over one cycle of the $V_{out}$ sine wave) constant. This means that the average value of $I_\varepsilon$ is zero. Estimate (very approximately - within ±50% is OK!) the amplitude of $V_{out}$ that will meet this condition. How will this amplitude value change if R5 is changed?

Construct the circuit of Figure 6.6.

3.4 Observe and record signals throughout the circuit ($V_1$, $V_{out}$, $V_R$, $V_G$) to be sure you understand its operation. Measure the frequency and compare to your design prediction from prelab 2.3. How well does the gate voltage agree with your prediction from lab section 3.2?

One of the nice features of automatic gain control is relative insensitivity to component variations within the AGC loop, as shown in the following sections.

3.5 Amplifier U2 is shown in the inverting configuration. How would the circuit operation change if it were noninverting? Verify by "rewiring" with the same values for R3 and R4 in a noninverting configuration. Check signals throughout the circuit to see what changes and what doesn't. Explain.

3.6 How will circuit operation change if the gain of op-amp U2 changes? Try different values for R4 (30kΩ, 75kΩ). Observe signals throughout the circuit ($V_1$, $V_{out}$, $V_R$, $V_G$) to be sure you understand what changes, what doesn't, and why. In particular, is the gate control voltage $V_G$ different? Explain.

Resistor R5 can be used as an amplitude control on $V_{out}$:

3.7 Change R5 to 50kΩ. How does the circuit operation change? In particular, how do $V_G$ and $V_{out}$ change? Explain.

---

LAB WRITEUP

~~Since this is the last lab of the course, and you have the final exam next week, the "writeup" requirement will be a little different:~~

~~Have the lab TA check your lab notebook for the results from parts 1 and 2, and demonstrate the stable Wien bridge oscillator sine wave for part 3.~~

Note: previous was from a B term offering of ECE3204 when the last class was on Friday after the Wednesday Lab. Since you have until next Tuesday, there will be a writeup due. However, since you also have the exam, it doesn't need to be as detailed a writeup. Just include the results of your prelab calculations, and any scope photos and measured results indicating you got the circuits working.