ECE3204 D2015 Lab 5

Digital ÷16 Frequency Divider
Digital-to-Analog Converter
Butterworth Active Filter
Sample-and-Hold Amplifier (part 2)

Objective

The purpose of this lab is to design and test an active Butterworth filter. This filter will be used with a square wave input to produce a near-sinusoidal output. The sine wave will be sampled by the sample-and-hold amplifier built in lab 4. The lab also (briefly) investigates a four-bit D/A converter.

Prelab

P1. Digital ÷16 Frequency Divider

P1.1 Using a timing diagram of input and output waveforms, show that if a four-bit counter has a 20kHz clock input, the MSB output of the counter will be a square wave at a frequency

$$f_{MSB} = \frac{20\text{kHz}}{16} = 1.25\text{kHz}$$

P1.2 Design a circuit to convert the +15V logic swing at the LM555 pin 3 output to a +5V swing CMOS logic signal. The total current drawn from the LM555 output must be less than 1mA; the output resistance of the conversion network must be less than 10kΩ. (Hint: two resistors!).

P2. Digital-to-Analog Converter

The digital CMOS outputs of the 74HC163 counter can be modeled as shown in Figure 5.1:

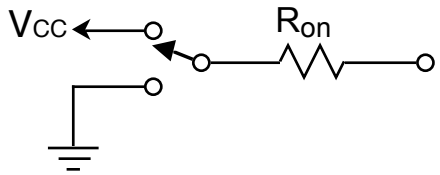

Figure 5.1

where V_{CC} is the chip +5V supply voltage, and $R_{on} \approx 100\Omega$.

P2.1 Design a four-bit D/A converter that will provide the input-output relationship shown in the following table:

Table 5.1

N	Q_D	Q_C	Q_B	Q_A	Vout
0	0	0	0	0	0.0 V
1	0	0	0	1	0.5 V
2	0	0	1	0	1.0 V
3	0	0	1	1	1.5 V
:		:			:
14	1	1	1	0	7.0 V
15	1	1	1	1	7.5 V

Your D/A circuit should draw no more than 0.5mA from any of the sources driving its inputs. You have ±15V supplies available for your circuit.

P2.2 Sketch the output you expect if the input to the D/A converter is the output of a counter. Keep in mind that, without any special reset or carry logic, with a continuous input clock the counter output state will cycle continuously: 1, 2, 3, ..., 14, 15, 0, 1, 2, ...

P3. Butterworth Active Filter

P3.1 Design a third-order lowpass Butterworth filter to the following specifications:

a) Bandwidth = 1.33 kHz

b) DC gain = unity

c) Maximum capacitor size = 0.02μF. (Note: the complete design can be realized with five 0.01μF capacitors).

d) Power supplies: ±15V.

P3.2 Design the topology in the s-plane, showing pole locations. Indicate required ratios between circuit component values.

P3.3 Draw the complete circuit diagram, including actual component values, active devices used, bypassing, etc.

P3.4 What is the approximate attenuation of the filter seen by the third harmonic of a 1.25kHz square wave?

Lab

1. Digital ÷16 Frequency Divider

1.1 Construct the circuit you designed in prelab section P1.2 to convert the +15V logic swing at the LM555 pin 3 output to a +5V swing CMOS logic signal. Verify that V_{CLK} swings from 0 to +5V. This level conversion needs to be done since any voltage outside the 0 to +5V supply rails of the 74HC163 counter could damage the chip.

1.2 Use the output of your conversion circuit as the input clock of the 74HC163 four-bit counter, as shown in Figure 5.2. Record the input and output waveforms, and measure the input and output frequencies to verify the ÷16 frequency relationship. If your lab station has a frequency counter available, you may want to use it since the accuracy is better than the oscilloscope time base. Do your measurements indicate that the ÷16 relationship is **exactly** 16? Explain.

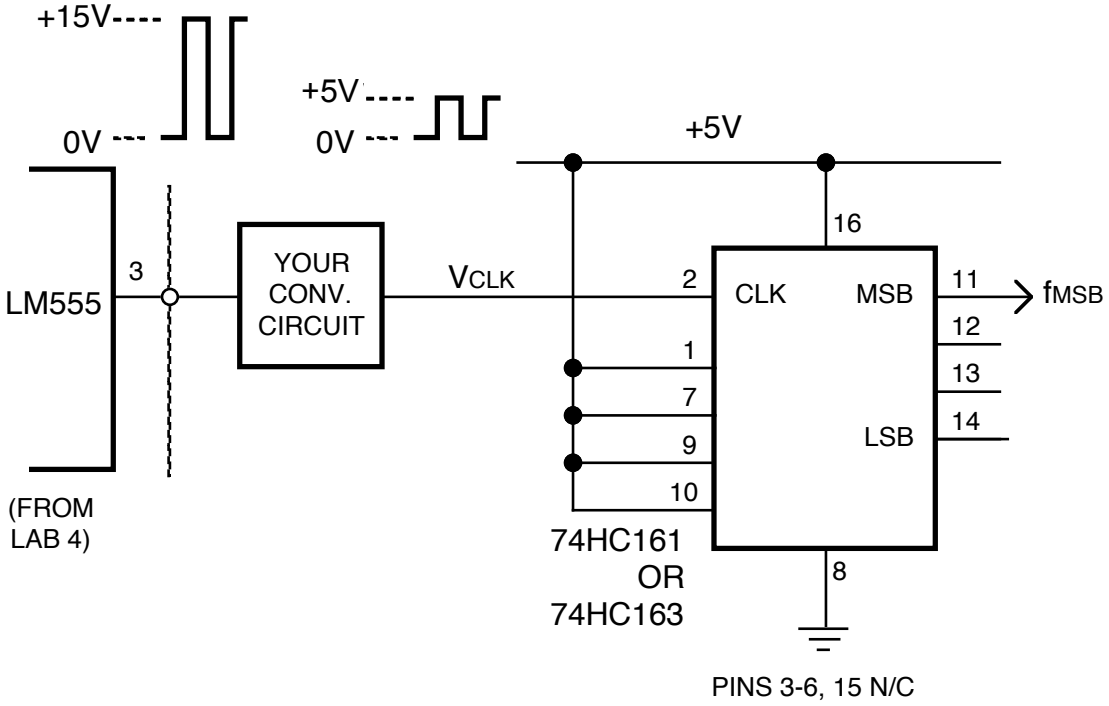

Figure 5.2.

2. Digital-to-Analog Converter

Construct the four-bit D/A converter you designed in section P2.1 of the prelab. Connect it to the output of the four-bit counter as shown in Figure 5.3.

2.1 Record the output voltage V_{out}. Measure the output voltages corresponding to each digital input code. (For the purposes of this lab, measurements using cursors from the oscilloscope screen are sufficiently accurate). How closely do the output voltages conform to what you expected from your design goal in prelab section P2.2 and Table 5.1?

2.2 As an illustration of what happens when the D/A resistors are improperly scaled, increase and decrease the resistance that defines your MSB by about 20% (while leaving the other resistor values unchanged). What happens to the output? Explain.

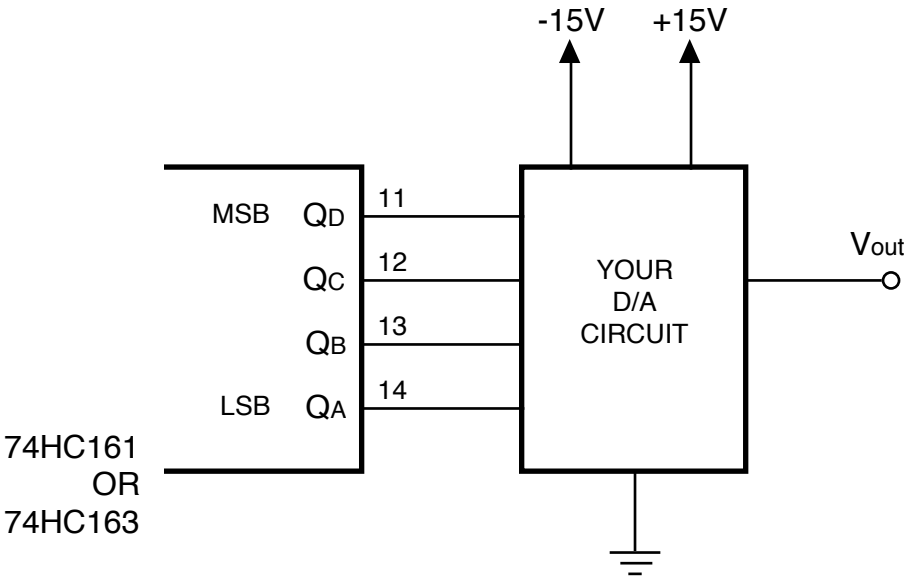

Figure 5.3

3. Butterworth Active Filter

Construct the third-order lowpass Butterworth filter you designed in prelab section P3.3.

3.1 Measure and plot the frequency response of your filter. Consider logarithmically spaced test frequencies, since the frequency response (Bode) plot is on log-log axes. Be sure to cover a wide enough frequency range (at least 100 Hz to 10 kHz) to verify the maximally flat magnitude response in the passband, as well as the -60dB/decade rolloff in the stopband.

3.2 What is the 3-dB bandwidth of your circuit? How closely does it agree with your design goal from prelab section P3.1?

3.3 Measure and record the step response of your circuit to an input 1V, 100Hz square wave. Measure the 10%-90% rise time and "overshoot" (excursion of step beyond final value as a fraction of step amplitude). How does this compare (both qualitatively and quantitatively) with the step response of a simple, single-time-constant RC lowpass filter? Explain.

3.4 Use the MSB output of the counter (a 5V pk-pk, 1.25kHz square wave) as the input of your Butterworth filter. Measure and record the filter output. Explain the output waveform in light of your response to prelab section P3.4.

4. Sample-and-hold part II

In lab 4, viewing the output of the sample-and-hold required stopping the trace acquisition, since the sample clock (from the LM555 circuit) and the sampled waveform (from the function generator) were not synchronized. In this part we will sample the synchronous 1.25kHz sine wave out of the Butterworth filter, which will result in a stable scope display.

Double-check the wiring of your sample-and-hold circuit to make sure it matches the topology of Figure 4.3 from Lab 4.

4.1 Connect the Butterworth filter output V_{FILTER} to the sample-and-hold input as shown in Figure 5.4.

4.2 Use the capability of the 4-channel scope to record the V_{FILTER}, V_{HOLD}, and V_{GATE} waveforms.

4.3 "Droop:" Place a 1 MΩ resistor in parallel with the hold capacitor. What happens to the "hold" part of the waveform? What happens to the "sample" part of the waveform? Explain.

4.4 Analog switch: Remove the 1 MΩ resistor, and replace C_{HOLD} with a 10kΩ resistor. Record the output waveform.

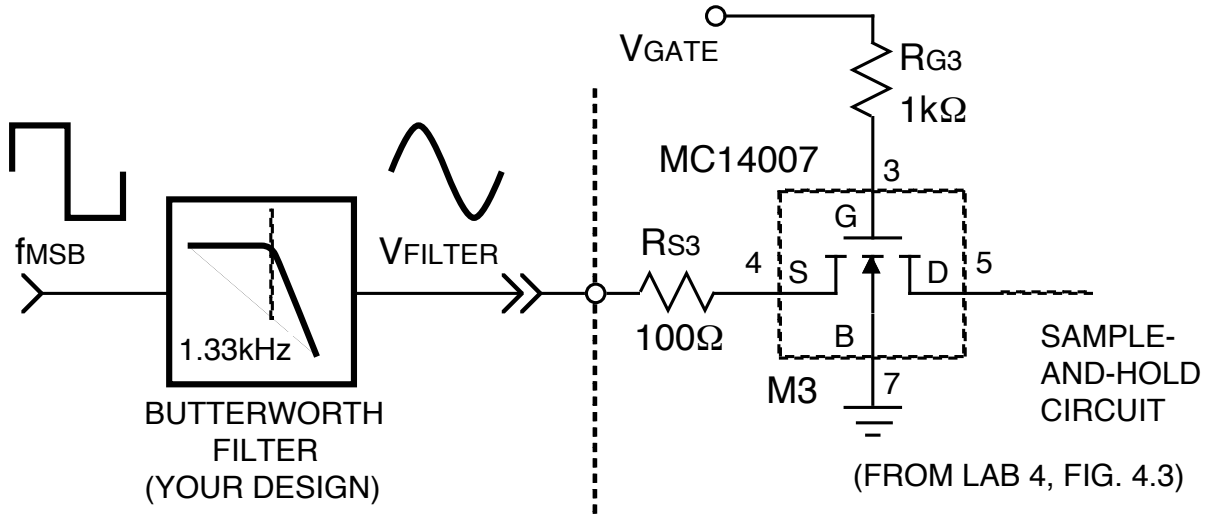

Figure 5.4

Lab Writeup

Organize your lab writeup in sections similar to those of this handout.

Be sure to (at a minimum) answer any questions posed in this lab handout. Additionally, if any other insights come to you in the course of your analyzing and thinking about your data, discuss those as well.

Feel free to use screen shots of the oscilloscope to illustrate your measurements.

See the Sample Lab Writeup for general tips on writeup presentation style.