ECE 3204 D2015 Lab 4

LM555 Timer
MOS Inverter
MOSFET Analog Switch
Sample-and-Hold Amplifier
2:1 Analog Multiplexer

Objective

The purpose of this lab is to gain familiarity with circuits that are useful in "mixed-signal" (both analog and digital) applications: a clock generator, digital and analog switches, the sample-and-hold, and a 2-to-1 analog multiplexer. See section 5.1 of the 6th edition textbook of your textbook for coverage of the MOSFET as an analog switch.

Prelab

P1. LM555 Timer

This functional block is covered in section 17.7 of the 6th edition textbook. Figure 4.1 below shows the LM555 configured as an astable multivibrator (clock generator).

P1.1 Qualitatively, what is the expected waveform on the timing capacitor (at pins 2 and 6)? What are the maximum and minimum values of the capacitor voltage?

P1.2 Calculate values required for R_A and R_B to achieve a 20kHz (±5%) clock signal with a duty cycle of approximately 60%. For the timing capacitance C, use 0.01μF.

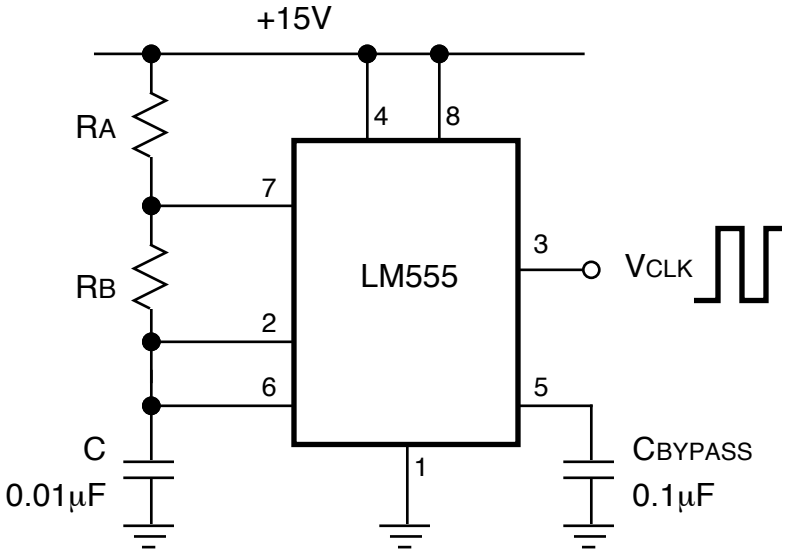

Figure 4.1

P2. CMOS Inverter

The digital output V_{clk} of the LM555 timer will swing from its negative to positive supply: ground to +15V. The 2:1 multiplexer will require V_{clk} and its complement V_{comp}. To generate the complement signal, we will be using a digital inverter constructed of two transistors from the MC14007 MOSFET array, as shown in Figure 4.2.

P2.1 Explain how the circuit of Figure 4.2 produces the logic complement of V_{clk} at V_{comp}.

One advantage of CMOS logic is its low power dissipation.

P2.2 Consider the drain currents i_{D1} and i_{D2} flowing in the transistors M1 and M2. Assuming there is no load on V_{comp}, what are the approximate drain currents when V_{clk} is high? When V_{clk} is low? When does a significant amount of drain current flow?

P2.3 Sketch V_{comp} when V_{clk} is driven from pin 3 of the LM555 circuit you designed in part P1.2.

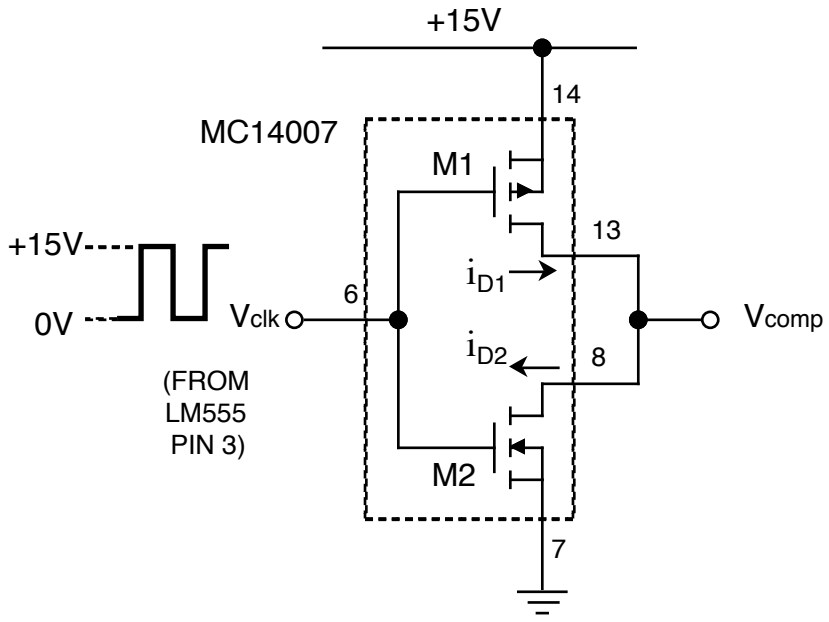

Figure 4.2

P3. Sample-and-hold

The sample and hold circuit of Figure 4.3 uses one of the MC14007 N-channel MOSFETs as analog switch M3. Note that V_{GEN} is a 1kHz, 5V peak-to-peak sine wave with a +2.5V DC offset: the voltage swings from 0V to +5V. Resistors R_{G3} and R_{S3} are for protection of the analog switch.

P3.1 Show that when V_{GATE} = +15V, the analog switch is conducting and $V_{CAP} \approx V_{GEN}$ for V_{GEN}, 0V ≤ V_{GEN} ≤ +5V.

P3.2 Show that when V_{GATE} = 0V, the analog switch is off and the voltage at V_{CAP} will remain constant, holding its previous value when V_{GATE} transitioned to 0V.

P3.3 Sketch V_{GATE} and the sample-and-hold output V_{HOLD} when the gate is driven from V_{comp} of section P2.3, and V_{GEN} is as shown.

P3.4 If V_{GEN} were to go to a voltage of -5V, what would happen in the analog switch MOSFET M3? (Hint: consider the role of the substrate/body (B) terminal of the MOSFET)

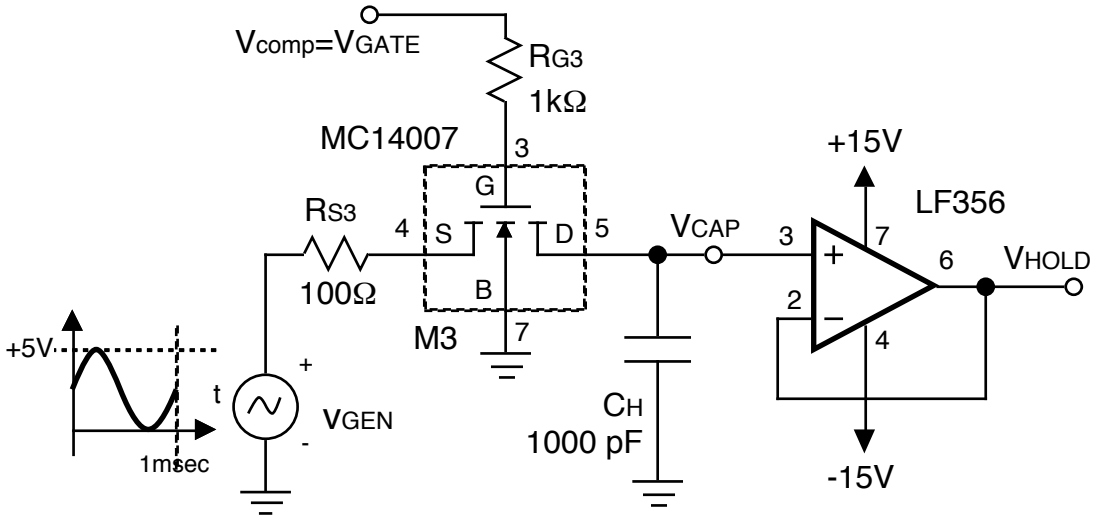

Figure 4.3

P4. Analog Multiplexer

The sample and hold circuit of Figure 4.3 can be modified to make a 2-to-1 analog multiplexer as shown in Figure 4.4. The hold capacitor C_{HOLD} is removed, and one of the MC14007 N-channel MOSFETs is used as analog switch M4. The input to the M4 switch is a DC voltage V_{DC} from a potentiometer connected between the +15V supply and ground. The gate of M4 is driven by V_{clk}, which is the logic complement of V_{comp}. Thus when one switch is on, the other is off, and vice versa. Resistors R_{G3}, R_{G4}, R_{S3}, and R_{S4} are for protection of the analog switches.

P4.1 When V_{comp} = +15V and V_{clk} = 0V, what are the states ("on" or "off") of the M3 and M4 MOSFET analog switches? What is the voltage at V_{MUX}? at V_{OUT}?

P4.2 Repeat P4.1 for V_{comp} = 0V and V_{clk} = +15V.

P4.3 Using a timing diagram format, sketch the control signals V_{comp} and V_{clk}, the multiplexed voltage V_{MUX}, and the output V_{OUT} when V_{DC} = +2.5V and V_{GEN} is as shown.

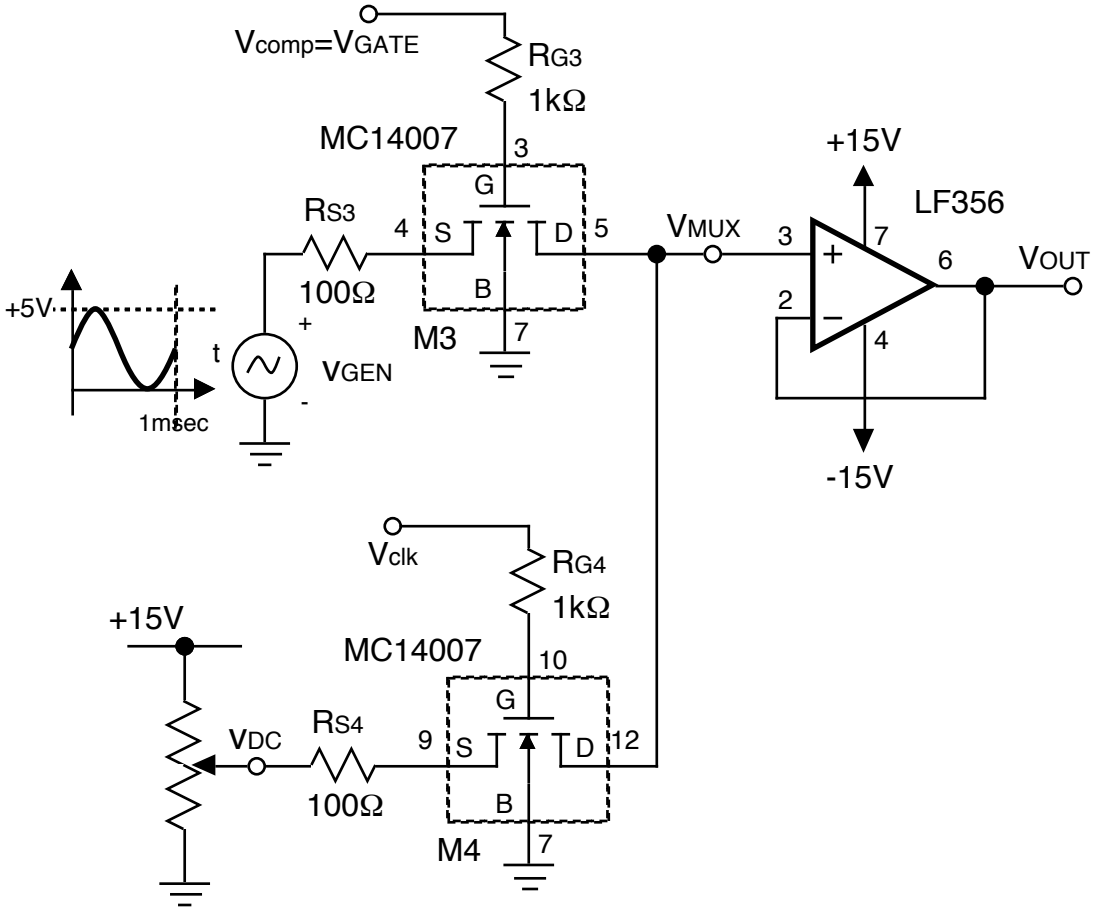

Figure 4.4

Lab

A couple of notices before starting this lab:

1) BE SURE **NOT** TO DISASSEMBLE YOUR BREADBOARD WHEN YOU ARE DONE WITH THIS LAB! LAB 5 WILL BUILD ON THESE CIRCUITS!

2) BE **EXTREMELY** CAREFUL WITH THE MC14007 MOSFET! IT IS VERY SUSCEPTIBLE TO DAMAGE FROM ELECTROSTATIC DISCHARGE (ESD) AND/OR IMPROPER SUPPLY VOLTAGE CONNECTION. DOUBLE CHECK THE PACKAGE PINOUT AND YOUR WIRING BEFORE APPLYING POWER!

1. LM555 Timer

Construct the circuit of Figure 4.1 with your design values from prelab section P1.2.

1.1 Using the capability of your 4-input scope, display and record the waveforms at the capacitor (pin 2), the discharge pin (pin 7), and the output (pin 3). Measure the frequency and the duty cycle. How do they compare with what you expect from your prelab design?

1.2 Consider the capacitor charge and discharge waveform on pin 2. What are the maximum and minimum voltages of this waveform? How does this compare with what you expect from your prelab?

1.3 Vary the supply voltage down to about +5V. Does the frequency change? Explain.

Having the frequency independent of the supply voltage is a very desirable quality in battery powered systems, where the supply voltage decreases over time as the battery discharges.

2. CMOS Inverter

Set the positive supply back to +15V. Construct the circuit of Figure 4.2, with V_{clk} driven from pin 3 of the LM555 circuit you constructed in part 1.

2.1 Measure and record the waveform at V_{comp}. How well does this circuit provide a 0 to +15V waveform? How does this result compare with what you expected from prelab section P2.3?

3. Sample-and-hold

Some measurement circuits (for example, some analog-to-digital converters) require that their input voltage remain constant during the time it takes for the circuit to complete a measurement. If the signal being measured is changing during this time, the sample-and-hold circuit can be used to capture the instantaneous value of the signal and hold it for a longer period of time.

Construct the sample and hold circuit of Figure 4.3 using the MC14007 N-channel MOSFET as analog switch M3. The gate should be driven from V_{comp} of section 2. V_{GEN} should be as shown in Figure 4.3.

3.1 Using the capability of your 4-input scope, display and record the waveforms at the input V_{GEN}, the control input V_{GATE}, and the sample-and-hold output V_{HOLD}. You will probably get the best scope display by triggering off the V_{GATE} waveform, displaying both V_{GATE} and V_{HOLD}. You may have to fine-adjust the 1kHz frequency to get a stable display of the sampling and holding behavior of this circuit (or, with the digital scope, just STOP the acquisition to freeze the waveform).

3.2 On the waveform, identify where the V_{HOLD} signal shows that when V_{GATE} = +15V, the analog switch is conducting and $V_{CAP} \approx V_{GEN}$.

3.3 On the waveform, identify where the V_{HOLD} signal shows that when V_{GATE} = 0V, the analog switch is off and the voltage on V_{CAP} remains constant.

4. Analog Multiplexer

The multiplexer is used when one measurement circuit (for example, an analog-to-digital converter) must monitor multiple analog signals (for example, the left and right audio channels in a digital audio system). In this section of the lab, we will see that the multiplexer output voltage switches back and forth between the two inputs.

Modify the sample and hold circuit to make the 2-to-1 analog multiplexer of Figure 4.4.

4.1 Using the capability of your 4-input scope, display and record the control input V_{clk}, the two analog inputs, and the multiplexer output V_{MUX}.

4.2 Verify your determination of the MOSFET analog switch states from prelab section P4.1.

4.3 Adjust the potentiometer to vary the DC input voltage to one channel of the multiplexer. How is the multiplexer output affected? Explain.

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Lab Writeup

Organize your lab writeup in sections similar to those of this handout.

Be sure to (at a minimum) answer any questions posed in this lab handout. Additionally, if any other insights come to you in the course of your analyzing and thinking about your data, discuss those as well.

Feel free to use screen shots of the oscilloscope to illustrate your measurements.

See the Sample Lab Writeup for general tips on writeup presentation style.