ECE 3204 D2015
HW Set 5

Due in class Friday April 17.

To make life easier on the graders:

- Be sure your NAME and ECE MAILBOX NUMBER are prominently displayed on the upper right of what you hand in.
- When appropriate, indicate answers with a box or underline
- Work as neatly as possible

All text problems from Sedra & Smith 6th edition.

1) Text 17.37 (p. 1392) [LM555 timer functionality]

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2) Text D17.39 (p. 1392) [Square wave oscillator with LM555]

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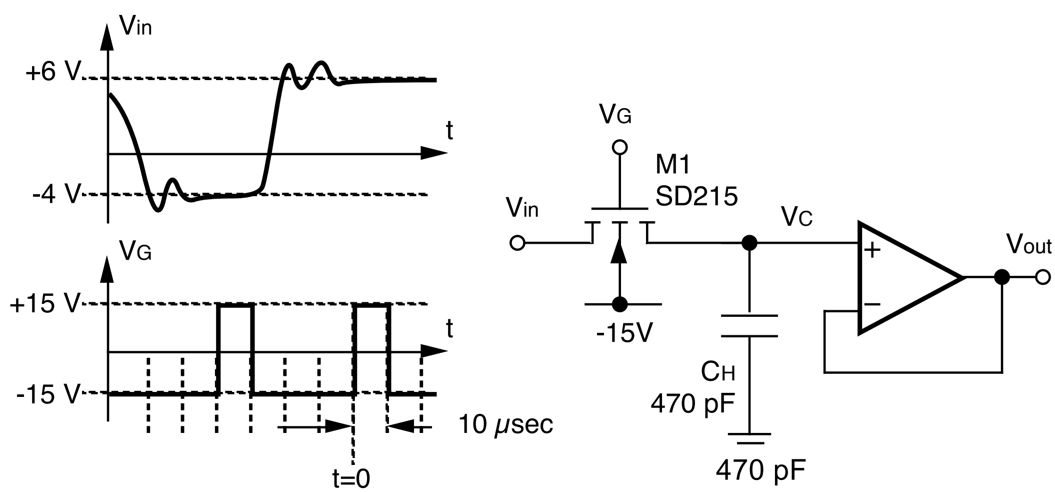
3) [Sample-and-hold]

In the sample-and-hold circuit shown in the figure below, the SD215 MOSFET is an N-channel device which turns on when V_{GS} is more positive than the threshold voltage $V_T \approx 2V$. For this problem, assume the maximum value of SD215 on resistance is 300Ω.



a) For V_{in} and V_G as shown, sketch the voltage on the hold capacitor V_C for time $-10\mu s < t < +10\mu s$. Your sketch does not need to be extremely accurate, as long it represents the qualitative behavior of the waveform. Note that t = 0 is defined at the rising edge of the second V_G pulse.

b) At what time t > 0 does V_C settle to within 10mV of its final value?

c) What must the slew rate of the op-amp be so that V_{out} is not distorted by slew rate limiting?

4) [LM555 analysis practice]

One problem with the simple LM555 clock circuit discussed in lecture and used in Lab 4 is that the duty cycle is constrained to be greater than 50%. This can be seen from the form of the equation for duty cycle (Note that the equation on p. 8 of the LM555 data sheet is wrong!):

$$\delta = \frac{R_A + R_B}{R_A + 2R_B}$$

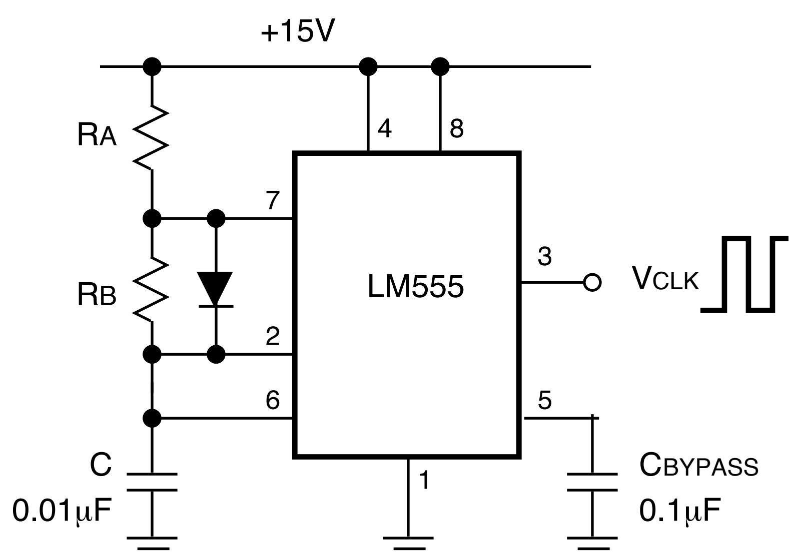
Clearly this is a problem if a true "square wave" (50% duty cycle) is desired at the output.

If a diode is added to the simple circuit from the lab (as shown in the figure below), show that the equation for duty cycle is changed so that a ≈50% duty cycle is possible. To simplify the math, you may assume an ideal diode with 0V forward voltage drop.

a) Determine the expression for output clock frequency in terms of R_A, R_B, and C. (Hint 1: consider the voltage waveform on the timing capacitor, and the paths of the charging and discharging currents).
(Hint 2: You will need to look at the internal block diagram of the LM555; refer to the block diagrams posted with lecture 15 and 16 on the course website).

b) Determine the expression for duty cycle in terms of R_A and R_B.

c) With a C value of 0.01μF, choose R_A and R_B to realize an output clock of 10kHz, and a duty cycle of ≈50%.



5) [D/A converter]

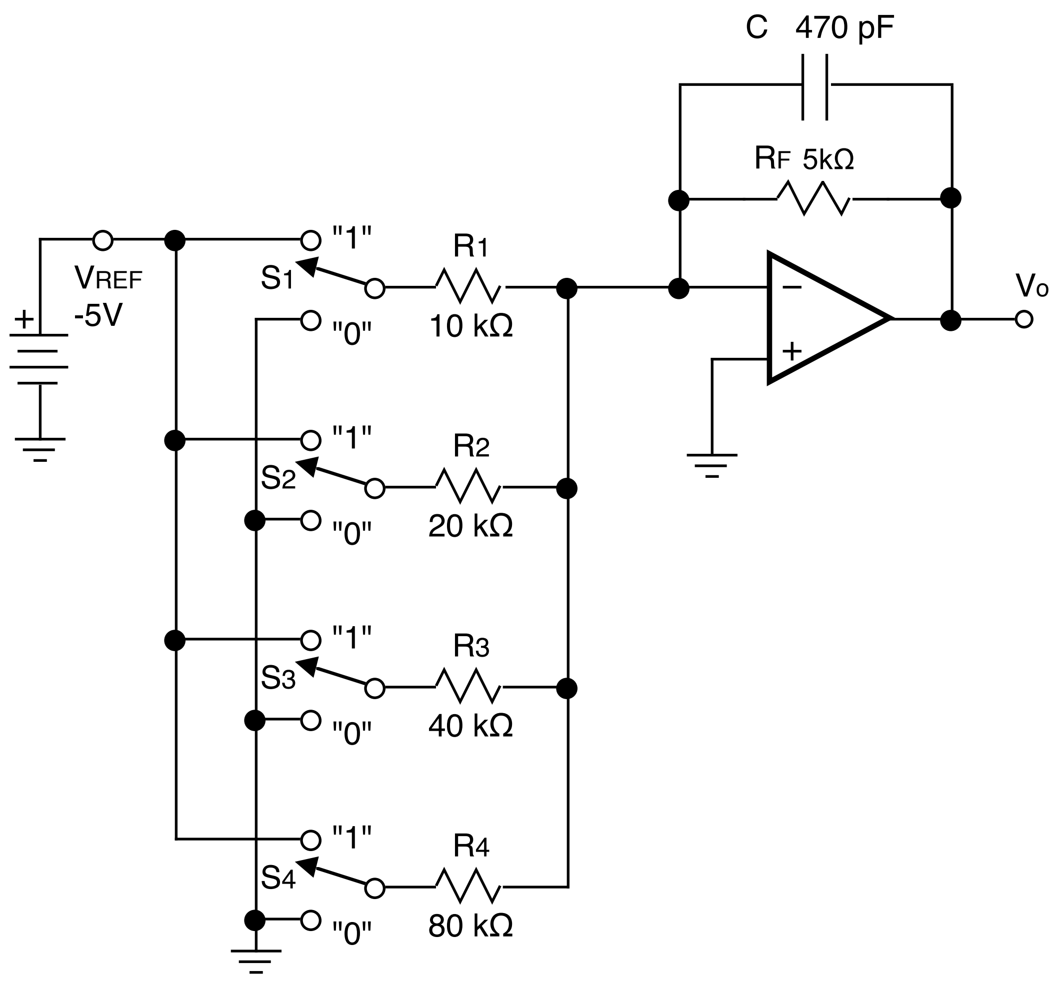
The figure below shows a 4-bit D/A converter.

a) What is the full-scale voltage of this D/A?

b) What is the LSB step size?

c) Assuming the op-amp to be ideal, what is the settling time (to 1/2 LSB accuracy) for a full scale step? ("Full scale step": Digital code changes from 0000 to 1111).

d) What must the slew rate of the op-amp be so that the settling time you predict in part (c) is not degraded by slew rate limiting?



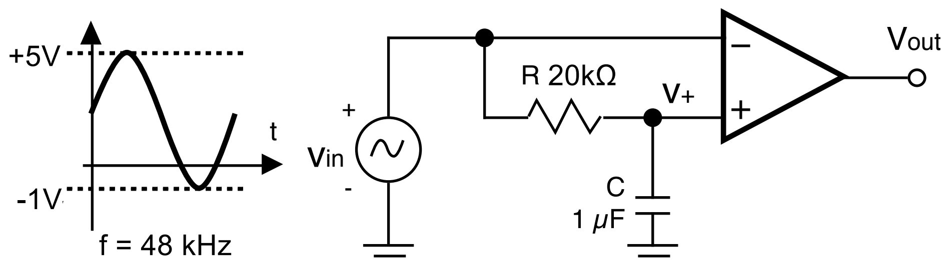
6) [Frequency counter]

The circuit in the figure below is used in a frequency counter application. The input voltage V_{in} is a 48kHz, 6V peak-to-peak sine wave riding on a +2V DC level. The op-amp is ideal except for an output voltage clipping limit of ±15V.

a) Find an approximate (error ≤ 100mV) expression <u>in the time domain</u> for voltage V_+.

b) On a timing diagram, sketch V_+ and V_{out} for V_{in} as shown. Label any significant voltages and/or times.

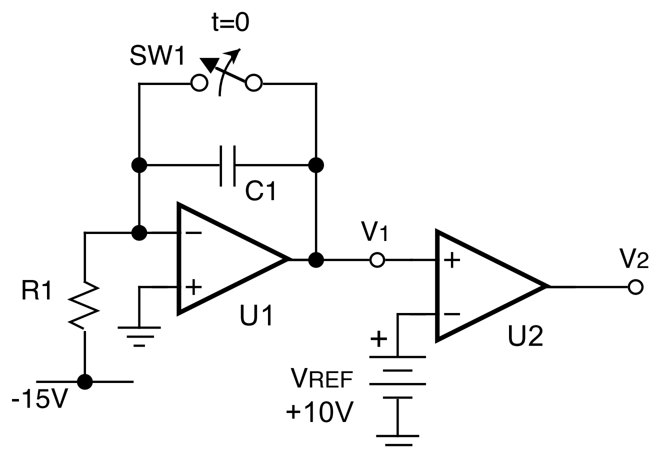
c) Repeat part (b) with the op-amp ideal except for a slew rate limit of ±5 V/μsec.



7-8) (weight=2 problems) [Timer circuit design]

This problem involves design of the timing circuit shown in the figure below. The intent is for the logic signal at the output of comparator U2 to change state at a fixed delay time of t_{DLY}=30µs after switch SW1 is opened.

For time t<0, switch SW1 is closed, shorting capacitor C1. At time t=0, the switch is opened. You may consider the op-amps to be ideal except for an output voltage limit of ±13V.



a) Find an expression for voltage V1 as a function of time for t>0. Since the values of R1 and C1 are not determined yet, your expression will have to be symbolic (in terms of R1, C1) rather than numeric.

b) At what time t_{MAX} does V1 reach the voltage limit of the U1 op-amp (again, in terms of R1 and C1)?

c) Sketch a timing diagram of voltages V1 and V2 vs. time for times t=0 through $t=t_{MAX}$.

d) Determine values for R1 and C1 from the following conditions:

- Output V2 makes a transition between the ±13V output levels at time t_{DLY}=30µs.
- Maximum current drawn from output of U1 op-amp is 100µA.

e) An advantage of circuits such as the LM555 timer is that their timing characteristics were insensitive to changes in the power supply voltage. Is that true in this case? If the -15V supply changes, does the t_{DLY} time change?

f) Suggest a way to make the t_{DLY} time insensitive to variations in the -15V supply. Hint: Use another op-amp and some gain setting resistors to develop the +10V V_{REF} in a different way.