Name SOLUTIONS

ECE Box # ______________

A	85-100
B	70-84
C	55-69

μ 74.9

σ 13.7

MED 77

Problem	Average Score	Points
1	22.4	30
2	24.2	30
3	28.3	40

ECE3204 D2009

Microelectronics II

Exam 3

- This is a **closed book, closed notes test**! Use of calculators (no pre-stored formulas!) is allowed.
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- Look for the simple, straightforward way to solve the problem for the level of accuracy required. **Don't get entangled in unnecessary algebra**.
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- Unless otherwise indicated or implied, you may assume all op-amps to be ideal.
- You will have 55 minutes to complete this exam. There are three problems on a total of 7 pages.

1. In the sample-and-hold circuit shown on the opposite page, assume the MOSFET can be modeled as a switch with an "on" resistance of $r_{DS(on)} = 1k\Omega$. For parts (a) through (e), you may assume the op-amps to be ideal.

a) Is this an N-channel or P-channel MOSFET? (Circle one) **[1]**

(N-CHANNEL) P-CHANNEL

Explain! How do you know? **[4]**

DIRECTION OF BODY-CHANNEL P-N JUNCTION

For parts (b) and (c): A colleague suggests that op-amps "A" and "B" are not necessary, since as followers they only provide unity voltage gain.

b) What is the purpose of op-amp "A"? That is, how would sample-and-hold circuit performance be degraded if the signal source were connected directly to the MOSFET switch?

IMPROVES t_{ACQ}: WOULD CHARGE THROUGH R_S WITHOUT OP-AMP **[5]**

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c) What is the purpose of op-amp "B"? That is, how would sample-and-hold circuit performance be degraded if the hold capacitor C_H were connected directly to the load resistor R_L?

PREVENTS R_L FROM DISCHARGING C_H **[5]**

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d) Using the space on the opposite page, CAREFULLY sketch the capacitor voltage V_C as a function of time for $0 \leq t \leq 5\mu sec$. **[5]**

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e) Find the acquisition time t_{ACQ} defined as the time from the MOSFET switch turning on until v_C has settled to within 1mV of its ideal final value (Accuracy ±10%)

t_{ACQ}: $9.999V = 10V - 20V e^{-t_{ACQ}/r_{DS(on)} C_H}$ (27ns) **[5]**

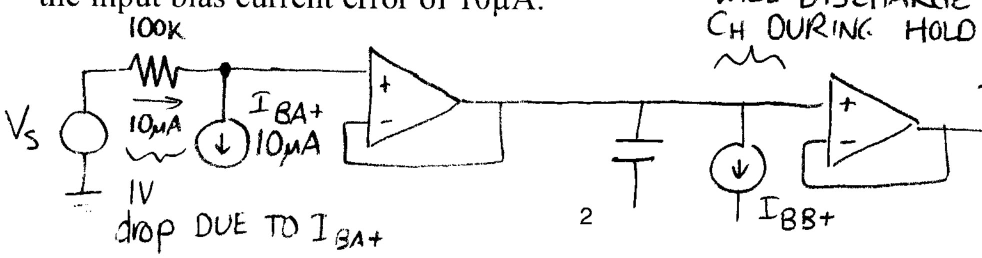
t_{ACQ} = 267ns $t_{ACQ} = 27ns \ln\left(\frac{20V}{1mV}\right) =$

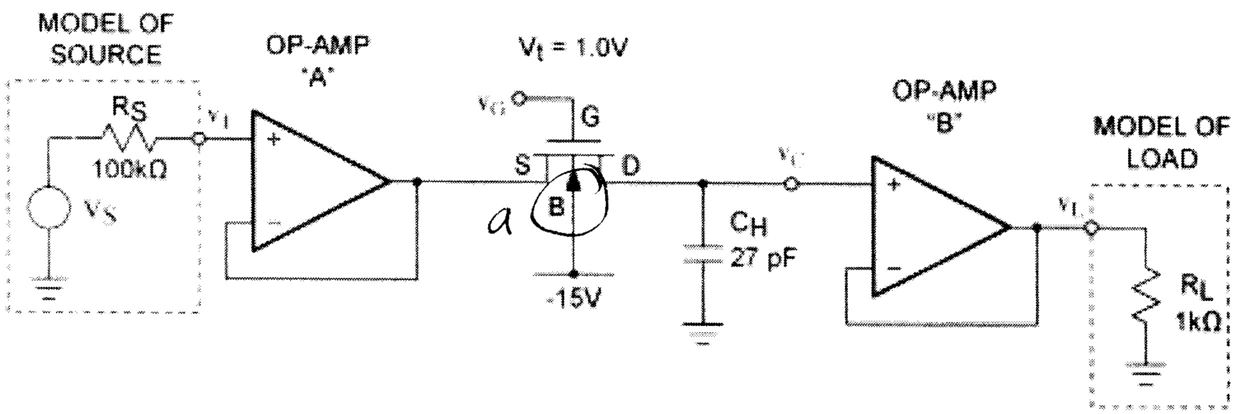
For part (f), assume the op-amps ideal except for an input bias current error of 10μA.

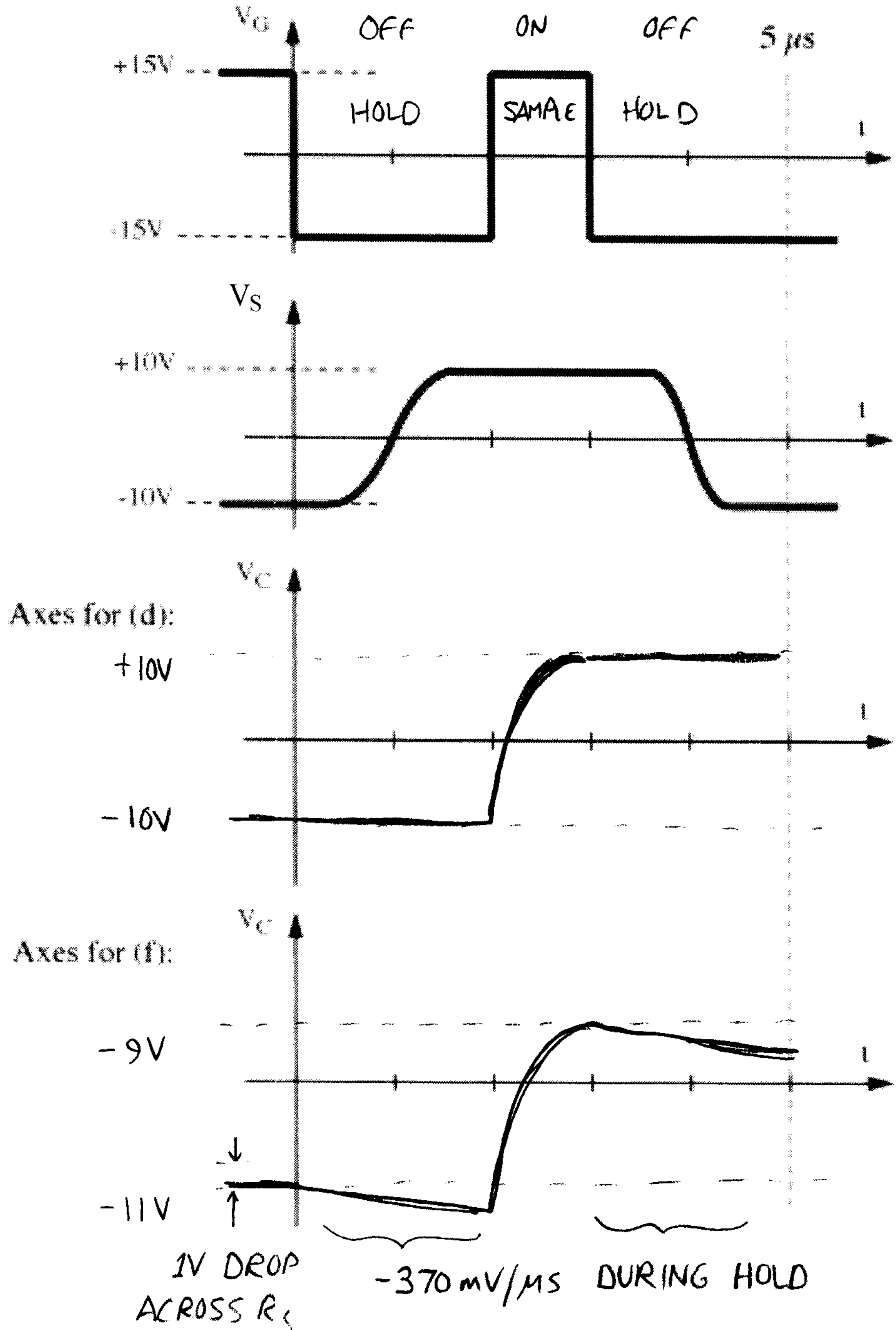
f) Using the space on the opposite page, CAREFULLY sketch the capacitor voltage V_C as a function of time for $0 \leq t \leq 5\mu sec$. Include any effects that may be due to the input bias current error of 10μA. **[5]**

WILL DISCHARGE C_H DURING HOLD

$\frac{10\mu A}{27pF} = 370 mV/\mu s$




MODEL OF SOURCE
RS
100kΩ
VS
VI
OP-AMP "A"
Vt = 1.0V
VG
G
S
D
B
a
-15V
VC
CH
27 pF
OP-AMP "B"
MODEL OF LOAD
VL
RL
1kΩ


VG
+15V
-15V
OFF
ON
OFF
5 μs
HOLD
SAMPLE
HOLD
t
VS
+10V
-10V
t
VC
Axes for (d):
+10V
-10V
t
VC
Axes for (f):
-9V
-11V
t
1V DROP ACROSS RS
-370 mV/μs DURING HOLD

2. At the top of the following page are six s-plane pole-zero plots, designated A - F:

Following are qualitative descriptions of various circuit functions. For each description, indicate ALL pole-zero plots which could correspond to the transfer function of the circuit being described. NOTE:

- Each plot A-F may be used any number of times: once, more than once, or not at all.
- Some descriptions may correspond to more than one plot. You need to give all of the correct plots to receive full credit.

a) Plot of open-loop gain for an op-amp that is unity gain stable. **[4]**

PLOT(S): B

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b) A sine wave oscillator with constant output amplitude.. **[4]**

PLOT(S): D

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c) A closed-loop op-amp. At the frequency where $|A\beta| = 1$, the phase shift $\angle A\beta = -225°$. **[4]**

PLOT(S): E

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d) A Butterworth low-pass filter. **[4]**

PLOT(S): C 4th order

B 1st order

What order filter? Indicate the filter bandwidth on the s-plane plot(s)

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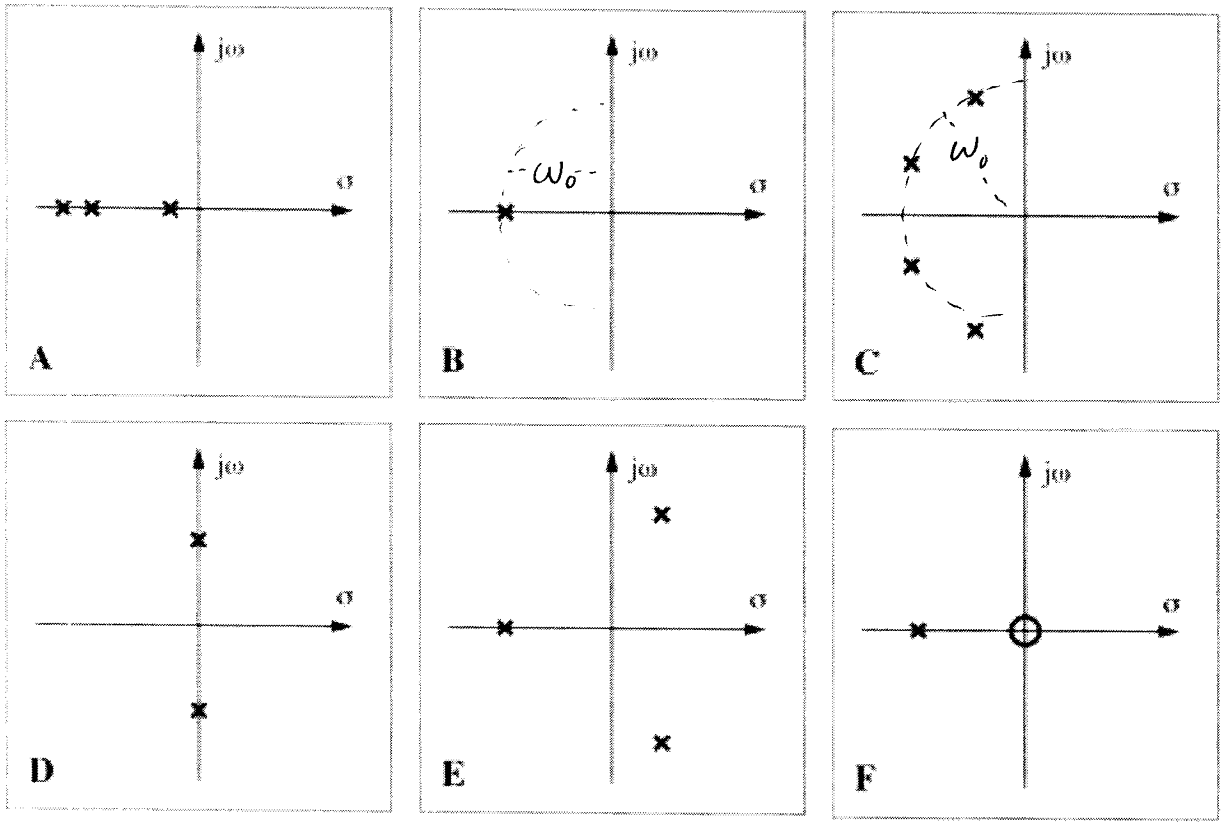
e) A highpass filter with zero transmission at DC ($|T(0)| = 0$). **[4]**

PLOT(S): F

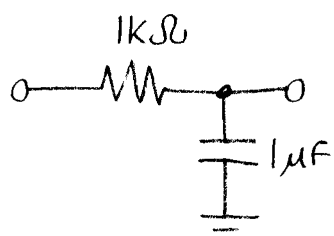


f) In the space below, write a transfer function T(s) for any one of the s-plane plots shown above and design a circuit to implement the transfer function. Your choice, just indicate the letter of the plot in the box. Numerical values required, accuracy ±10%. Choose wisely! No extra credit for complicated circuits that do not implement the s-plane plot and/or transfer function you choose!

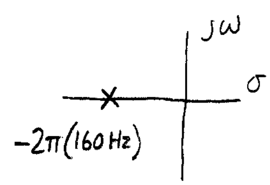
[10]

Plot: **B** Transfer function: $T(s) = \dfrac{1}{1 + sRC}$

Circuit design:



$$f_{3dB} = \frac{1}{2\pi(1k)(1\mu F)} = 160\text{ Hz}$$



LOTS OF OTHER POSSIBILITIES!

3. An op-amp has an open-loop DC gain of $10^5 = 100{,}000$ and two poles: one at 10Hz, and one at 100kHz.

a) Determine the expression for A(s), the op-amp open-loop gain transfer function. **[5]**

$$A(s) = \frac{100000}{\left(1 + \frac{s}{2\pi[10Hz]}\right)\left(1 + \frac{s}{2\pi[100kHz]}\right)}$$

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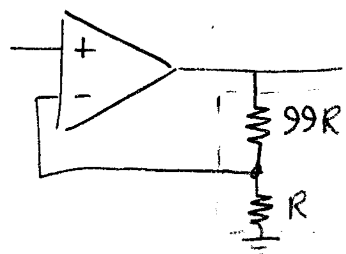
b) Using the space on the opposite page, carefully sketch the magnitude and phase Bode plots |A(f)| and ∠A(f) for the op-amp open-loop gain. Or, if you prefer, |A(ω)| and ∠A(ω). **[5]**

Now consider this op-amp connected closed loop with a noninverting gain of +100.

c) Sketch the circuit configuration:



$\beta = 0.01$

[5]

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d) Determine the numerical value of the feedback factor β, the fraction of the op-amp output that is fed back to the op-amp inverting input. **[5]**

β = 0.01 = 40dB

$|\beta| = 0.01 = -40dB$

$\angle\beta = 0$

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e) Using the space on the opposite page, carefully sketch the magnitude and phase Bode plots |Aβ| and ∠Aβ for the loop gain. $\angle A\beta = \angle A$ **[5]**

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f) Using your plot from (e), determine the frequency f_1 at which the magnitude of the loop gain is equal to unity: when |Aβ| = 1. **[5]**

f_1 = 10 kHz

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g) What is the phase margin ϕ_M? Indicate ϕ_M on your plot from (e). **[5]**

$\phi_M \cong 85°$

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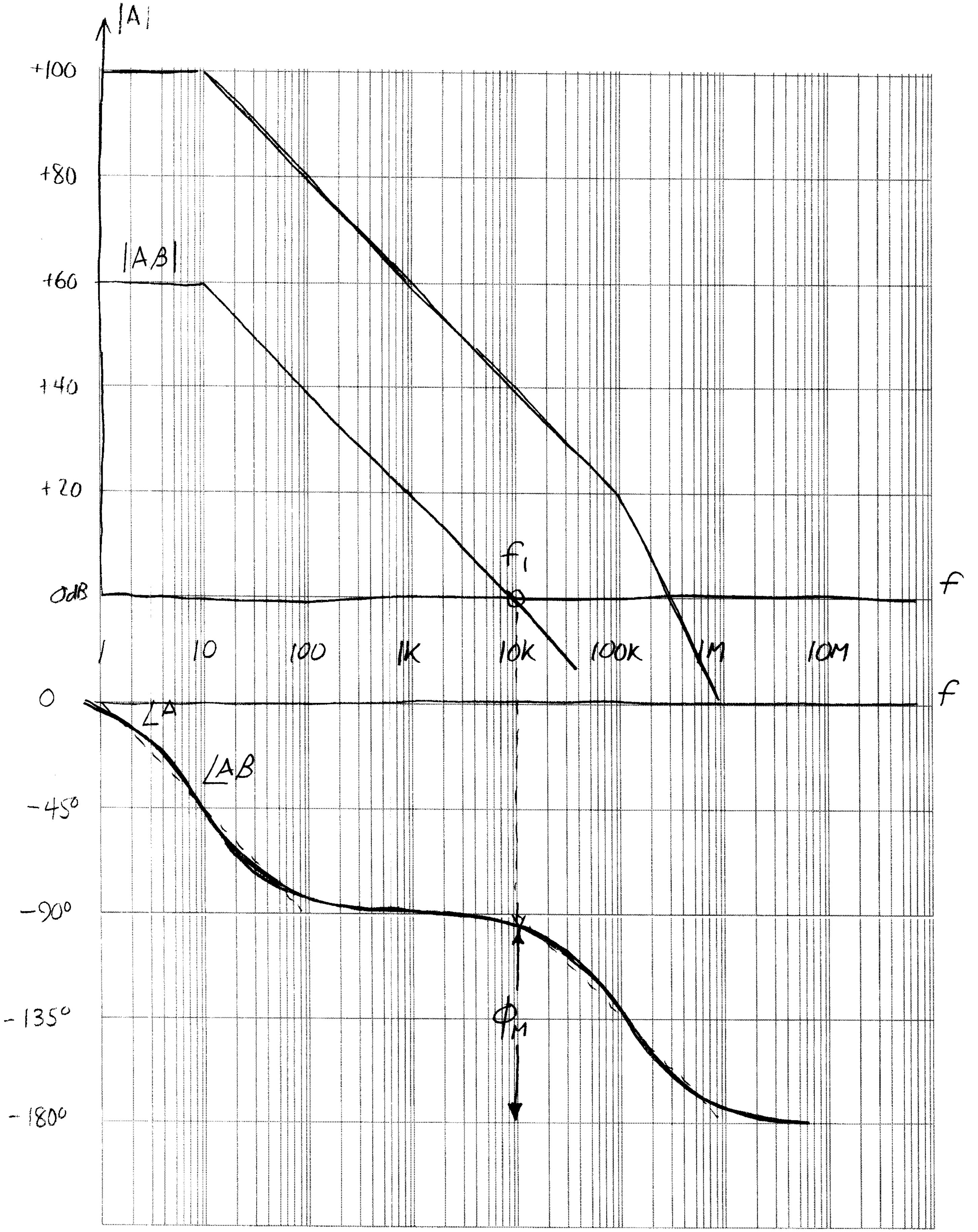
h) Is this circuit stable? Explain. **[5]**

STABLE — PHASE LAG OF ∠Aβ AT f_1 ~ −95° ; FAR FROM −180° OSCILLATION CRITERION



|A|
+100
+80
+60
+40
+20
0dB
|Aβ|
f₁
f
1
10
100
1K
10K
100K
1M
10M
0
∠A
∠Aβ
-45°
-90°
-135°
-180°
φM
f