Name _____

ECE Box # _____

Problem	Score	Points
1	_____	30
2	_____	30
3	_____	40

ECE3204 D2009

Microelectronics II

Exam 3

- This is a **closed book, closed notes test**! Use of calculators (no pre-stored formulas!) is allowed.
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- Look for the simple, straightforward way to solve the problem for the level of accuracy required. **Don't get entangled in unnecessary algebra**.
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- Unless otherwise indicated or implied, you may assume all op-amps to be ideal.
- You will have 55 minutes to complete this exam. There are three problems on a total of 7 pages.

1. In the sample-and-hold circuit shown on the opposite page, assume the MOSFET can be modeled as a switch with an "on" resistance of $r_{DS(on)} = 1k\Omega$. For parts (a) through (e), you may assume the op-amps to be ideal.

a) Is this an N-channel or P-channel MOSFET? (Circle one) **[1]**

N-CHANNEL P-CHANNEL

Explain! How do you know? **[4]**

For parts (b) and (c): A colleague suggests that op-amps "A" and "B" are not necessary, since as followers they only provide unity voltage gain.

b) What is the purpose of op-amp "A"? That is, how would sample-and-hold circuit performance be degraded if the signal source were connected directly to the MOSFET switch?

[5]

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c) What is the purpose of op-amp "B"? That is, how would sample-and-hold circuit performance be degraded if the hold capacitor C_H were connected directly to the load resistor R_L?

[5]

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d) Using the space on the opposite page, CAREFULLY sketch the capacitor voltage V_C as a function of time for $0 \le t \le 5\mu sec$. **[5]**

---

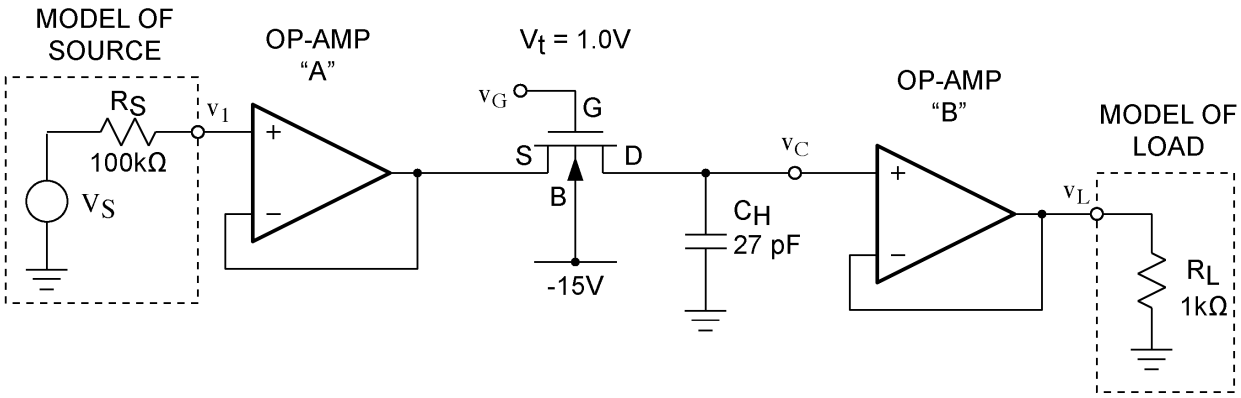
e) Find the acquisition time t_{ACQ} defined as the time from the MOSFET switch turning on until v_C has settled to within 1mV of its ideal final value (Accuracy ±10%)

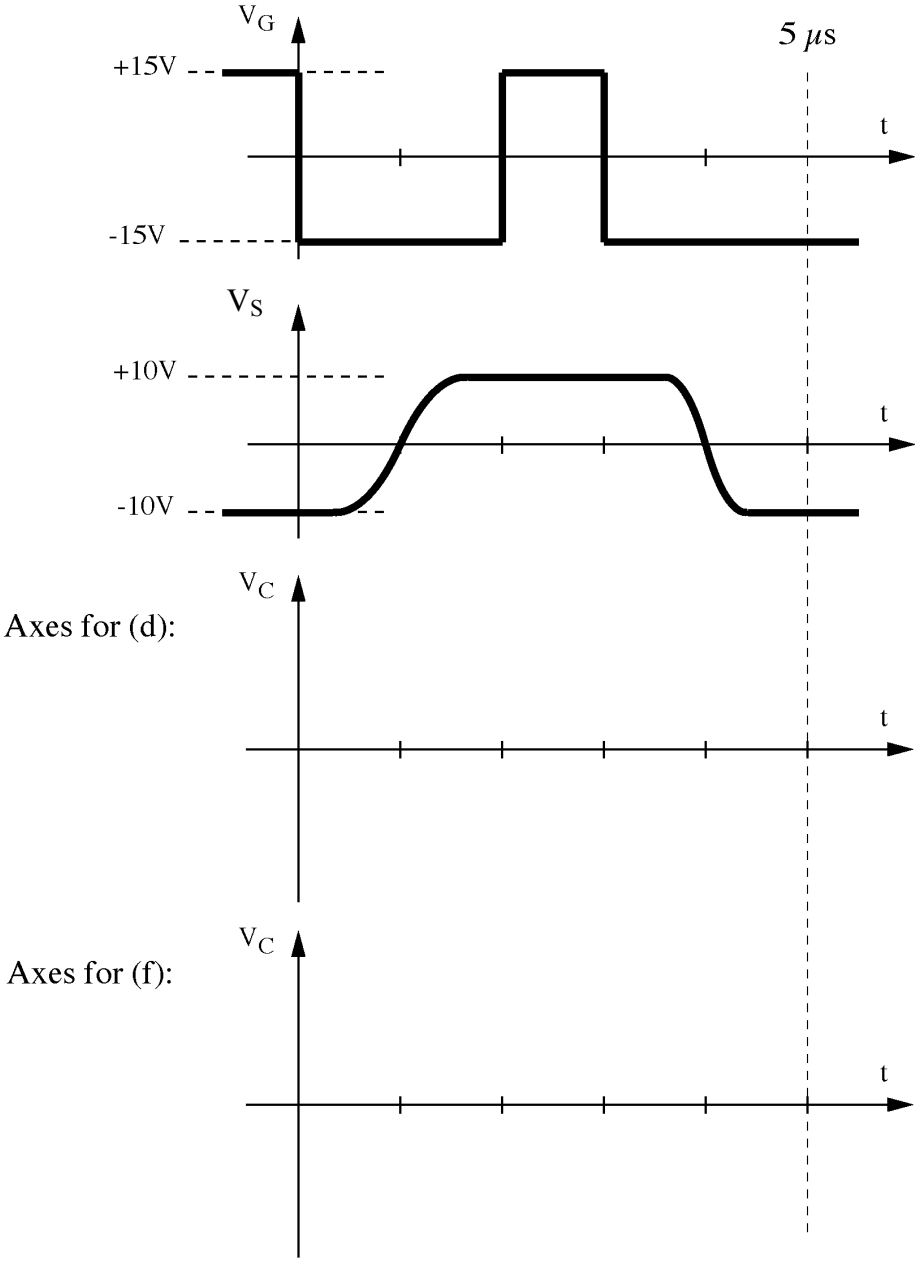
[5]

t_{ACQ} = _____

For part (f), assume the op-amps ideal except for an input bias current error of 10μA.

f) Using the space on the opposite page, CAREFULLY sketch the capacitor voltage V_C as a function of time for $0 \le t \le 5\mu sec$. Include any effects that may be due to the input bias current error of 10μA. **[5]**


MODEL OF SOURCE
OP-AMP "A"
V_t = 1.0V
OP-AMP "B"
MODEL OF LOAD
R_S
100kΩ
V_S
v_1
v_G
G
S
D
B
-15V
v_C
C_H
27 pF
v_L
R_L
1kΩ


V_G
+15V
-15V
t
5 μs
V_S
+10V
-10V
t
V_C
Axes for (d):
t
V_C
Axes for (f):
t

2. At the top of the following page are six s-plane pole-zero plots, designated A - F:

Following are qualitative descriptions of various circuit functions. For each description, indicate ALL pole-zero plots which could correspond to the transfer function of the circuit being described. NOTE:

- Each plot A-F may be used any number of times: once, more than once, or not at all.
- Some descriptions may correspond to more than one plot. You need to give all of the correct plots to receive full credit.

a) Plot of open-loop gain for an op-amp that is unity gain stable.

[4]

PLOT(S): _____

---

b) A sine wave oscillator with constant output amplitude..

[4]

PLOT(S): _____

---

c) A closed-loop op-amp. At the frequency where $|A\beta| = 1$, the phase shift $\angle A\beta = -225°$.

[4]

PLOT(S): _____

---

d) A Butterworth low-pass filter.

[4]

PLOT(S): _____

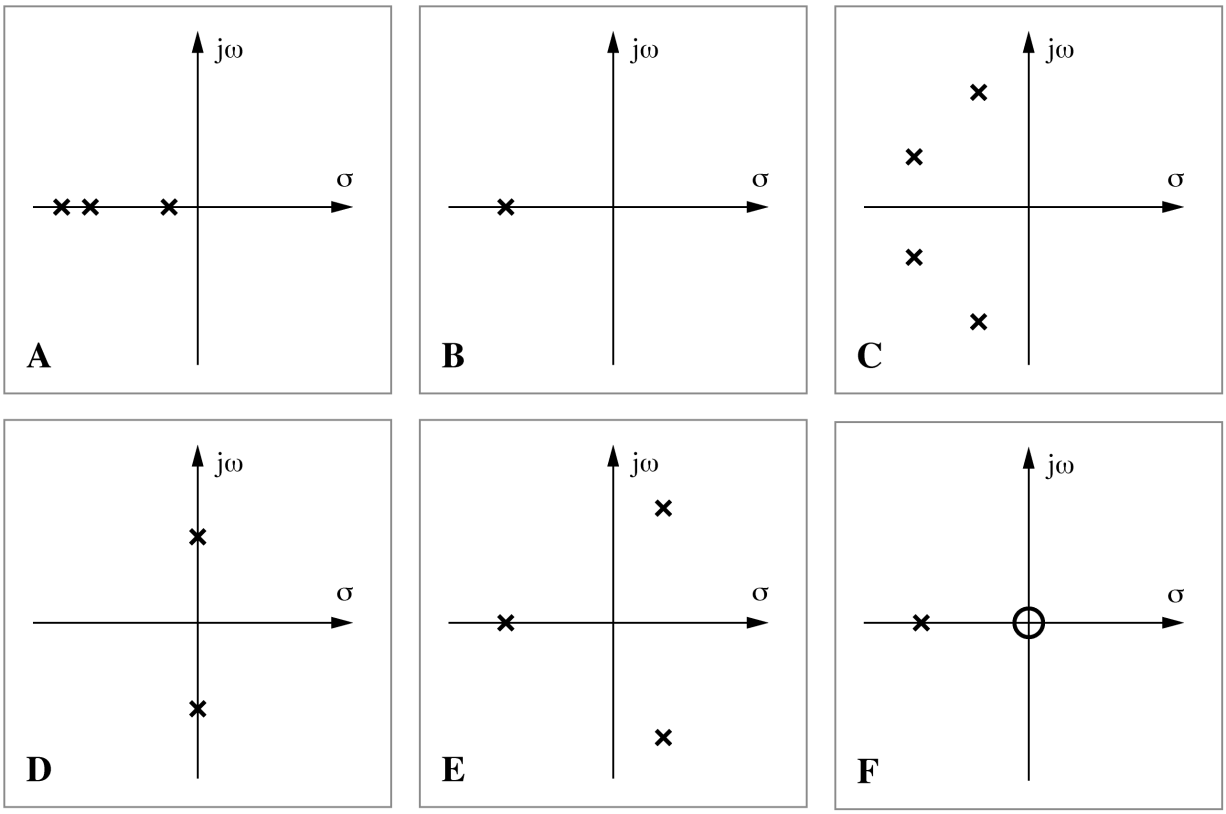
What order filter? Indicate the filter bandwidth on the s-plane plot(s)

---

e) A highpass filter with zero transmission at DC ($|T(0)| = 0$).

[4]

PLOT(S): _____



f) In the space below, write a transfer function T(s) for any one of the s-plane plots shown above and design a circuit to implement the transfer function. Your choice, just indicate the letter of the plot in the box. Numerical values required, accuracy ±10%. Choose wisely! No extra credit for complicated circuits that do not implement the s-plane plot and/or transfer function you choose!

[10]

Plot: ☐ Transfer function: T(s) = _____

Circuit design:

3. An op-amp has an open-loop DC gain of 10^5 = 100,000 and two poles: one at 10Hz, and one at 100kHz.

a) Determine the expression for A(s), the op-amp open-loop gain transfer function.

[5]

A(s) = _____

---

b) Using the space on the opposite page, carefully sketch the magnitude and phase Bode plots |A(f)| and ∠A(f) for the op-amp open-loop gain. Or, if you prefer, |A(ω)| and ∠A(ω). **[5]**

Now consider this op-amp connected closed loop with a noninverting gain of +100.

c) Sketch the circuit configuration:

[5]

---

d) Determine the numerical value of the feedback factor β, the fraction of the op-amp output that is fed back to the op-amp inverting input.

[5]

β = _____

---

e) Using the space on the opposite page, carefully sketch the magnitude and phase Bode plots |Aβ| and ∠Aβ for the loop gain. **[5]**

---

f) Using your plot from (e), determine the frequency f_1 at which the magnitude of the loop gain is equal to unity: when |Aβ| = 1. **[5]**

f_1 = _____

---

g) What is the phase margin ϕ_M? Indicate ϕ_M on your plot from (e). **[5]**

ϕ_M = _____

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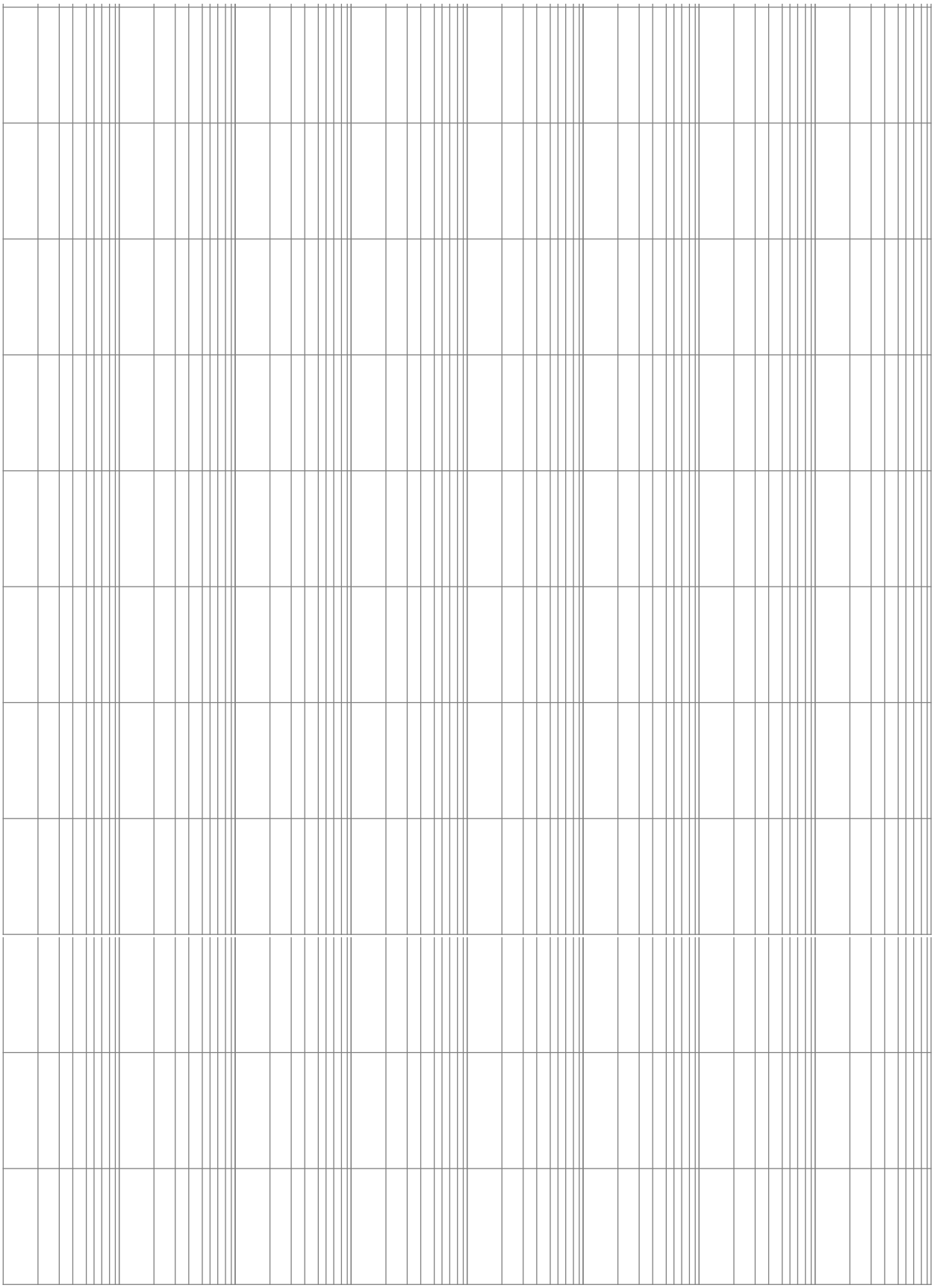
h) Is this circuit stable? Explain.

[5]