A	85-100
B	70 - 84
C	50 - 69

μ 73.3

σ 16.8

MED 76

Name SOLUTIONS

ECE Box # ____________

Problem	Average Score	Points
1	22.7	30
2	11.1	20
3	15.8	20
4	23.7	30

ECE3204 D2015

Microelectronics II

Exam 3
May 5, 2015

- This is a **closed book, closed notes test**! Use of calculators is allowed. No pre-stored formulas or outside resource access!
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- Look for the simple, straightforward way to solve the problem for the level of accuracy required. **Don't get entangled in unnecessary algebra**.
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- Unless otherwise indicated or implied, you may assume all op-amps to be ideal.
- You will have 55 minutes to complete this exam. There are four problems on a total of 9 pages.

1. Following are six circuit descriptions, designated A - F:

A) Wien bridge oscillator with constant output amplitude.
B) Active bandpass filter with +32dB of gain in passband
C) Fourth-order Butterworth lowpass filter
D) Lowpass filter formed by cascading two STC lowpass circuits
E) Band-reject filter
F) The open-loop gain of an LM741 op-amp.

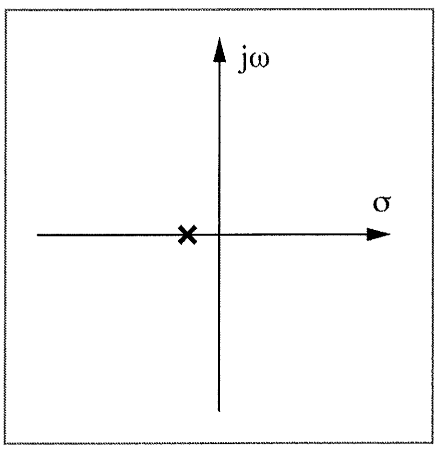
For each of the s-plane pole/zero or magnitude $|v_{out}/v_{in}|$ Bode plots below and on the opposite page, write in the letter of the corresponding circuit description. Then "fill in the blank" by sketching the corresponding s-plane pole/zero plot or magnitude $|v_{out}/v_{in}|$ Bode plot (whichever is missing). Notes:

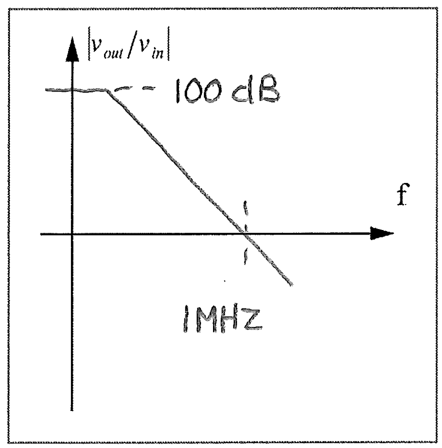
- Each description may be used once, more than once, or not at all.
- Some plots may correspond to more than one description; in that case, any correct answer is OK
- In the case of an oscillator, you need not fill in a Bode plot since there is no input v_{in}.

[30]

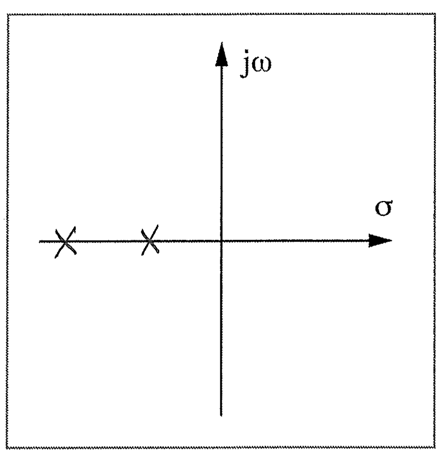
DESCRIPTION | s-PLANE PLOT | MAGNITUDE BODE PLOT

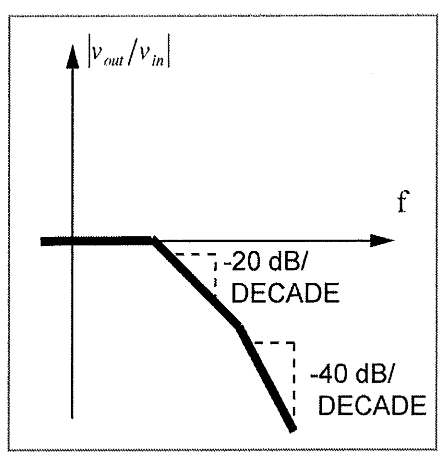
F

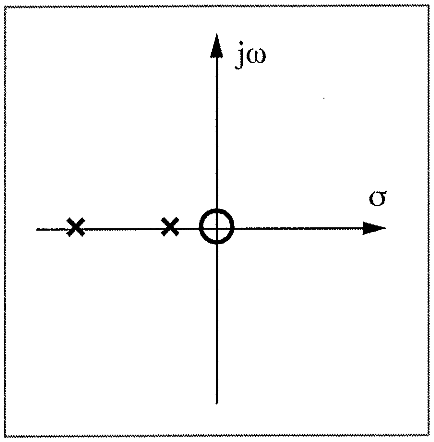
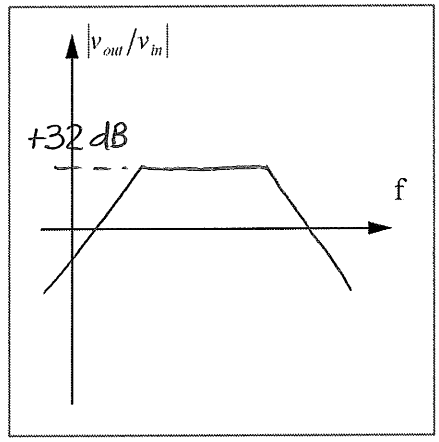
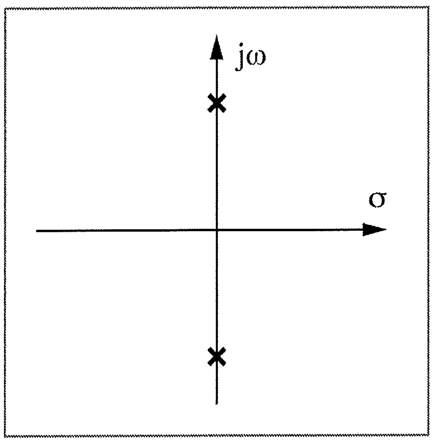
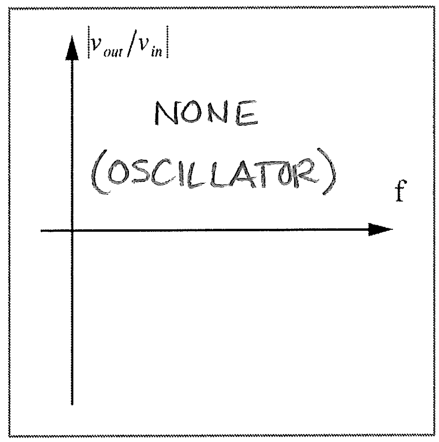
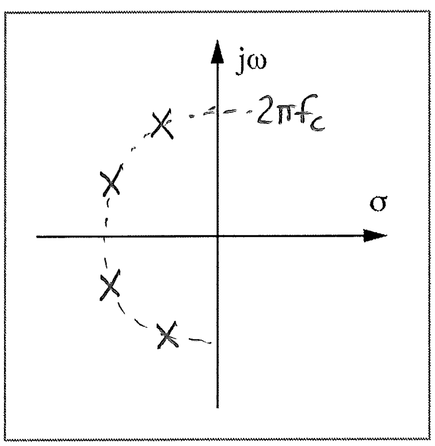
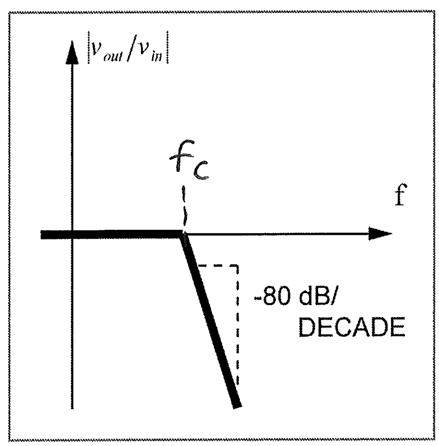




D





DESCRIPTION	s-PLANE PLOT	MAGNITUDE BODE PLOT
B		
A		
C		

2. The sample-and-hold circuit shown on the opposite page is used in a battery powered system with ±9V supply rails. Assume the MOSFET can be modeled as a switch with an "on" resistance of $r_{DS(on)} = 500\Omega$ for the gate drive condition shown. The MOSFET threshold voltage is $V_t = +1.0V$. Assume the MOSFET is "on" for all time $t < 0$.

a) Is this an N-channel or P-channel MOSFET? (Circle one) **[3]**

N-CHANNEL P-CHANNEL

---

b) Why is the B terminal of the MOSFET connected to -9V? What would go wrong if the B terminal were connected to ground instead? **[2]**

KEEP S-B, S-D JUNCTIONS REVERSE BIASED

---

c) Using the space on the opposite page, CAREFULLY sketch the capacitor voltage V_C as a function of time for $0 \le t \le 1$ μsec. **[5]**

---

d) What is the value of V_C at time t = 1 μsec? (Accuracy ±5mV) **[5]**

$V_C(t{=}1\mu sec) =$ -3.978 V

HELD VALUE AFTER 200 nsec OF EXPONENTIAL SETTLING FROM t'=0 WHEN NMOS TURNS ON

$V_C(t'=200nsec)$

$= -4V - (-8V)\, e^{-(200nsec/34nsec)}$

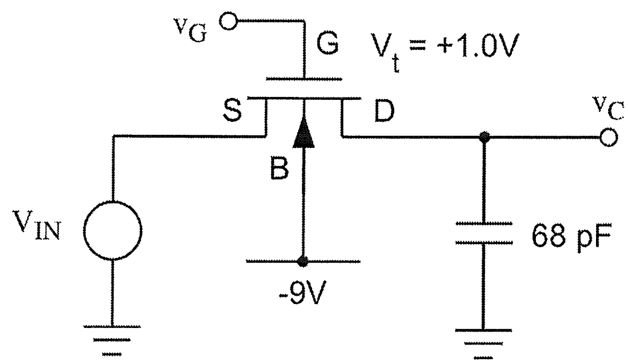
---

e) Find the acquisition time t_{ACQ} defined as the time that would be needed from the MOSFET switch turning on until v_C has settled to within 10mV of its ideal final value (Accuracy ±10%). Note that this requirement may or may not be met in the timing of the figure on the opposite page! **[5]**

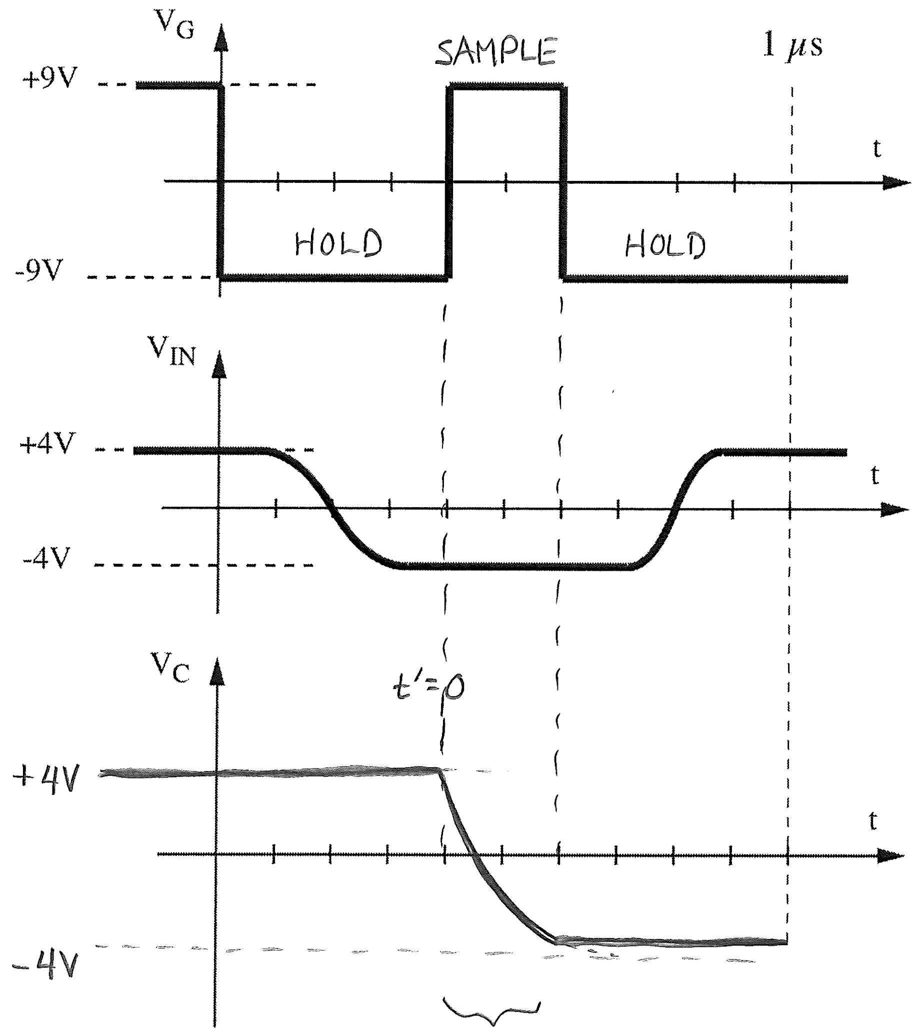
$t_{ACQ} =$ 227 nsec

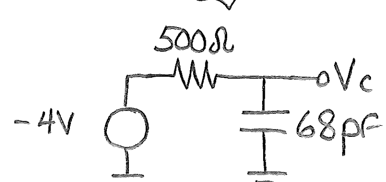
$\cancel{-4V} + 10mV = \cancel{-4V} + 8V\, e^{-t_{ACQ}/34nsec}$

$t_{ACQ} = 34nsec \, \ln\left(\frac{8V}{10mV}\right)$



Axes for (c):





$\tau = (500\Omega)(68pF)$

$= 34 nsec$

3. In the digital-to-analog converter (DAC) design for Lab 5, you had a choice between the R-2R ladder and binary-weighted resistor DAC. This problem involves designing YOUR CHOICE of ONE of these DACs to meet the input-output characteristic specified in Figure 3A on the opposite page. In this problem we require (as shown in Figure 3A) at V_{OUT} a positive-going characteristic from the input $CODE_{IN}$ binary number composed of bits $b_1b_2b_3b_4$.

To simplify the design process, you may assume the switches to be ideal.

---

a) First, determine the maximum output voltage V_{MAX} for this DAC characteristic (accuracy ±1%):

[5]

V_{MAX} = 3.0V $\quad (15\ \text{STEP})\left(\frac{0.2V}{\text{STEP}}\right)$

---

b) Now, choose ONE of the DAC circuits and specify the design by the required values:

[15]

If you choose the binary-weighted resistor DAC in Figure 3B, provide values for R_B and R_F to meet the following design constraints:

i) The LSB step size must be 0.2V

ii) For the voltage source connected to the switches, the maximum total current drawn i_{TOTAL} must not exceed 100 μA. → $R_B \geq \frac{5V}{100\mu A} = 50\ k\Omega$

LSB STEP:

$5V \frac{R_F}{400K} = 0.2V$

R_B = 50kΩ $\qquad R_F$ = 16kΩ

$(0.32)R_B$

$R_F = 400K\left(\frac{0.2V}{5V}\right)$

$= 16\ k\Omega$

-- OR --

If you choose the R-2R ladder DAC in Figure 3C, provide values for R and V_{REF} to meet the following design constraints:

i) The LSB step size must be 0.2V

ii) The Thevenin equivalent output resistance R_{out} seen at the output terminal should be 10kΩ.

R = 10 kΩ $\qquad V_{REF}$ = 3.2V

Figure 3A

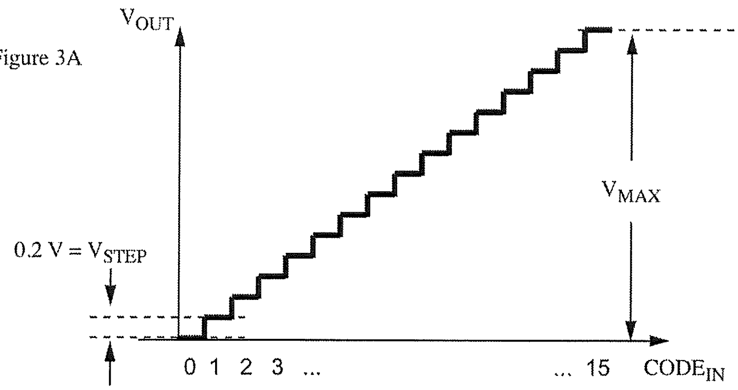


Figure 3B: Binary Weighted R DAC

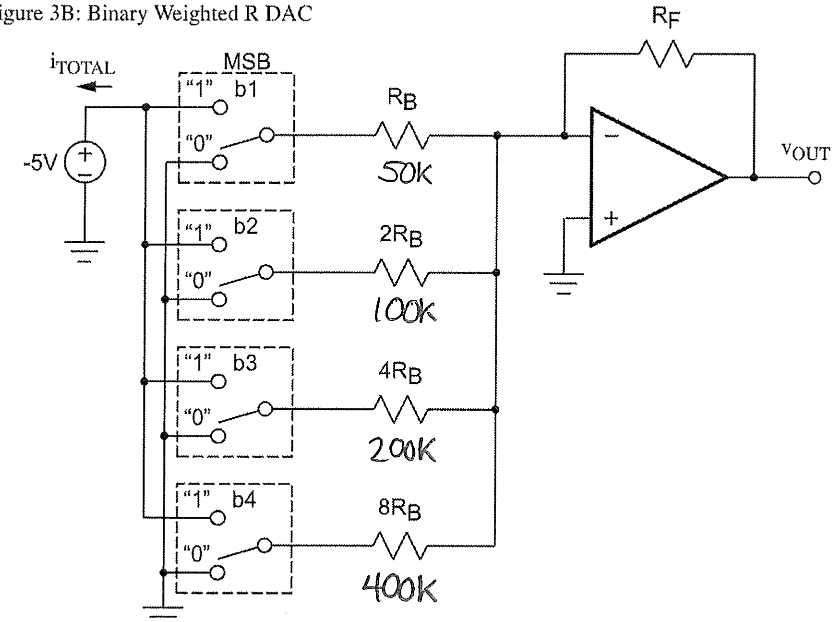
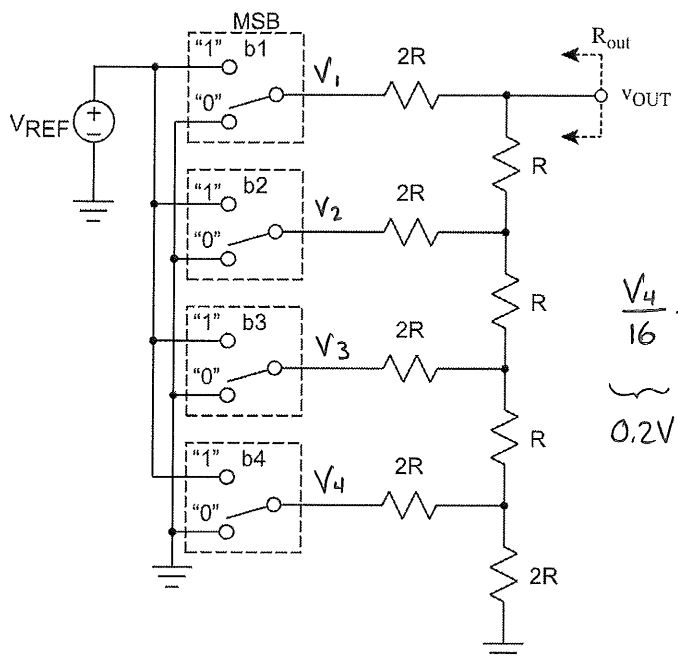
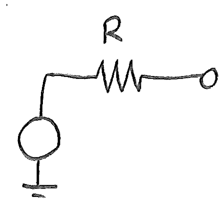


Figure 3C: R-2R Ladder DAC



THEVENIN EQUIVALENT



$$\underbrace{\frac{V_4}{16}}_{0.2V} + \frac{V_3}{8} + \frac{V_2}{4} + \frac{V_1}{2}$$

$$0.2V \Rightarrow V_{REF} = 16(0.2) = 3.2V$$

4. You and a colleague are working on a design for an application in which an op-amp must drive an electrostatic actuator which can be modeled as a load capacitance of $C_L = 2200\text{pF}$. Your colleague proposes the design shown on the opposite page, which incorporates two potential improvements over a simple op-amp follower:

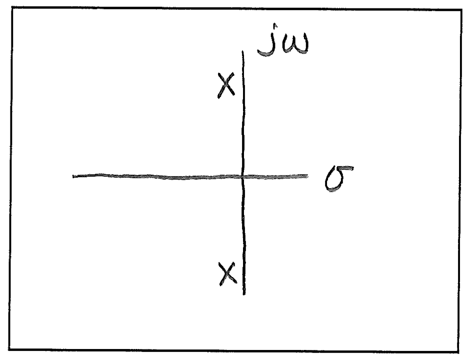
- A resistor $R_S = 10\text{k}\Omega$ is included in series with the load to form a lowpass filter, with the intention of filtering out high-frequency noise
- Feedback is taken from the voltage v_L at the capacitor load, rather than the op-amp output, with the intention of improving accuracy

Your colleague builds the circuit in the lab using an LM741, with DC gain A_0=+100dB and unity gain frequency f_T = 1MHz. You test the step response of the circuit using a square wave input and observe the scope photo shown on the opposite page. Your colleague is mystified and seeks an explanation!

a) Using the adjacent space, sketch the approximate location in the s-plane of the poles of the closed loop transfer function of v_L/v_{IN}.

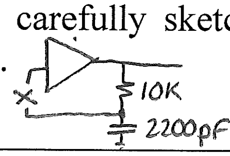
No numerical values are required, just qualitatively correct locations.

[5]



b) Using the space on the opposite page, carefully sketch the magnitude and phase of the loop gain Aβ for this circuit.

β: LOWPASS



f_B = 7 KHz **[8]**

c) From your plot for (b), determine the frequency f_1 at which the magnitude of the loop gain is equal to unity: when $|A\beta| = 1$.

[6]

f_1 = 80 KHz

d) What is the phase margin ϕ_M? Indicate ϕ_M on your plot from (b).

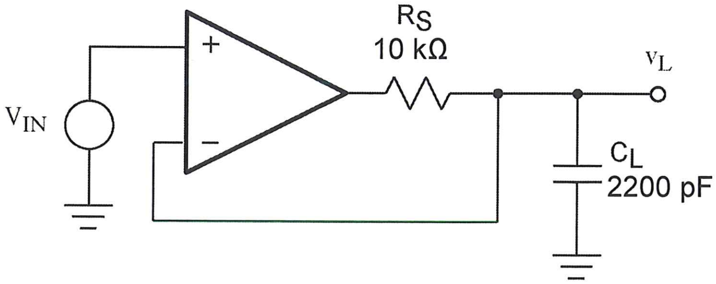
[6]

$\phi_M \cong 5°$

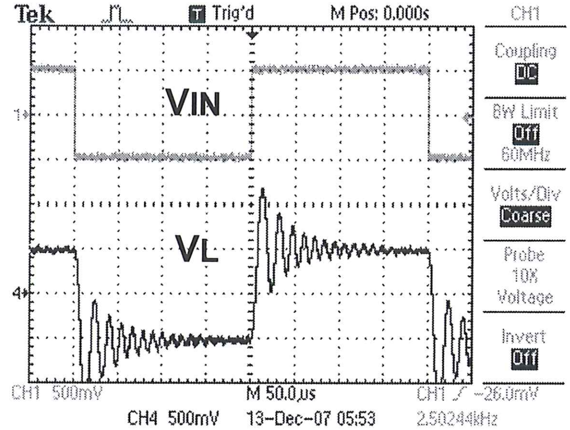
e) Is this circuit stable? Explain.

MARGINALLY STABLE / UNSTABLE: OVERSHOOT AND RINGING IN STEP RESPONSE **[5]**

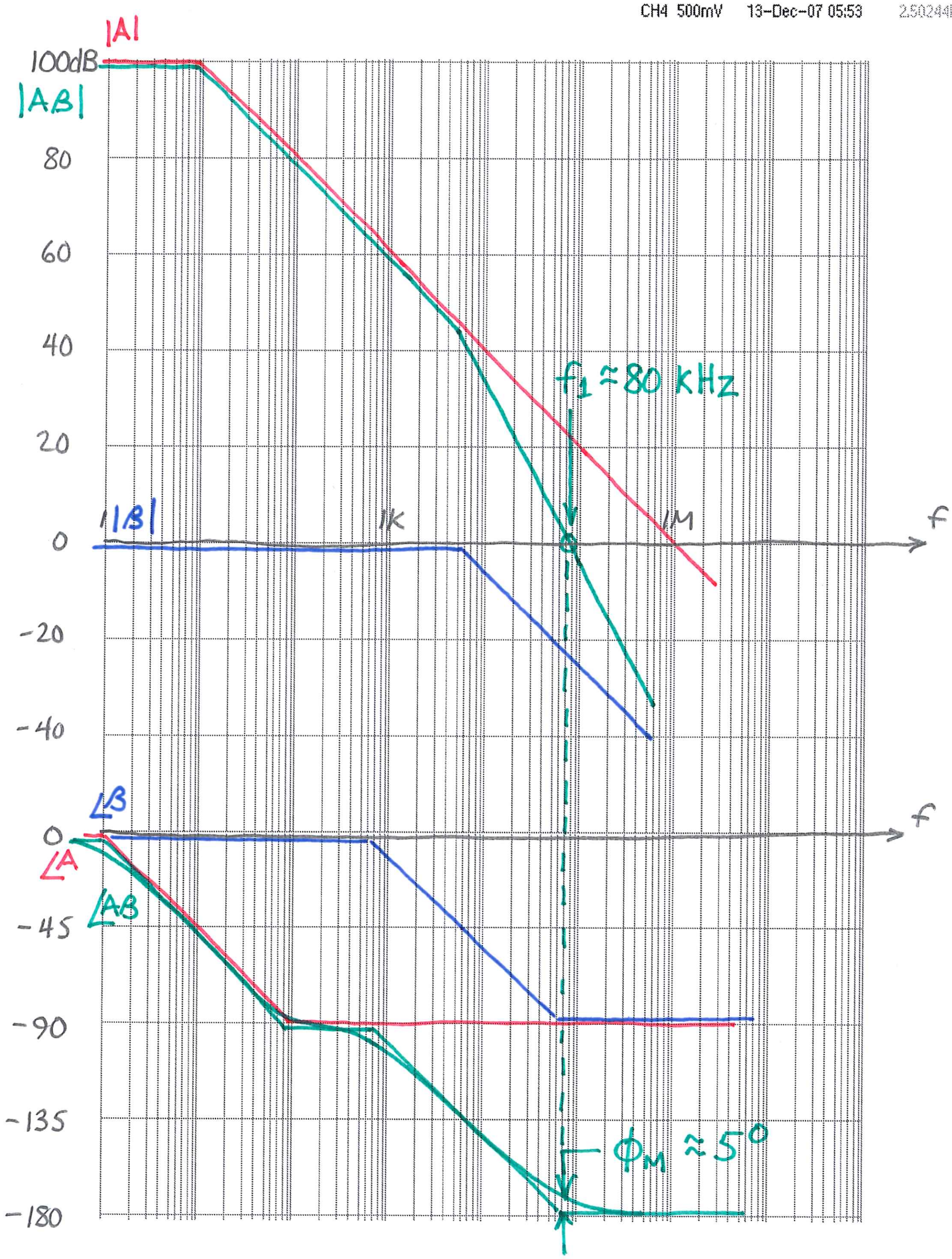
(TECHNICALLY STABLE IN BOUNDED INPUT → BOUNDED OUTPUT SENSE)



V_{IN}
+
−
R_S
10 kΩ
v_L
C_L
2200 pF



Tek
Trig'd
M Pos: 0.000s
VIN
VL
CH1 500mV
M 50.0µs
CH4 500mV
13-Dec-07 05:53
CH1 ∫ -26.0mV
2.50244kHz
CH1
Coupling
DC
BW Limit
Off
60MHz
Volts/Div
Coarse
Probe
10X
Voltage
Invert
Off



|A|
100dB
|AB|
80
60
40
20
0
-20
-40
|B|
1
1k
1M
f
$f_1 \approx 80$ kHz
∠B
∠A
∠AB
-45
-90
-135
-180
$\phi_M \approx 5^\circ$