

A	76-100
B	60-75
C	46-59

Name SOLUTIONS

ECE Box # \_\_\_\_\_

$\mu$  61.6  
 $\sigma$  16.4  
 MED 63

Problem	Score	Points
1	<u>25.0</u>	30
2	<u>12.7</u>	25
3	<u>13.9</u>	25
4	<u>10.0</u>	20

ECE3204 D2015

Microelectronics II

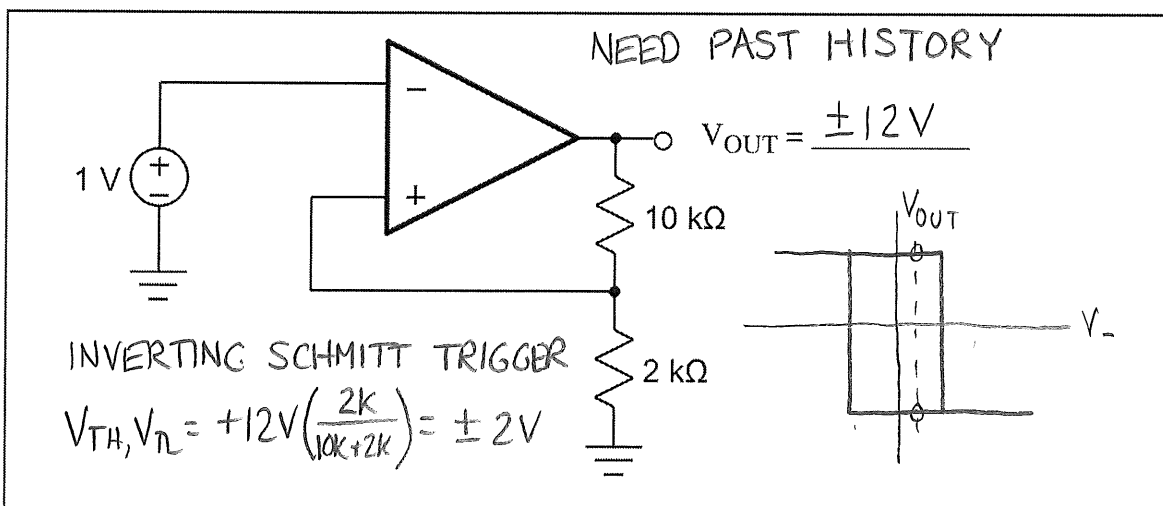
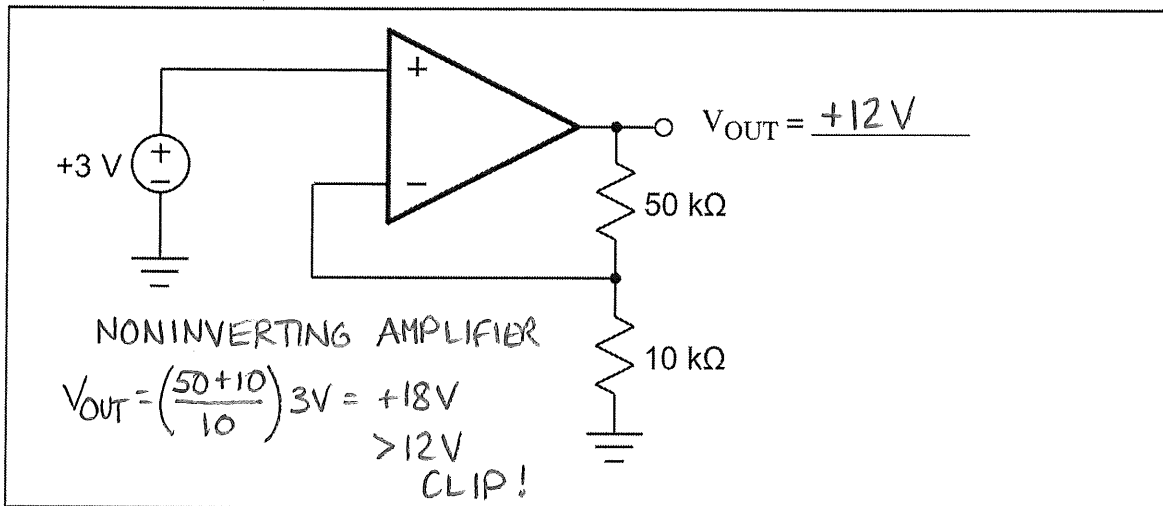
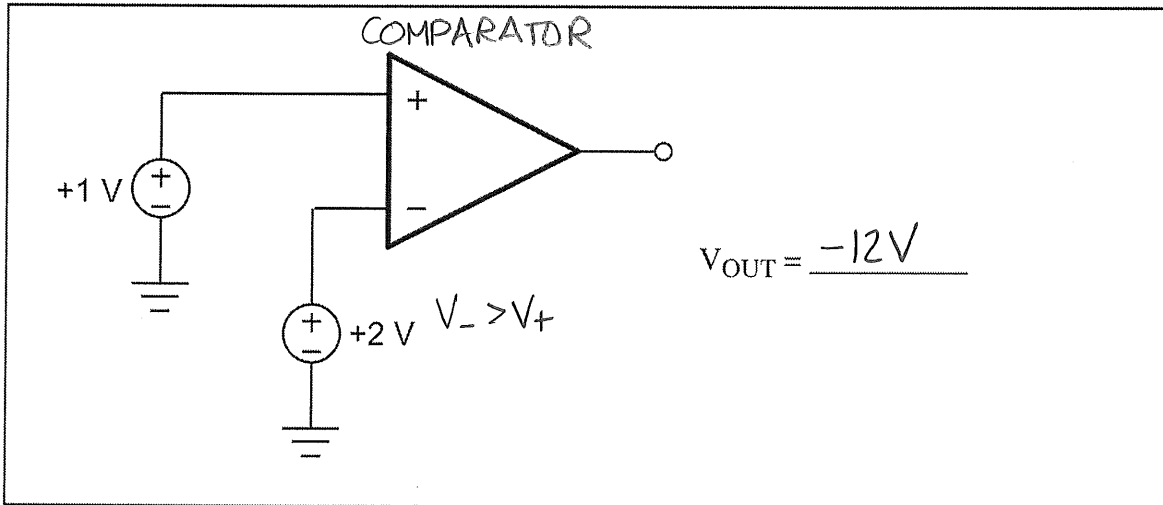
Exam 2

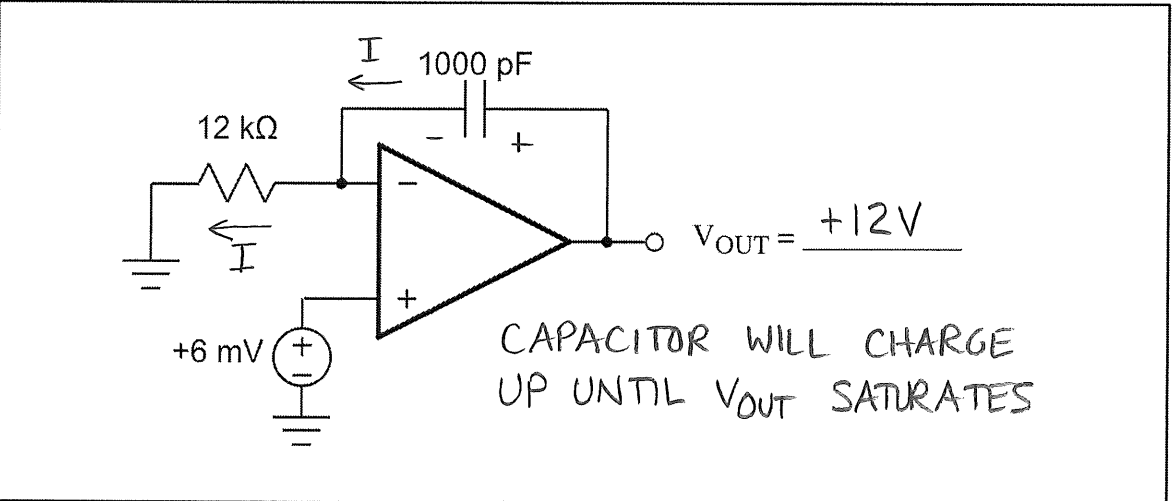
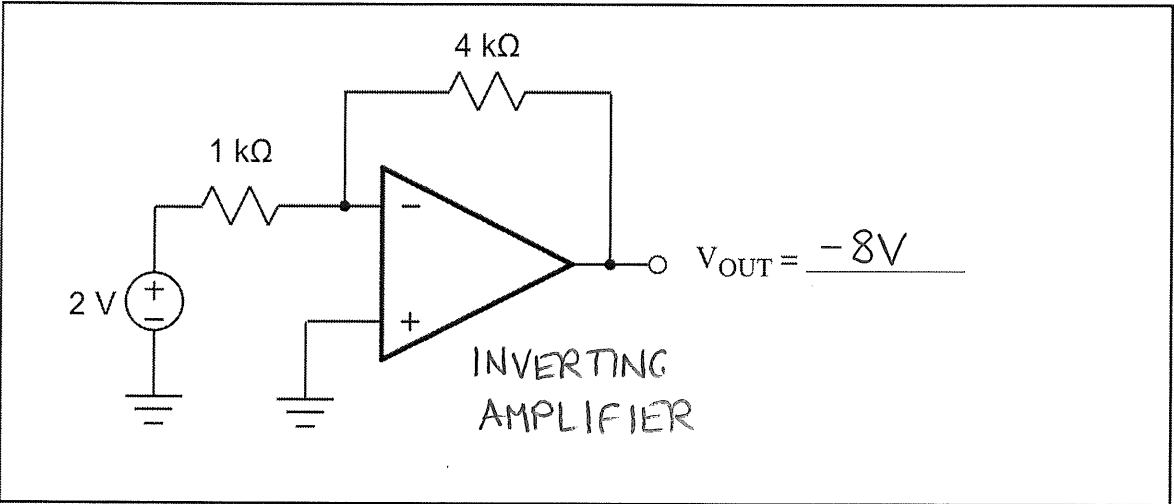
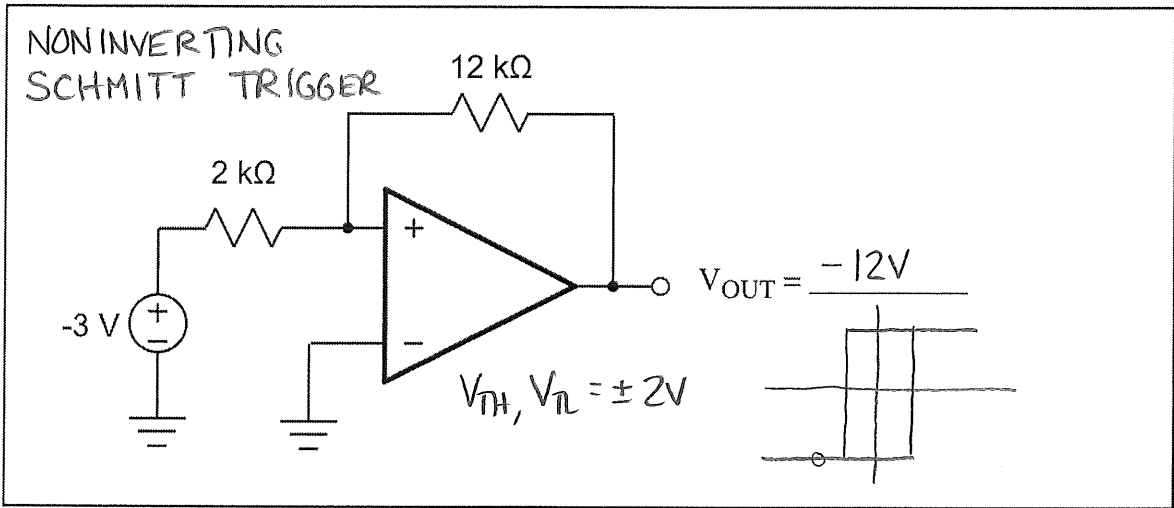
April 21, 2015

- This is a **closed book, closed notes test!** Use of calculators is allowed. No pre-stored formulas or outside resource access!
- Show **all** your work. Partial credit may be given. If you think you need something that you can't remember, write down what you need and what you'd do if you remembered it.
- Look for the simple, straightforward way to solve the problem for the level of accuracy required. **Don't get entangled in unnecessary algebra.**
- As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
- Unless otherwise indicated or implied, you may assume all op-amps to be ideal.
- You will have 55 minutes to complete this exam. There are four problems on a total of 9 pages.

1. For each of the following circuits, find (if possible) the DC output voltage. If it is not possible to determine a voltage, indicate what the possible voltages are and what kind of information you would need to know to determine the voltage. Assume op-amps ideal except for an output voltage limit of  $\pm 12V$ .

[30]





2. This problem is concerned with the timer circuit shown on the opposite page. This is a single-power-supply automotive environment with a +12V battery power supply. You may assume the op-amps shown to be ideal except for output swing limits of 0V and +12V.

For time  $t < 0$  a switch shorts the integrating capacitor C. At time  $t = 0$  the switch across the integrating capacitor C is opened.

- a) On the axes provided, sketch  $V_{COMP}$ ,  $V_{INT}$ , and  $V_{OUT}$  for the time range  $-10\mu s < t < +30\mu s$ . Be sure to indicate any interesting times and voltage levels on your plot.

$$I_R = \frac{3V}{50k\Omega} = 60\mu A \quad [1] \quad \left. \begin{array}{l} \text{WHEN SWITCH} \\ \text{OPENS, CAP} \\ \text{WILL INTEGRATE } I_R \end{array} \right\} \begin{array}{l} \text{KVL} \\ V_{INT} = 3V + V_C \\ \frac{1}{C} \int I dt \\ = 3V + \frac{60\mu A}{180pF} t = 3V + \left(3.33E+5 \frac{V}{sec}\right) t \quad [2] \end{array} \quad [12]$$

- b) At what time  $t_p$  does the logic level of  $V_{OUT}$  change state?

[8]

$$t_p = \underline{18\mu s}$$

COMPARATOR CHANGES STATE WHEN  $V_- = V_+$

$$3V + \left(3.33E+5 \frac{V}{sec}\right) t_p = +9V \quad [3]$$

$$t_p = \frac{9V - 3V}{3.33E+5} = 18\mu s$$

- c) As the battery charges and discharges, the +12V supply voltage will change. Suppose the supply voltage increases to +14V. Will  $t_p$  decrease, remain the same, or increase? (Circle one)

DECREASE

REMAIN  
THE SAME

INCREASE

[5]

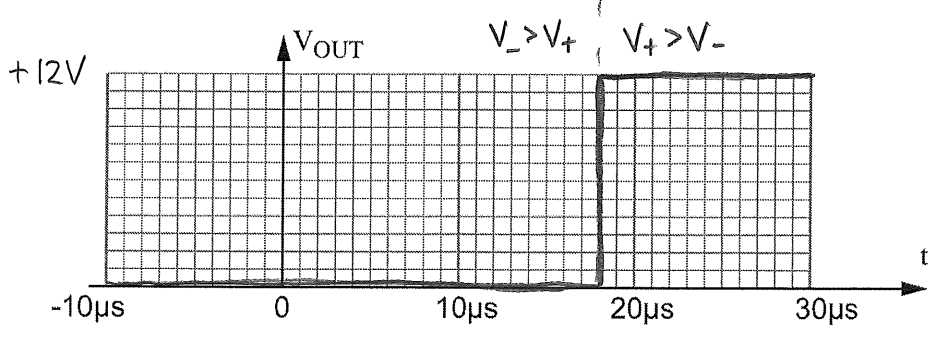
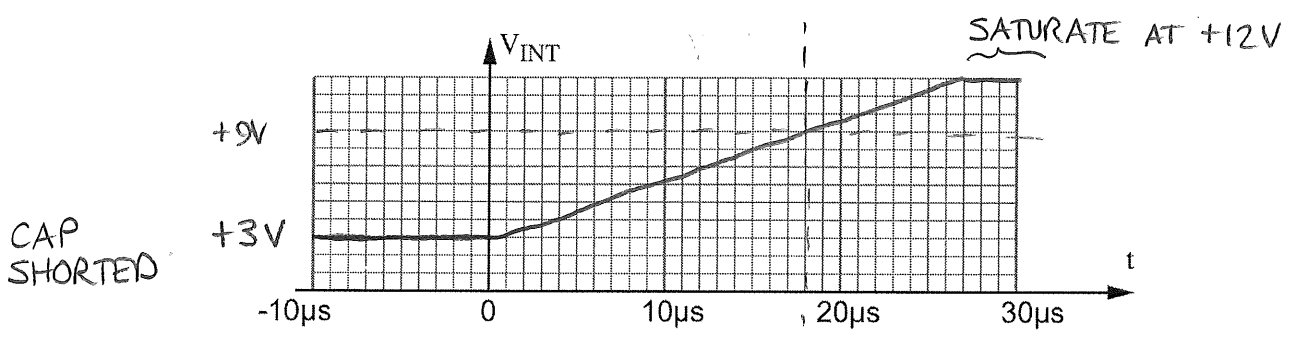
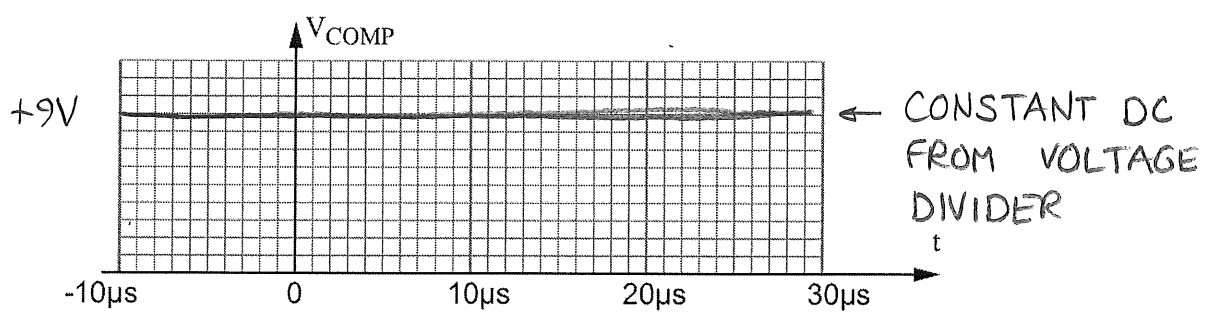
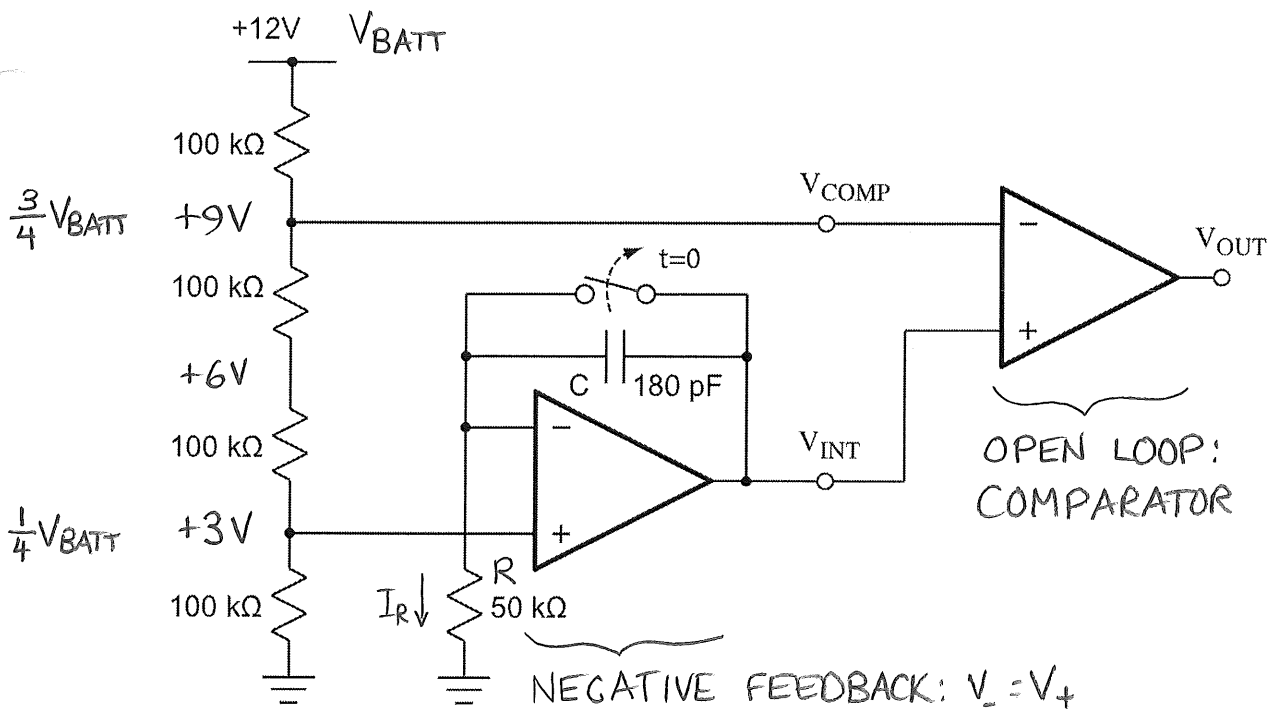
EXPLAIN YOUR ANSWER! IN TERMS OF  $V_{BATT}$ , CONDITION FOR  $t_p$

$$I_R = \frac{V_{BATT}/4}{R} \quad [1]$$

$$V_{INT} = \frac{V_{BATT}}{4} + \frac{V_{BATT}/4}{RC} t \quad [2]$$

$$\frac{V_{BATT}}{4} + \frac{V_{BATT}}{4RC} t_p = \frac{3}{4} V_{BATT}$$

$$[3] \quad V_{BATT} \text{ CANCELS} \\ t_p = 2RC$$



3. This problem involves design of a first order active lowpass filter circuit using the topology shown on the opposite page. You are to choose values for R1, R2 and C to achieve a transfer function  $v_{out}/v_{in}$  with the magnitude Bode plot shown, and an input resistance of  $1k\Omega$  as seen by the signal source. For part (a), assume the op-amp to be ideal.
- a) Choose R1, R2 and C to achieve the indicated transfer function and input resistance. Nonstandard value OK.

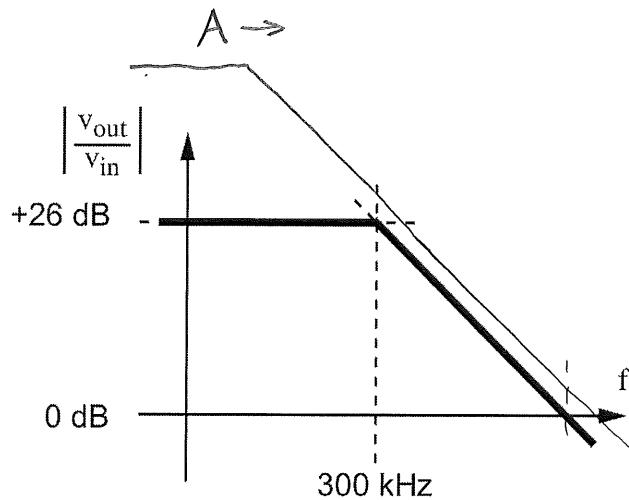
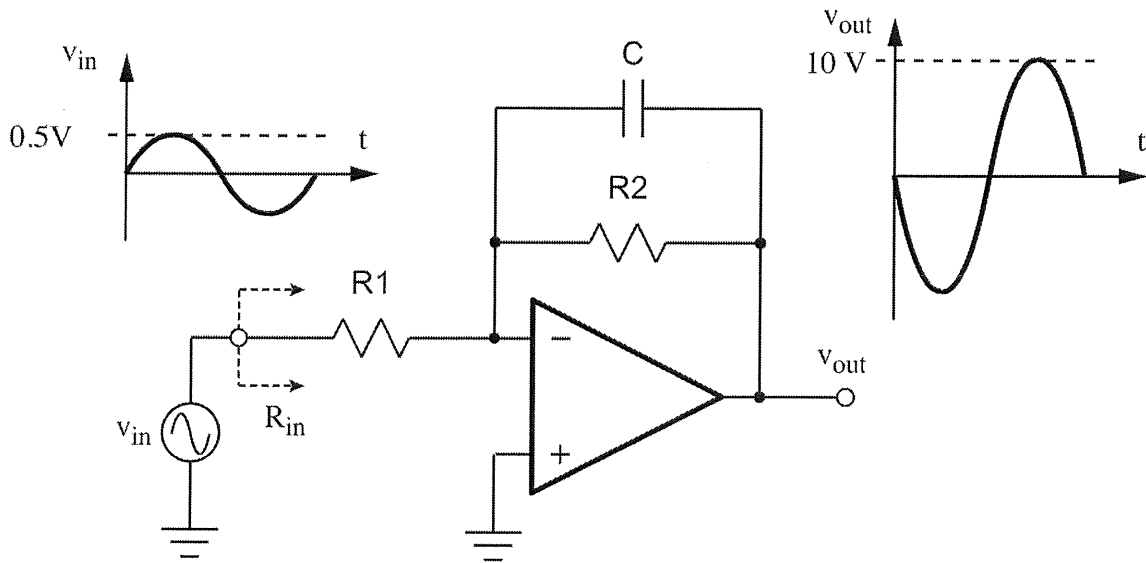
$$R1 = \frac{1k\Omega}{R_{IN}} \quad R2 = \frac{20k\Omega}{GAIN=20} \quad C = \frac{26.5 pF}{\frac{1}{2\pi(20k\Omega)C} = 300 KHz} \quad [15]$$

- b) In this part we drop the ideal op-amp assumption, and consider dynamic specifications. The op-amp will be operated with supply voltages high enough so that voltage clipping at  $v_{OUT}$  will not be a problem. We will also assume that DC errors (offset voltage, bias current) are negligible. In addition to the constraints from (a) that determined your choice of R1, R2, and C, the other requirements for the design are as follows:
- i) Bandwidth limited by feedback component values (R1, R2, C) and not by unity gain frequency  $f_T$
- ii) No slew rate limiting at  $v_{OUT}$  over the transfer function frequency range

For each of the specifications in the following table, fill in the correct minimum allowable value to meet requirements (i) and (ii).

[10]

Specification		Min	Max	Unit
Unity gain frequency	$f_T$	6.3	X	MHz
Slew rate limit	SR	18.9	X	V/ $\mu$ s



IF BANDWIDTH WERE 300 KHz FROM GAIN-BW PRODUCT

$$\frac{1}{21} f_T > 300 \text{ kHz} \Rightarrow f_T > 6.3 \text{ MHz}$$

WORST CASE SLEW RATE 300 KHz

$$\left. \frac{dv}{dt} \right|_{\text{MAX}} = 10 \text{ V } 2\pi \cdot 300 \text{ kHz}$$

$$= 18.9 \frac{\text{V}}{\mu\text{s}}$$

ALSO OK IF USING 3dB DOWN AT 300KHz

$$7.07 \cdot 2\pi (300 \text{ kHz}) = 13.3 \text{ V}/\mu\text{s}$$

4. The first task you are assigned on your summer internship is design of the amplifier / "level shifter" circuit shown on the opposite page. The input is a 1V peak audio signal, which swings above and below ground as shown. The output will be applied to an analog-to-digital converter (ADC) in a single-power-supply microprocessor system; the output swing must stay inside the ADC input range of 0V to +5V as shown. The circuit must both
- amplify the signal so the 2V pk-pk input swing becomes a 5V pk-pk output swing, and
  - shift its DC level so 0V at the input is shifted to +2.5V at the output.

The signal inversion is OK since the ADC digital output can be easily inverted in software).

- a) Find the required numerical values of feedback resistor  $R_F$  and bias voltage  $V_B$ . Nonstandard values OK.

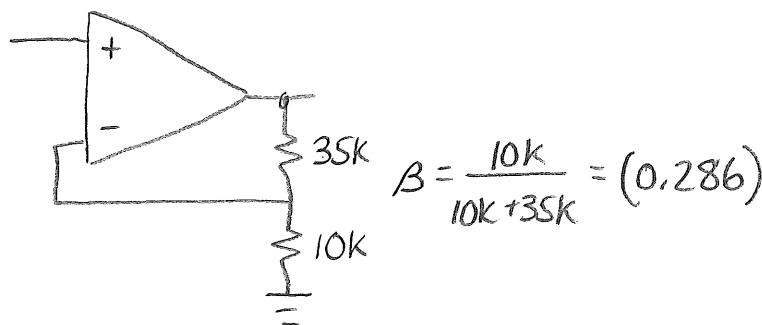
$$R_F = \underline{25 \text{ k}\Omega} \quad V_B = \underline{0.714 \text{ V}} \quad [14]$$

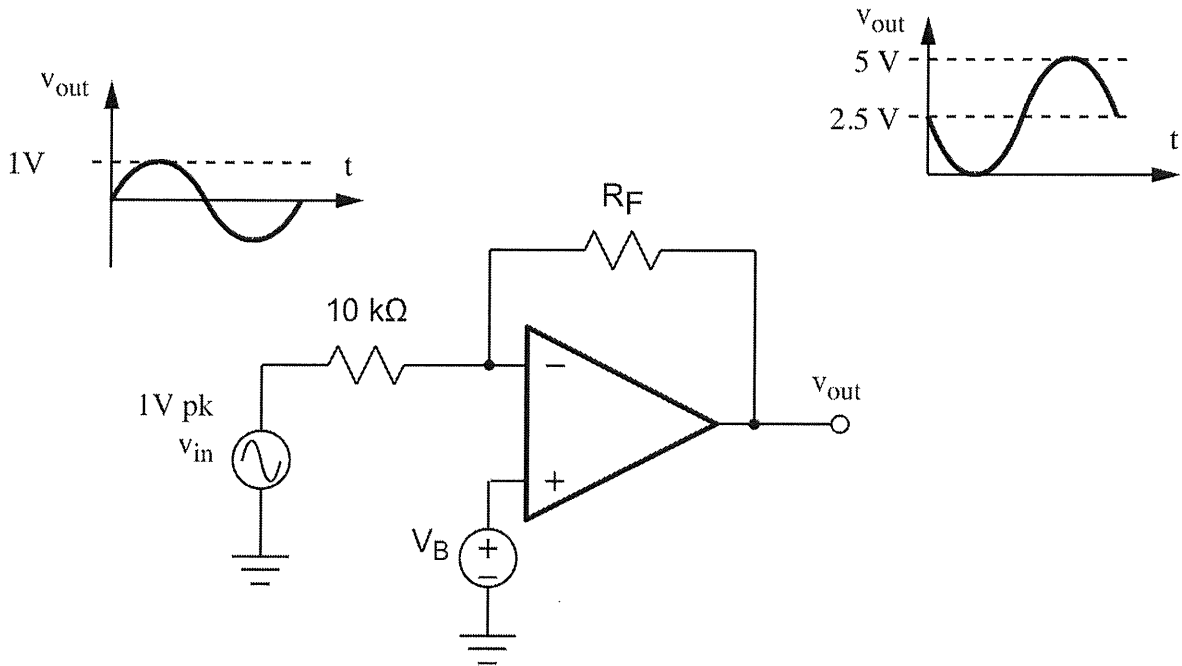
Your design is built with an LM741 op-amp with gain-bandwidth product (unity gain frequency)  $f_T = 1\text{MHz}$ .

- b) Determine the resulting closed loop 3dB bandwidth  $f_{3\text{dB}}$ .

$$f_{3\text{dB}} = \underline{286 \text{ kHz}} \quad [6]$$

SHOW FEEDBACK FACTOR





### SUPERPOSITION

$$V_{OUT} = \underbrace{V_B \left( \frac{R_F + 10k}{10k} \right)}_{2.5V \text{ (DC LEVEL SHIFT)}} + \underbrace{V_{in} \left( \frac{-R_F}{10k} \right)}_{2.5 \text{ (GAIN REQUIREMENT)}}$$

$$2.5V = V_B \left( \frac{25k + 10k}{10k} \right) \quad \Leftarrow \quad \underline{R_F = 25k\Omega}$$

$$V_B = 0.714 V$$