Project Notes:

Project Title:
Name: DANIEL HARN

Note Well: There are NO SHORT-cuts to reading journal articles and taking notes from them. Comprehension is paramount. You will most likely need to read it several times, so set aside enough time in your schedule.

Contents:

Knowledge Gaps: 1

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Article #1 Notes: Title 3

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Article #1 Notes: Title **Error! Bookmark not defined.**

Commented [1]: remember to share with Dr. C.

Commented [2]: Table of contents will be generated if using a HEADER format for each sub-section.

KEEPING THIS UP-TO-DATE WILL HELP YOU when it comes time to write your thesis.

Knowledge Gaps:

This list provides a brief overview of the major knowledge gaps for this project, how they were resolved and where to find the information.

Knowledge Gap	Resolved By	Information is located	Date resolved
Why IR is the best use of light for finding voids			
How does the location of voids correlate to what happens to the semiconductor			
Why is it that the semiconductor manufacturing processes is so inefficient			

Commented [3]: Up date this page regularly as this can facilitate the writing process.

Commented [4]: Because this is a living document, you will be updating this table regularly, therefore it doesn't make sense to worry about organizing every time you open this sheet. Remember the A□Z Sort tool. You can sort based on how you resolved your issue, or you can choose a different organizational method. For example, you could add a column for date resolved and organize chronologically.

Commented [5]: Your notes file will grow as you continue to read. As a result, your page numbers might change. How do you ensure your references remain useful?

1. You could include enough information to find the notes page without a page number. Be careful of just using author names because you might have more than one source from the same first author. If you include title or full citation, that should be enough.
2. Insert a cross-reference

a. insert tab, cross-reference

b. If you choose this path DON'T FORGET TO UPDATE THE FIELDS before you submit or print

Literature Search Parameters:

These searches were performed between (Start Date of reading) and XX/XX/2019.
List of keywords and databases used during this project.

Database/search engine	Keywords	Summary of search
Google scholar	Semi Conductor Voids	3,6, 7
Google scholar	Low coherance infetronomy wafer bonding	4

Commented [6]: This can help you keep track of the searches you perform and what you searched for so that redundancy does not occur.

Commented [7]: This might seem like a silly addition, but if you read literature reviews or meta-analyses, you will notice this information is preserved. It is good practice to record how you found your information.

Tags:

Tag Name	

Article #1 Notes: Title

Article notes should be on separate sheets

KEEP THIS BLANK AND USE AS A TEMPLATE

Source Title	
Source citation (APA Format)	
Original URL	
Source type	
Keywords	
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Summary of key points + notes (include methodology)	
Research Question/Problem/ Need	
Important Figures	
VOCAB: (w/definition)	
Cited references to follow up on	
Follow up Questions	

Commented [8]: Remember to take notes and summarize the work in your own words. Doing this upfront will help you avoid PLAGIARISM.

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Article #2 Notes: Title

Article notes should be on separate sheets

Source Title	
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Original URL	
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Keywords	
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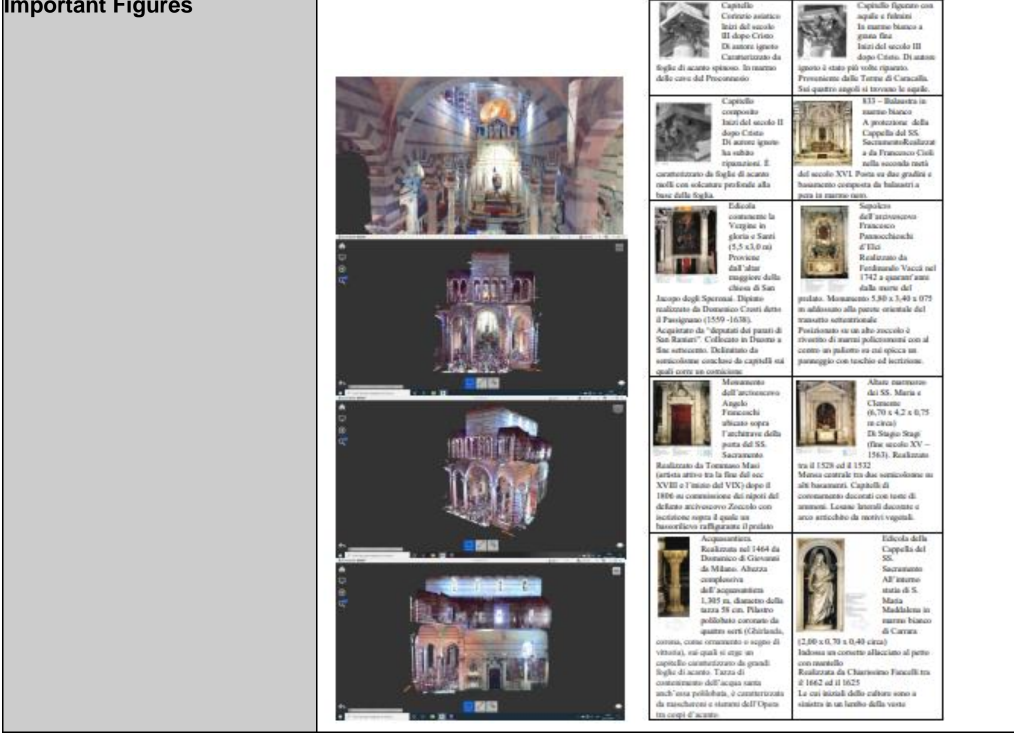
Summary of key points + notes (include methodology)	
Research Question/Problem/ Need	
Important Figures	
VOCAB: (w/definition)	
Cited references to follow up on	
Follow up Questions	

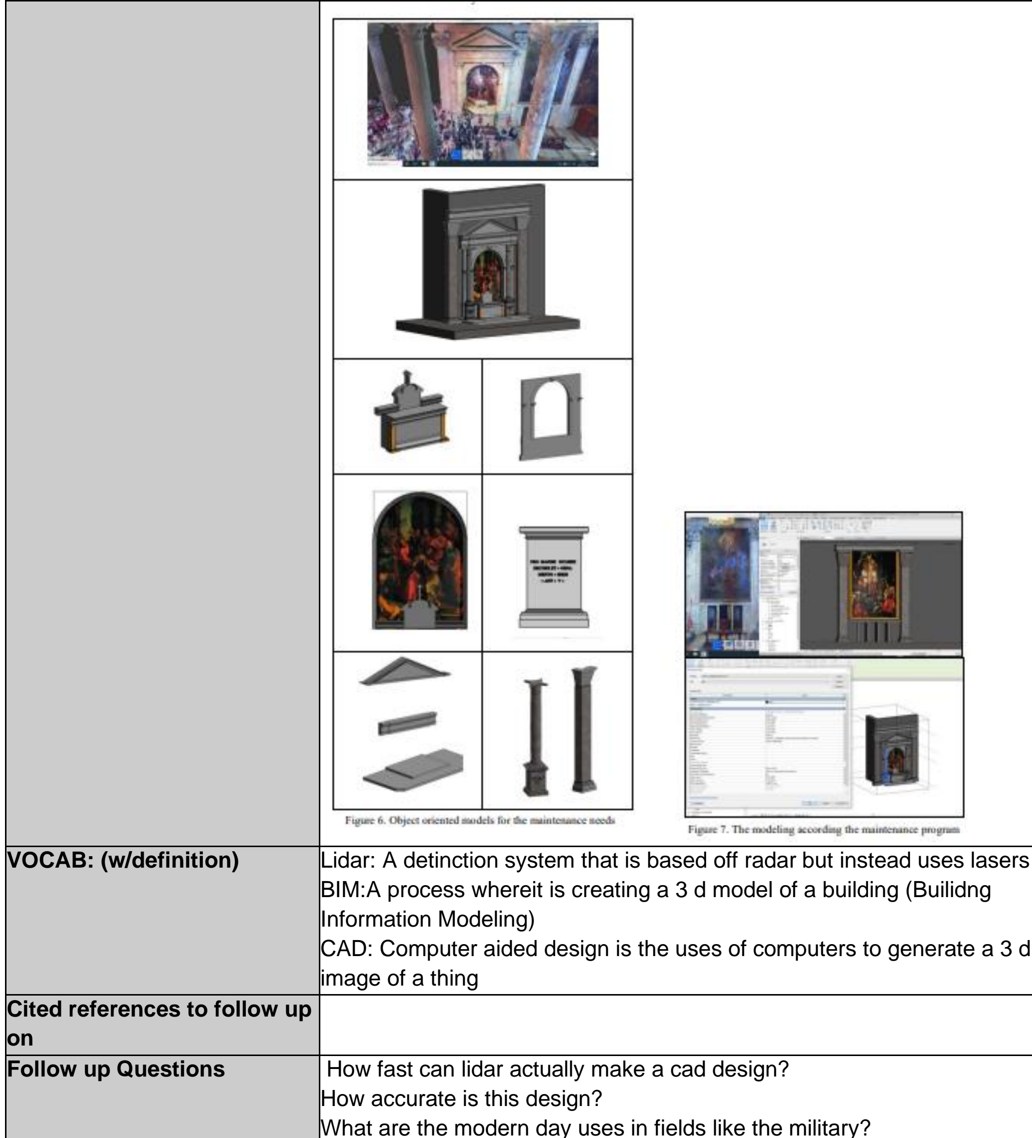
Commented [11]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #1 Notes: THE METROLOGY AND THE BIM APPROACH: A NEW COGNITIVE PARADIGM
ABOUT THE ANCIENT CONSTRUCTION
Article notes should be on separate sheets

Source Title	The International Society for Photogrammetry and Remote Sensing
Source citation (APA Format)	Fiamma, P. (2019). THE METROLOGY AND THE BIM APPROACH: A NEW COGNITIVE PARADIGM ABOUT THE ANCIENT CONSTRUCTION. *The International Archives of the Photogrammetry, Remote Sensing and Spatial Information Sciences,* XLII(2W17), 123-127. https://doi.org/10.5194/isprs-archives-XLII-2-W17-123-2019
Original URL	https://isprs-archives.copernicus.org/articles/XLII-2-W17/123/2019/
Source type	Journal Article
Keywords	KEY WORDS: ancient construction, BIM level, maintenance, methodology, technical component modeling
#Tags	

Summary of key points + notes (include methodology)	This article was about the idea that we could use Building Information Modeling (BIM) technology to make a Computer Aided Design (CAD) design of an architectural historical site. This BIM technology would scan the site and be able to make a CAD design of the site via metrology, capturing many measurements. The use of this technology has had its problems, as BIM technology was made to be used on modern buildings and architecture. The unusual, strangeness of historic architecture often results in mistakes as the BIM is not designed to look for these historic architecture pieces. The article specifically called out the Leaning Tower of Pisa in France and the difficulty BIM technology had with its unique architectural design. While BIM technology was successful in that case, it required some specific tinkering to deal with the old architectural work. Notes: • BIM is using lidar or fast lasers to map out the area to get a map of the incorporate it into cad • Some of the older artifacts have weird constructional pieces so although it works you do need to make adjustments sometimes to help
Research Question/Problem/ Need	To attempt to record historical architecture without hurting it and having accurate measurements that will last post its destruction.

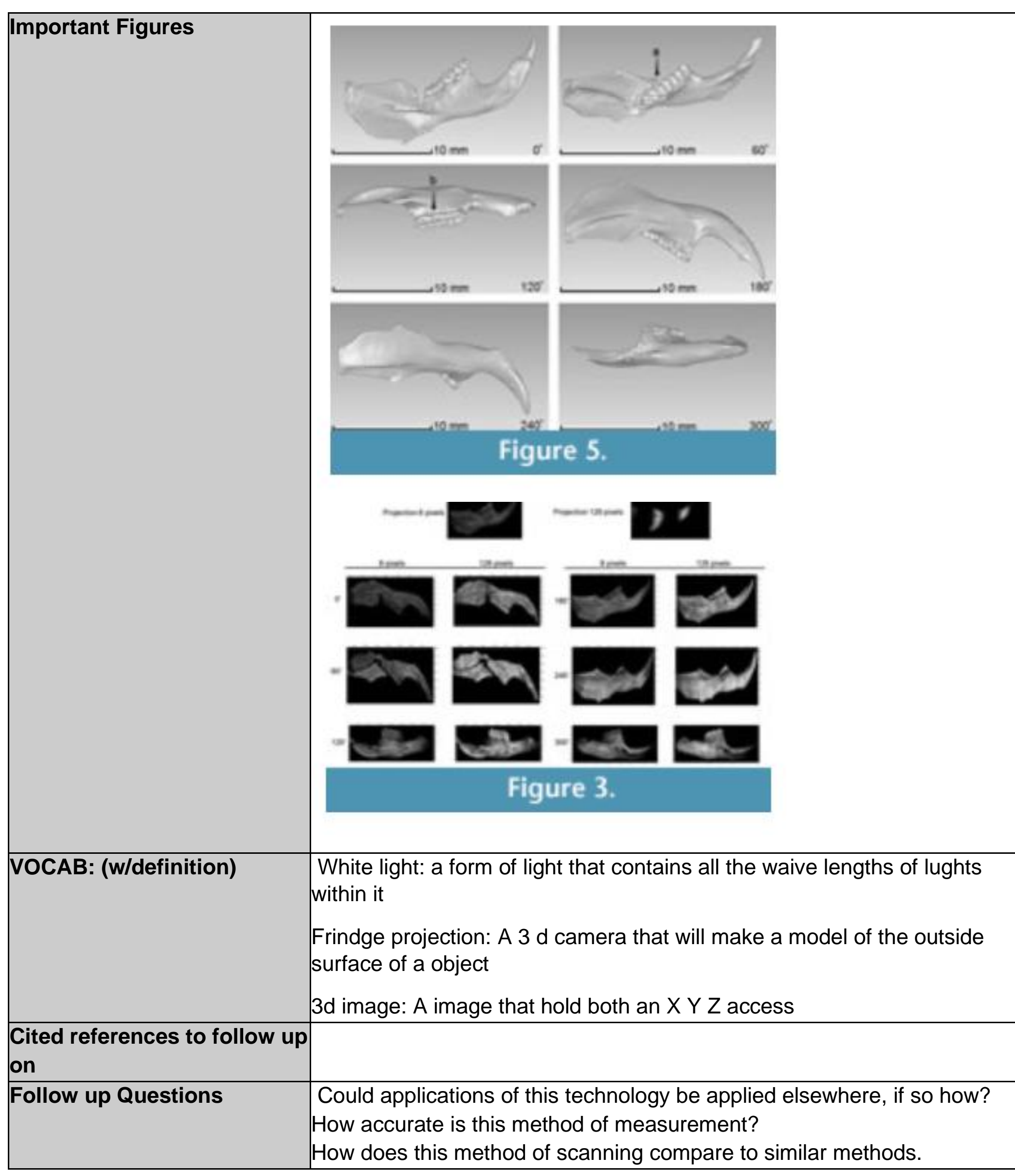
Important Figures	

	
VOCAB: (w/definition)	Lidar: A detinction system that is based off radar but instead uses lasers BIM:A process whereit is creating a 3 d model of a building (Builidng Information Modeling) CAD: Computer aided design is the uses of computers to generate a 3 d image of a thing
Cited references to follow up on	
Follow up Questions	How fast can lidar actually make a cad design? How accurate is this design? What are the modern day uses in fields like the military?

Article #2 Notes: A novel application of the white light/fringe projection duo: recovering high precision 3-D images from fossils for the digital preservation of morphology covered a major problem

Article notes should be on separate sheets

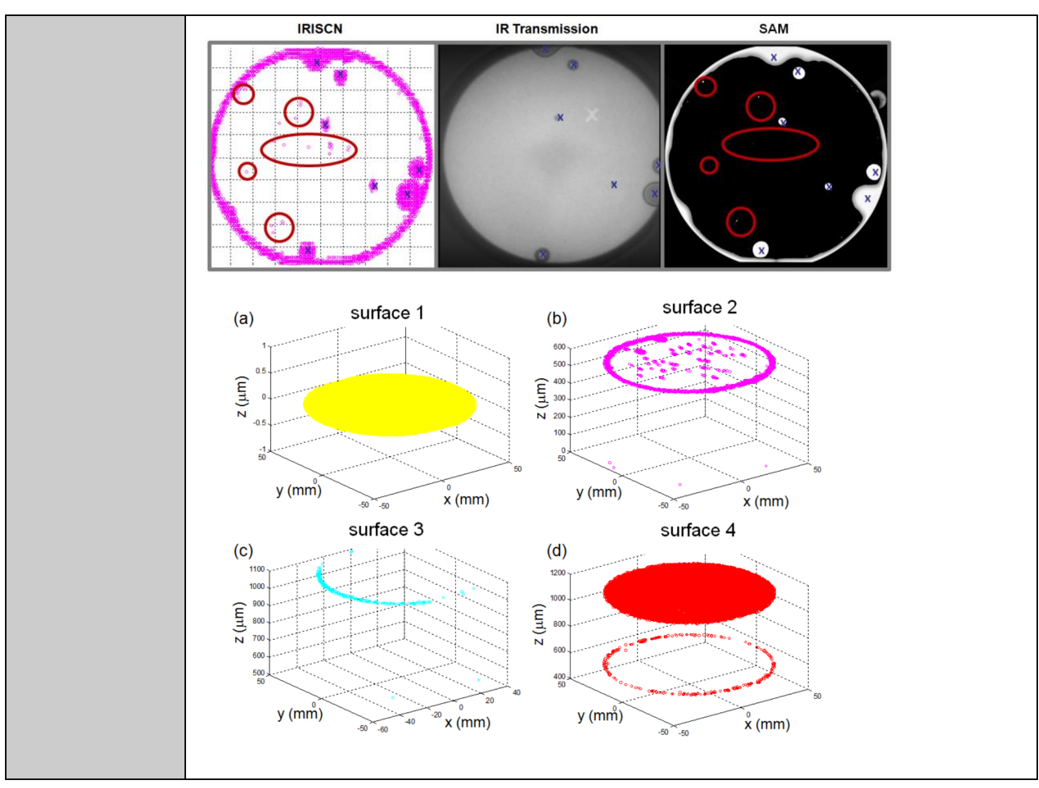
Source Title	Paleontologist Electronica
Source citation (APA Format)	Óptica~ing.juancarlosg@gmail.com, J. C. G.-G. de I. en, Guadalajara~taniagutierrezgarcia@gmail.com, T. A. G.-G. de, León~jfmosino@gmail.com, J. F. M. N. de M.-I. T. de, México~evazquez@ecologia.unam.mx, E. V.-D. N. A. de, Óptica~amalia@cio.mx, A. M. de I. en, & Historia~arromatu5@yahoo.com.mx, J. A.-C. N. de A. e. (2015, August 15). *A novel application of the white light/fringe projection duo: Recovering high precision 3-D images from fossils for the digital preservation of morphology*. Palaeontologia Electronica. https://doi.org/10.26879/516
Original URL	https://palaeo-electronica.org/content/2015/1272-3d-fossil-images-and-white-light#link_tab
Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	My article A novel application of the white light/fringe projection duo: recovering high precision 3-D images from fossils for the digital preservation of morphology covered a major problem. When attempting to get DNA out of a ancient fossil a lot of the time it ends up with the destruction or damage to the fossil. Due to this they thought that they could digitally preserv the fossil. With this problem they decided to use white light and and fringe projection duo to get extremely accurate measurements of the fossil to put online. With this use of technology they will be able to make a online replica so accurate that scientists will be able to maintain using the fossil to research things past destroying it too extract DNA.
Research Question/Problem/ Need	How can people preserve a fossil and receive information fro it without damaging it.

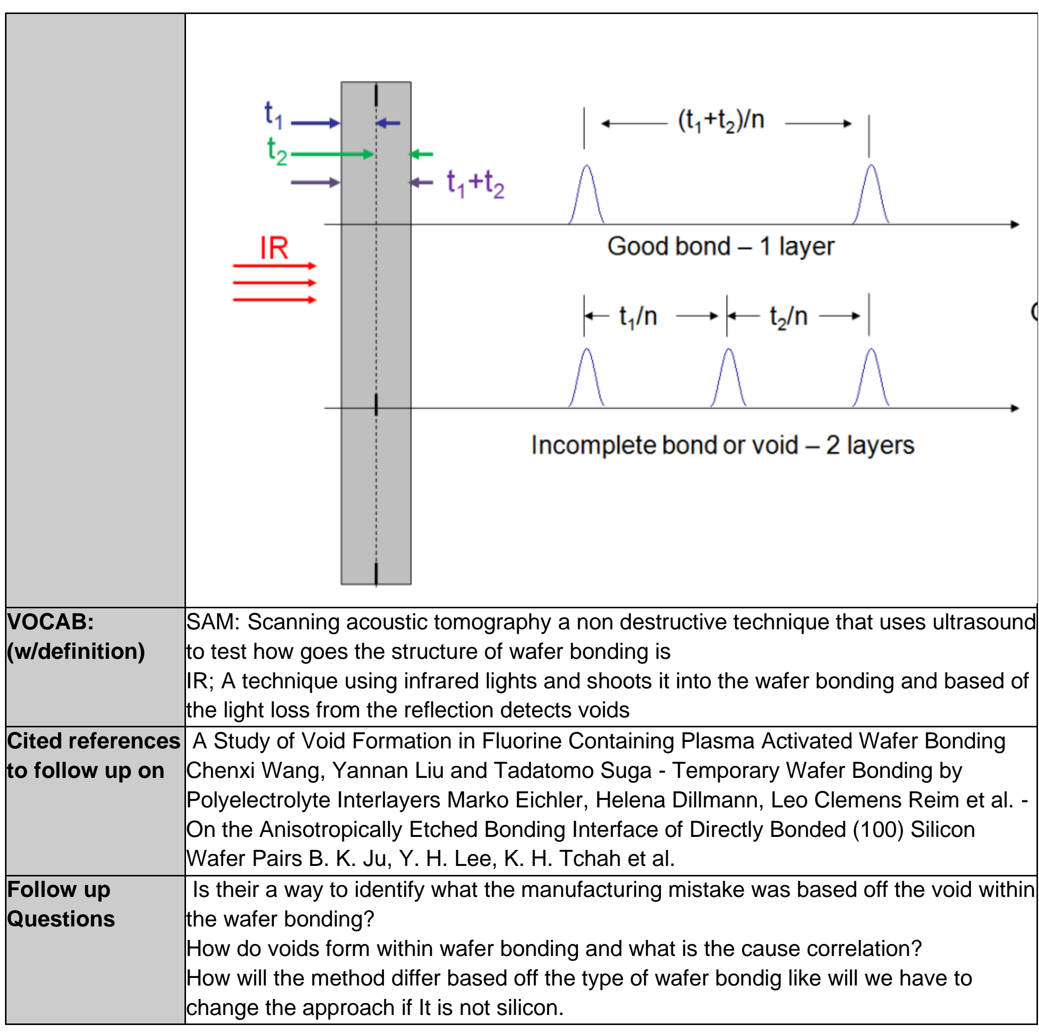
Important Figures	
VOCAB: (w/definition)	White light: a form of light that contains all the waive lengths of lughts within it Frindge projection: A 3 d camera that will make a model of the outside surface of a object 3d image: A image that hold both an X Y Z access
Cited references to follow up on	
Follow up Questions	Could applications of this technology be applied elsewhere, if so how? How accurate is this method of measurement? How does this method of scanning compare to similar methods.

Article #3 Notes: Inspection of Bonded Interfaces Using Scanning Infrared Interferometry

Article notes should be on separate sheets

Source Title	The Electrochemical Society
Source citation (APA Format)	Poduje, N., Kerr, W., & Turner, K. T. (2010). Inspection of Bonded Interfaces Using Scanning Infrared Interferometry. *ECS Transactions*, *33*(4), 537. https://doi.org/10.1149/1.3483545
Original URL	https://iopscience.iop.org/article/10.1149/1.3483545/pdf
Source type	Journal Entry
Keywords	
#Tags	
Summary of key points + notes (include methodology)	Summary: This article describes a new technique for measuring and investigating voids within wafer bonded materials like semi conductors. These voids are extremely small gaps in the wafer bonding and can lead to malfunctions with the computer chip. There are two methods they test the classic (IR) method or infrared infetronomy witch works by shining a light through the layers of the wafer and if there is an extra occurrence of reflection than there is a void within the wafer. This method is good as it is accurate and is a non contact way of finding foids. It can test thousands of voids at once and find abunch of reflections. They compared this method with IR transmission imagery(IRSCIN) and tested It on wafer bonding with natural voids. They compared these two stratageis the newer strategy of (IRSCIN) and the original (IR) strategy and compared the dat they collected against (SAM) Scanning acoustic microscopy. The method they made of IRSCIN was more accurate whilst also not making physical contact with the thing you want to find voids in. Notes • (IRSCIN)>(IR) • Voids can lead to issues within the product and need to be found to fix manufacturing • (IRSCIN) and (IR) are really good for stuff like semi conductors due to it not needing to touch it
Research Question/Problem/ Need	Finding a more accurate way to find voids within wafer bonding without physical contact.
Important Figures	IRISCN IR Transmission SAM


IRISCN
IR Transmission
SAM
(a)
surface 1
(b)
surface 2
(c)
surface 3
(d)
surface 4
z (µm)
y (mm)
x (mm)

	
VOCAB: (w/definition)	SAM: Scanning acoustic tomography a non destructive technique that uses ultrasound to test how goes the structure of wafer bonding is IR; A technique using infrared lights and shoots it into the wafer bonding and based of the light loss from the reflection detects voids
Cited references to follow up on	A Study of Void Formation in Fluorine Containing Plasma Activated Wafer Bonding Chenxi Wang, Yannan Liu and Tadatomo Suga - Temporary Wafer Bonding by Polyelectrolyte Interlayers Marko Eichler, Helena Dillmann, Leo Clemens Reim et al. - On the Anisotropically Etched Bonding Interface of Directly Bonded (100) Silicon Wafer Pairs B. K. Ju, Y. H. Lee, K. H. Tchah et al.
Follow up Questions	Is their a way to identify what the manufacturing mistake was based off the void within the wafer bonding? How do voids form within wafer bonding and what is the cause correlation? How will the method differ based off the type of wafer bondig like will we have to change the approach if It is not silicon.

Article #4 Notes: Measurements of a Semiconductor Waveguide Using a Low-Coherence Interferometric Reflectometer
Article notes should be on separate sheets

Source Title	IEEE
Source citation (APA Format)	Kasaya, K., Yoshikuni, Y., & Ishii, H. (1996). Measurements of a semiconductor waveguide using a low-coherence interferometric

	reflectometer. *IEEE Photonics Technology Letters*, *8*(2), 251–253. IEEE Photonics Technology Letters. https://doi.org/10.1109/68.484257
Original URL	https://ieeexplore.ieee.org/document/484257
Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	so basically this article was attempting to measure the lost wave guides within a semiconductor. They did this by using a Low-Coherence Interferometric Reflectometer. There is an older method to do this but when attempting to do this older method when you have short tunnels within the semiconductor it's usually going to make your answers a lot more skewed. So they measured 2,4, and 6 mm waveguides to see if using LCI would be a more effective method of for the shorter paths. The way it measured it is by shooting light through the semiconductor and seeing how much reflects back. So based off how much reflects back we will be able to measure the amount of waveguide lost during the experiment. The results said that the method was extremely accurate even more accurate than the old method.
Research Question/Problem/ Need	Try to find a strategy to measure waveguides in semiconductors for short passage ways accurately.

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<td>Important Figures</td>
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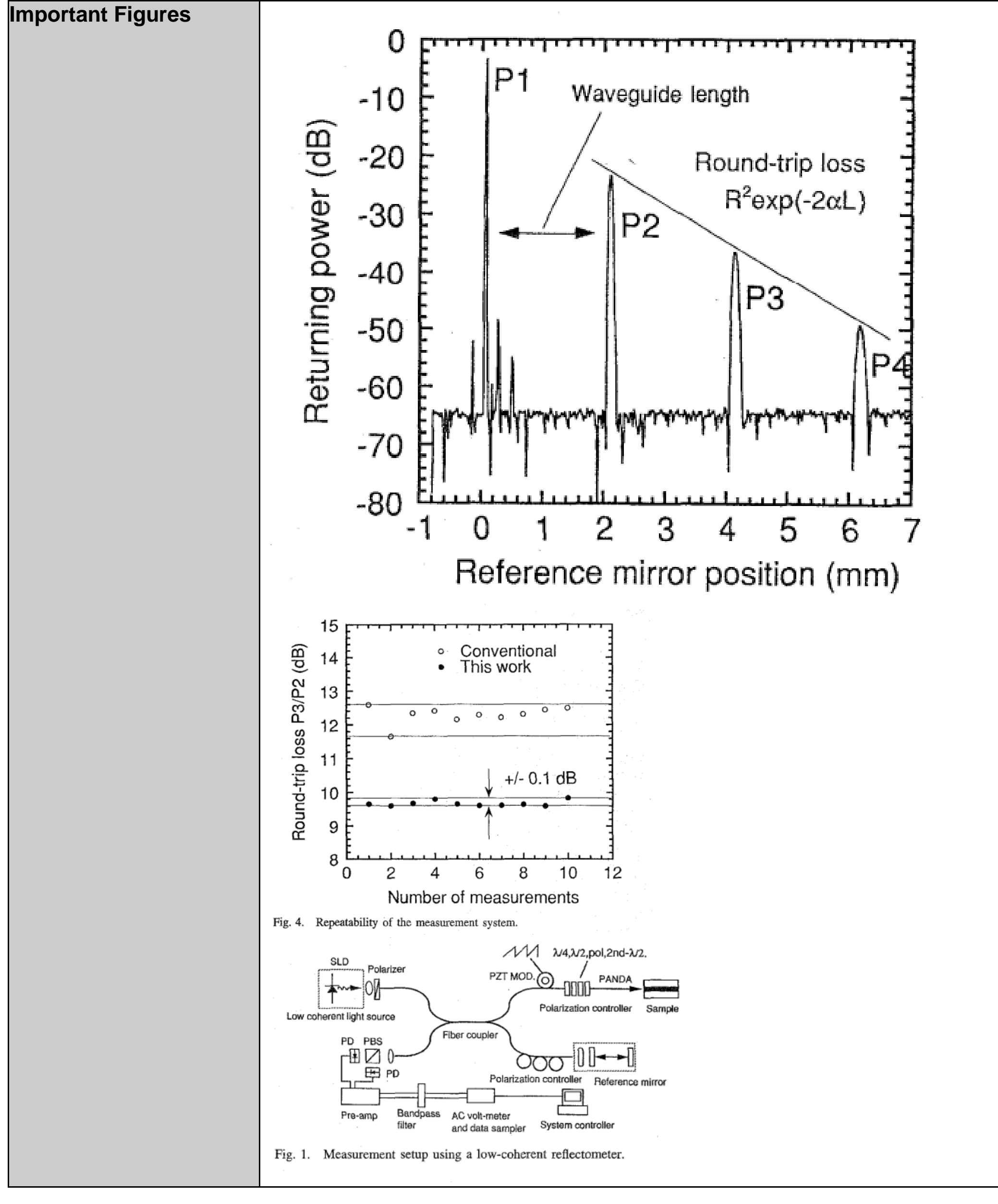

Fig. 4. Repeatability of the measurement system.

Fig. 1. Measurement setup using a low-coherent reflectometer.
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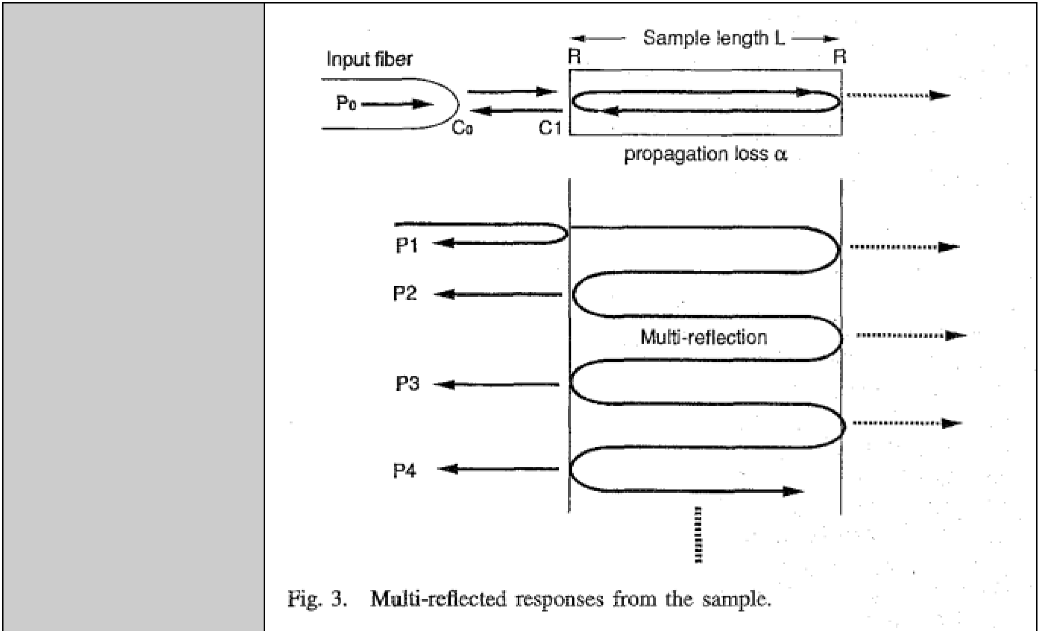
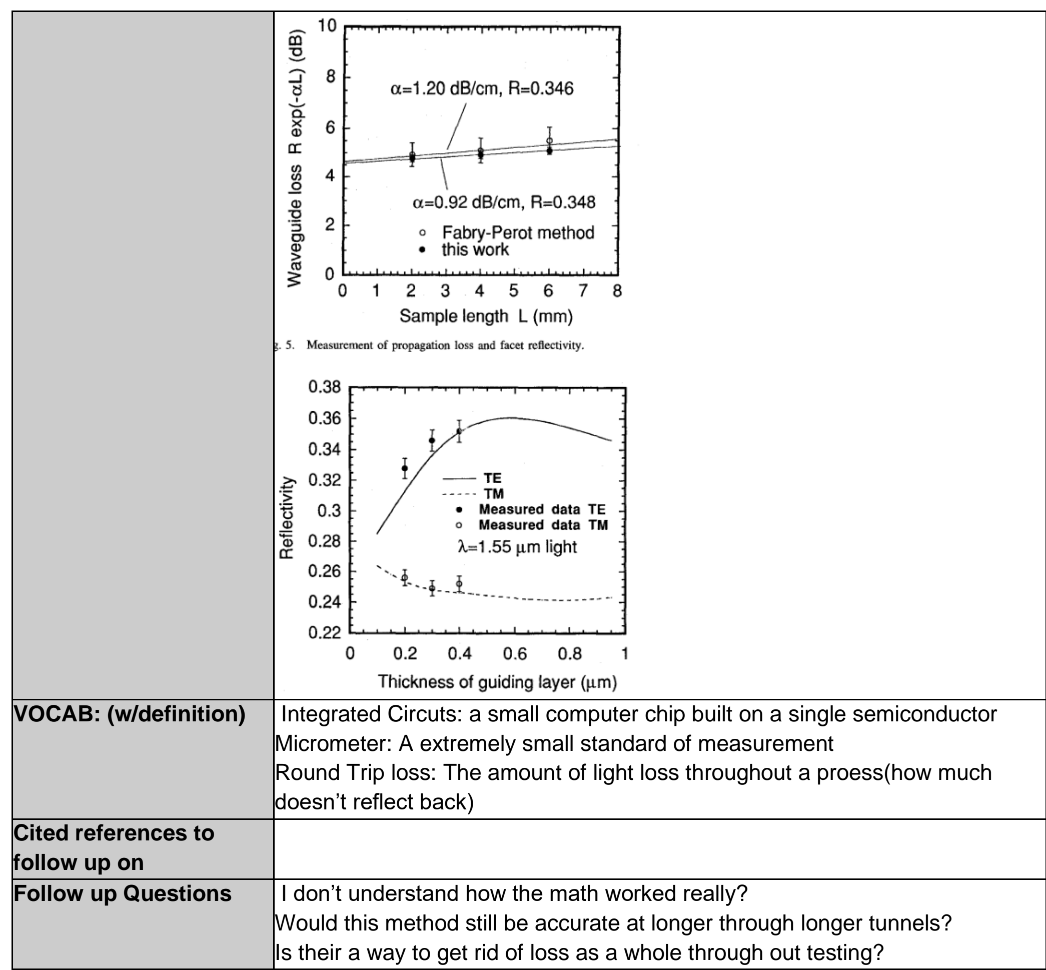


Fig. 3. Multi-reflected responses from the sample.

	 g. 5. Measurement of propagation loss and facet reflectivity.
VOCAB: (w/definition)	Integrated Circuts: a small computer chip built on a single semiconductor Micrometer: A extremely small standard of measurement Round Trip loss: The amount of light loss throughout a proess(how much doesn't reflect back)
Cited references to follow up on	
Follow up Questions	I don't understand how the math worked really? Would this method still be accurate at longer through longer tunnels? Is their a way to get rid of loss as a whole through out testing?

Article #5 Notes: On the Relationship between Semiconductor Manufacturing Volume, Yield, and Reliability

Article notes should be on separate sheets

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Source Title	IEEE
Source citation (APA Format)	Siddiqui, J., Ortega, J., & Albus, B. (2017). On the relationship between semiconductor manufacturing volume, yield, and reliability. *2017 IEEE International Reliability Physics Symposium (IRPS)*, SR-1.1-SR-1.5. https://doi.org/10.1109/IRPS.2017.7936409

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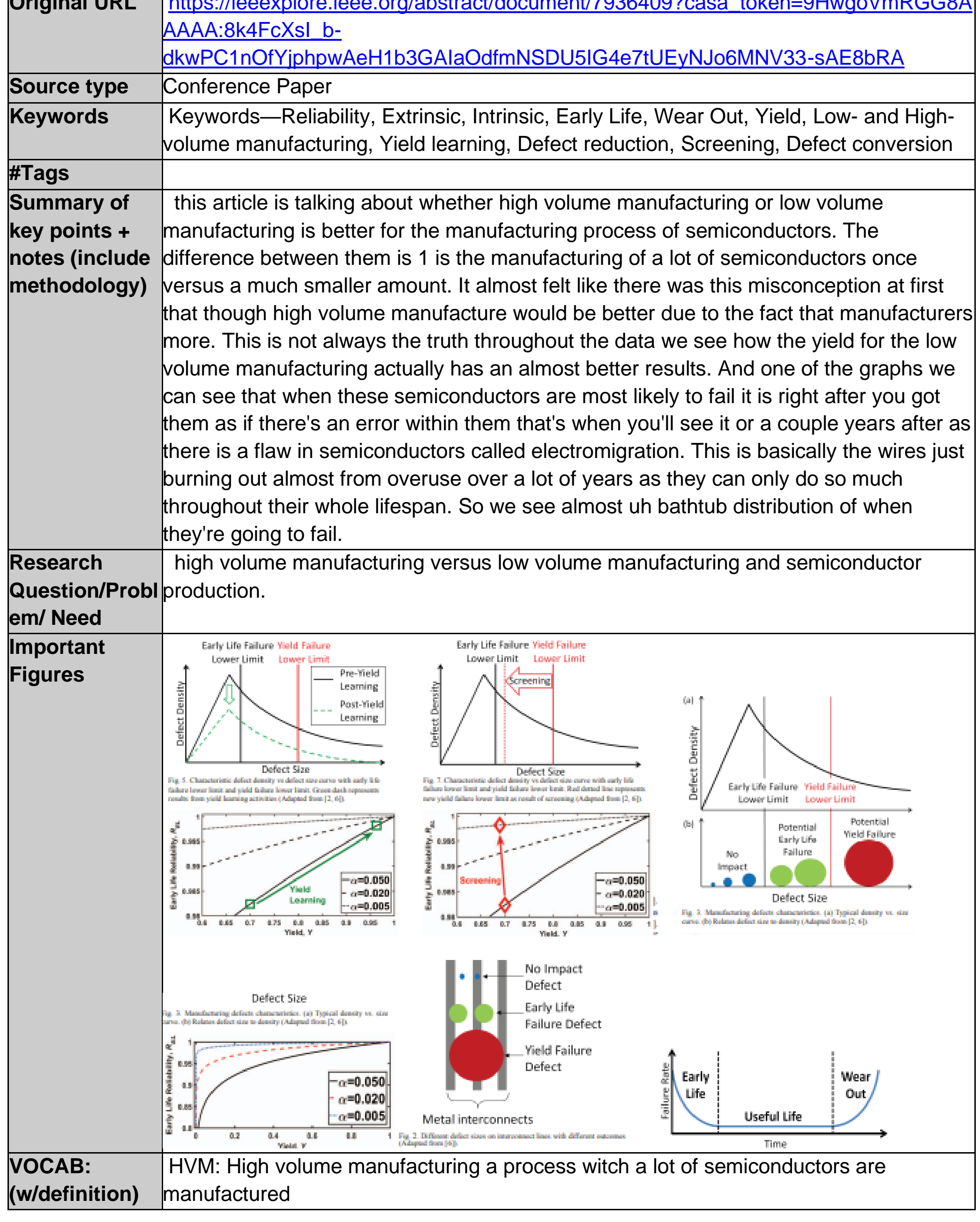
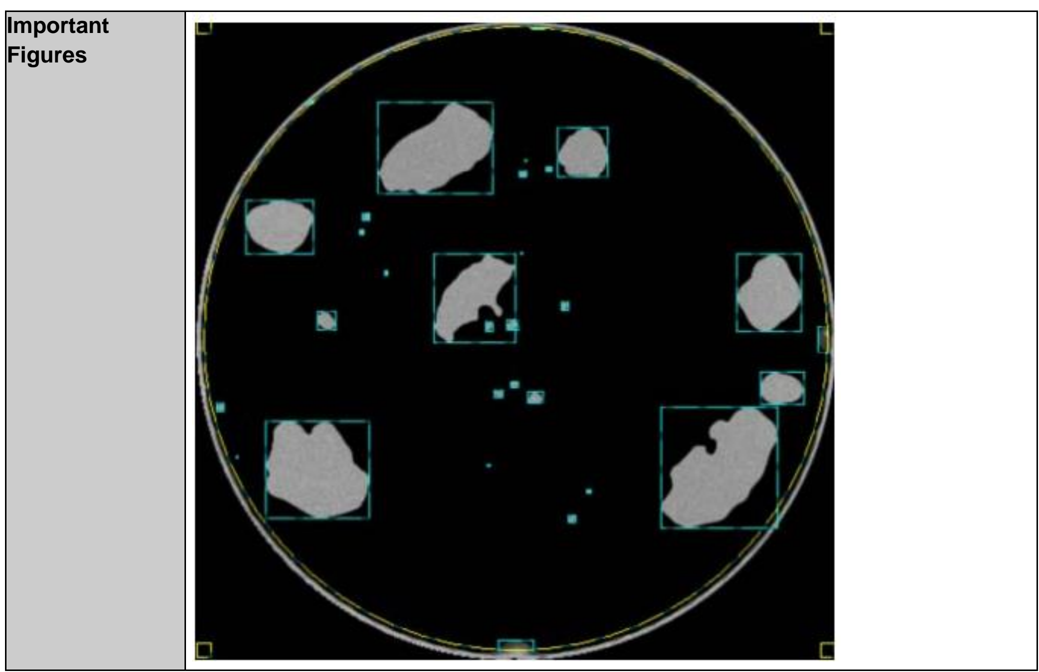
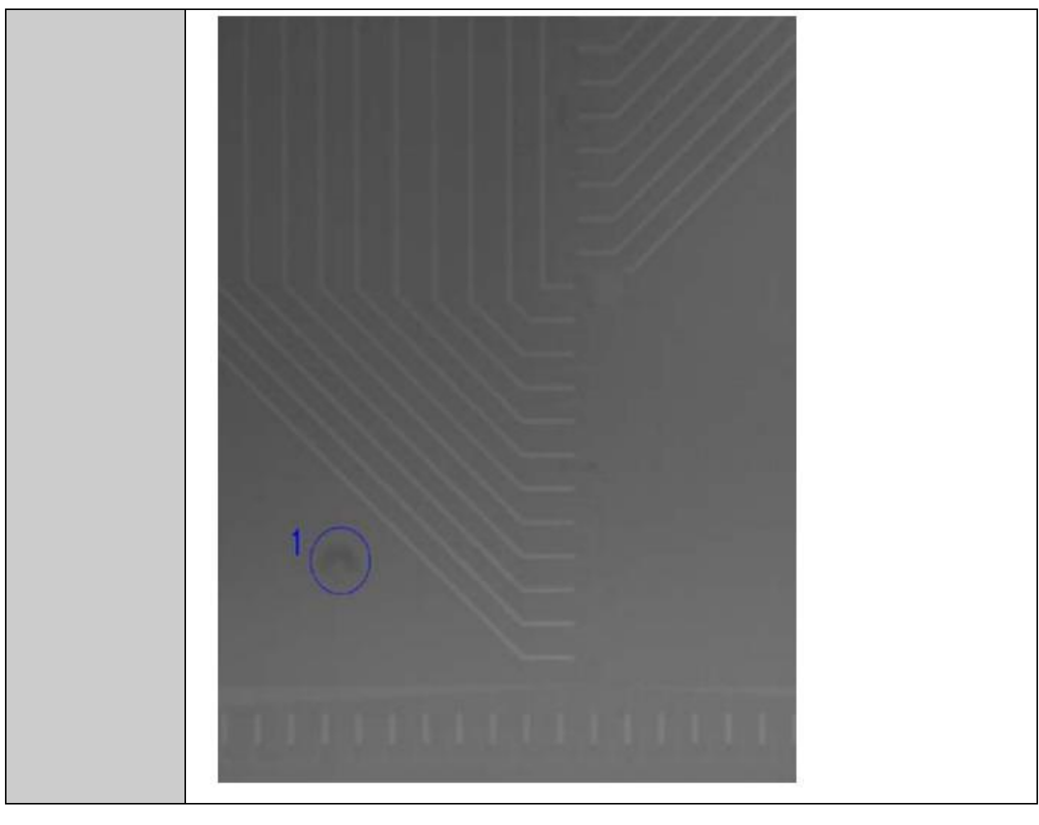
<tr><td>Source type</td><td>Conference Paper</td></tr>
<tr><td>Keywords</td><td>Keywords—Reliability, Extrinsic, Intrinsic, Early Life, Wear Out, Yield, Low- and High-volume manufacturing, Yield learning, Defect reduction, Screening, Defect conversion</td></tr>
<tr><td>#Tags</td><td></td></tr>
<tr><td>Summary of key points + notes (include methodology)</td><td>this article is talking about whether high volume manufacturing or low volume manufacturing is better for the manufacturing process of semiconductors. The difference between them is 1 is the manufacturing of a lot of semiconductors once versus a much smaller amount. It almost felt like there was this misconception at first that though high volume manufacture would be better due to the fact that manufacturers more. This is not always the truth throughout the data we see how the yield for the low volume manufacturing actually has an almost better results. And one of the graphs we can see that when these semiconductors are most likely to fail it is right after you got them as if there's an error within them that's when you'll see it or a couple years after as there is a flaw in semiconductors called electromigration. This is basically the wires just burning out almost from overuse over a lot of years as they can only do so much throughout their whole lifespan. So we see almost uh bathtub distribution of when they're going to fail.</td></tr>
<tr><td>Research Question/Problem/ Need</td><td>high volume manufacturing versus low volume manufacturing and semiconductor production.</td></tr>
<tr><td>Important Figures</td><td>
</td></tr>
<tr><td>VOCAB: (w/definition)</td><td>HVM: High volume manufacturing a process witch a lot of semiconductors are manufactured</td></tr>
</table>

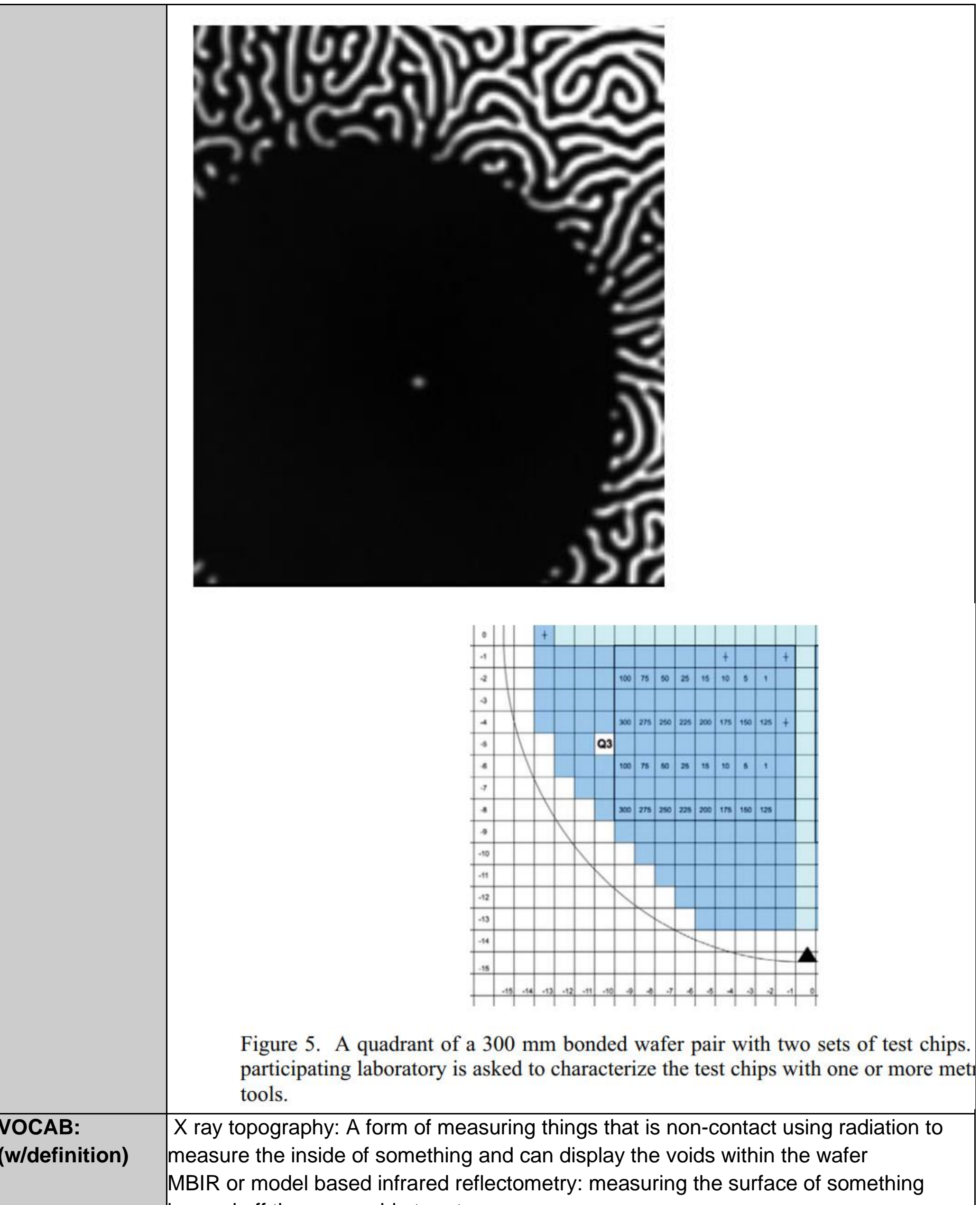
	LVM: low volume manufacturing a process where less semiconductors are manufactred Early life failure: a failure of a semiconductor early on usually caused by cracks or voids Wear out failure: failure of a semi conductor usually caused by over use over a long period of time
Cited references to follow up on	
Follow up Questions	is there an actual step within the manufacturing process that can be attributed to a lot of these failures? Why is LVM and HVM different they're all the same process I feel like they should have the same results why would the amount that are being put out affect that product. Is there a way to predict early life failures and also is there a way to extend its life so that it can be good enough quality for something like military computer chips.

Article #6 Notes: Intercomparison of Methods for Detecting and Characterizing Voids in Bonded Wafer Pairs
Article notes should be on separate sheets

Source Title	The Electrochemical Society
Source citation (APA Format)	Allen, R. A., Rudack, A., Read, D., & Baylies, W. (2010). Intercomparison of Methods for Detecting and Characterizing Voids in Bonded Wafer Pairs. *ECS Transactions*, *33*(4), 581. https://doi.org/10.1149/1.3483550
Original URL	https://iopscience.iop.org/article/10.1149/1.3483550/meta?casa_token=
Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article talked about finding the most effective ay to measure voids. It started off with an overview on how semi conductors are constructed and their different uses based off how they were constructed. Than the experiment this project did to find the most effective way of measuring voids was that they programmed voids into some semiconductor and than sent out these semi conductors to some labs with various equipment to measure voids. For example X ray topography, Ir coherence infetronomy, Sam, Full wafer infrared illumination, MBIR or model based infrared reflectometry, Infrared coradical microscope, Resonance ultra vibrations technology. Than the article gave a brief description on how each one of these technologies work. Than in the conclusion they got no results, although they talked about their testing method their was never any results to the test just a processes to investigate witch technologies for measuring voids within semi conductors is the best
Research Question/Problem/ Need	What is the best method within metrology witch can be used to find voids within wafer bonded material?

Important Figures	

	1

	 Figure 5. A quadrant of a 300 mm bonded wafer pair with two sets of test chips. participating laboratory is asked to characterize the test chips with one or more metr tools.
VOCAB: (w/definition)	X ray topography: A form of measuring things that is non-contact using radiation to measure the inside of something and can display the voids within the wafer MBIR or model based infrared reflectometry: measuring the surface of something beased off the waveguide to return.

Cited references to follow up on	
Follow up Questions	What ended up being the resuls as the most accurate method? Where can I find the data they found? Did they take into account other factors like being able to identify size and shape correctly in their raiting.

Article #7 Notes: Failure Analysis of IMC Cracking and Voiding Induced by Molding Compound Voids in Advanced Wire Bonding Packages

Article notes should be on separate sheets

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Source Title	IEEE
Source citation (APA Format)	Kuo, Y.-L., Lin, Y.-C., Lin, Y.-T., Huan, H.-S., & Su, D. (2004). Failure analysis of IMC cracking and voiding induced by molding compound voids in advanced wire bonding packages. *Proceedings of the 11th International Symposium on the Physical and Failure Analysis of Integrated Circuits. IPFA 2004 (IEEE Cat. No.04TH8743)*, 221–224. https://doi.org/10.1109/IPFA.2004.1345603
Original URL	https://ieeexplore.ieee.org/abstract/document/1345603?
Source type	Conference Paper
Keywords	
#Tags	
Summary of key points + notes (include methodology)	article is about finding voids and cracks within computer trips. So basically what they're doing is they're using a punch of technologies to they're using X-ray TCR Sam. Then once they use sticking out find voids which are the little air pockets that are stuck within there period if a void is above 100 micrometers it's going to cause a crack period due to the fact of that void is near a bond ball. They also use this technology to find why these bond balls are cracking. What is happening is at some point in the manufacturing process or the packing process there's a void within the semiconductor that is near the bond ball and if it becomes over 100 micrometers it'll cause a crack and if there's a crack within this computer chip it'll be completely broken. They decided to take the information that they got from xrays and compare it to if the computer chipped failed to see the correlation between them and find the failure data and be able to analyze if it's going to fail based off the information the X-ray produces.
Research Question/Problem/ Need	analyzing how to find problems within the bond balls of the computer chips and find the voids and cracks and the relationship to failure.

Important Figures

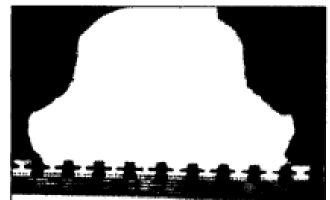


Figure 6: A bond ball with perfect IMC as reference. The bond balls far away from molding compound voids have normal IMC.

Table III: Linear regression analysis shows the molding compound void above 100um has potential crisis to induce IMC cracking failure.

Sample	Distance of voids to bond balls (um)	Void size (um)
#1	96.02	135
#2	16.55	75
#3	212.89	400
#4	562.68	550

Table II: The void size and void distance to bond balls in some samples was measured.

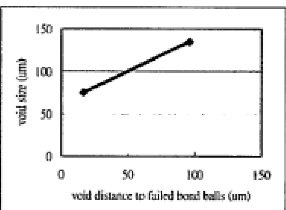


Table IV: The molding compound void should be smaller then 50um if we only concern the critical ones which are close to bond balls.

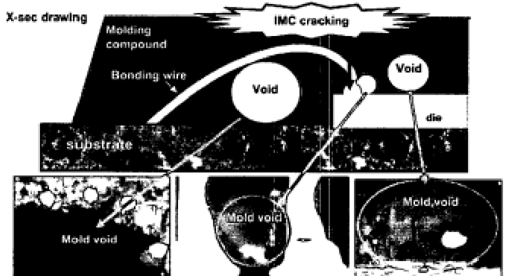


Figure 7: The shorter distance of a mold void to bond balls, the smaller size it needs to induce IMC

VOCAB: (w/definition)

Bond balls: It's a method of wire connecting within semi conductors
Voids:air pockets within the layer of wafer bonding
Cracking: cracks that occuir from largfe voids appearing near bond balls and leads to the break down of semiconductors

Cited references to follow up on

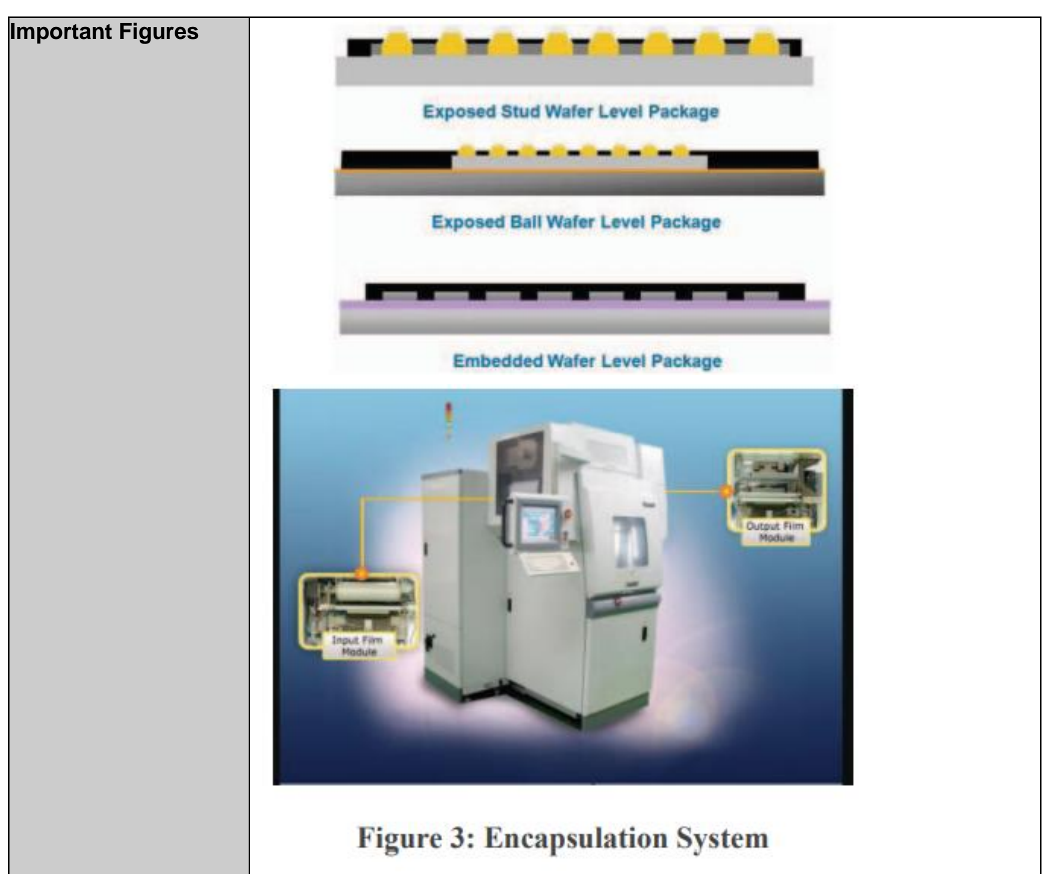
Follow up Questions

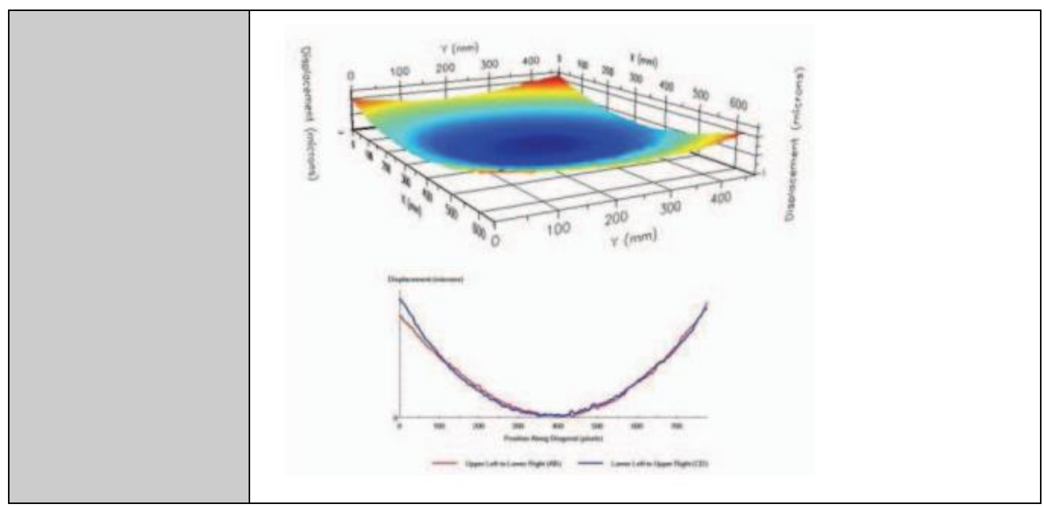
I don't understand how some of the graphs within this paper actually work and the relationship to what they mean?
Why did they do specifically bond balls?

	What were the benefits of their strategy compared to others like IR?

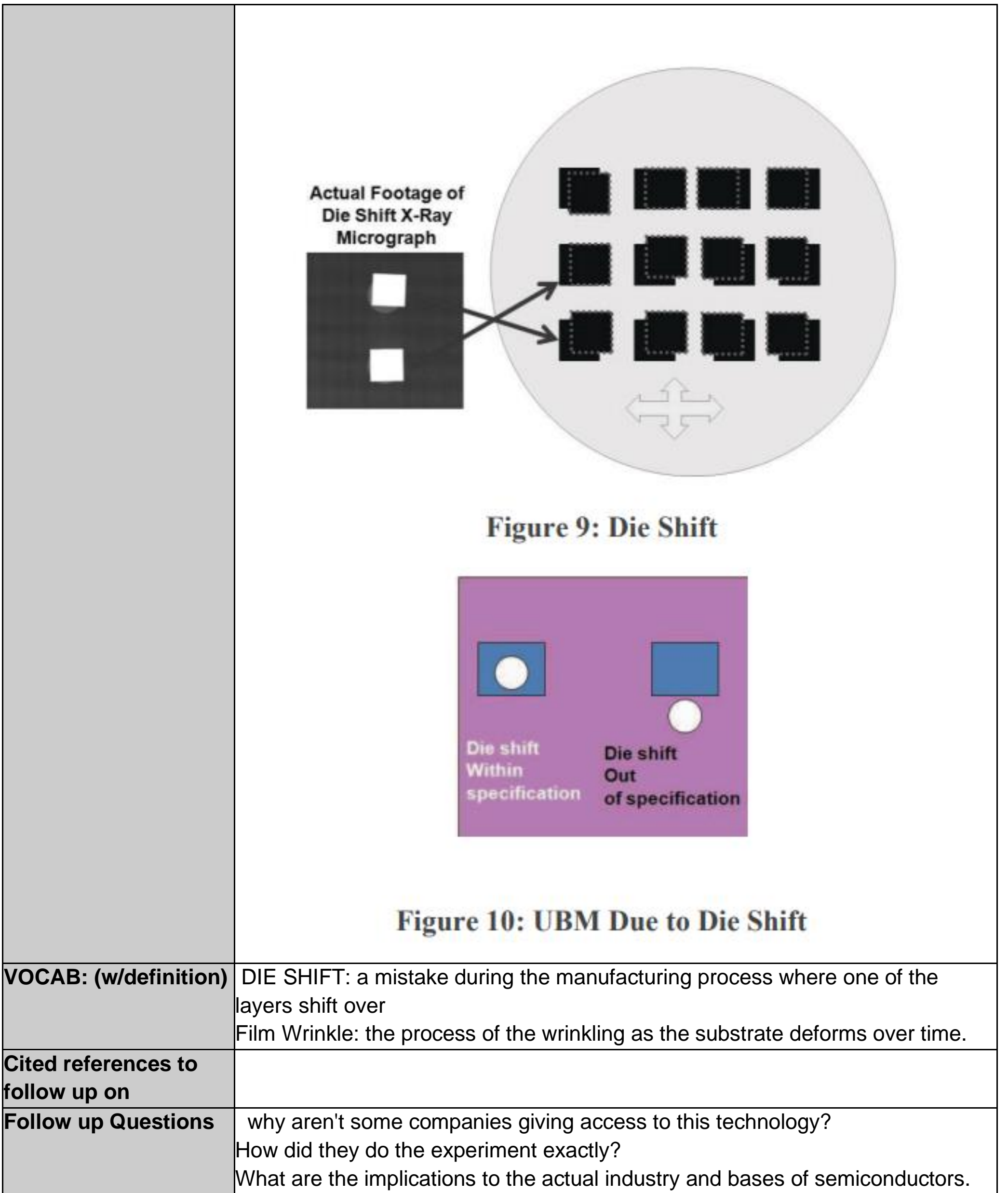
Article #8 Notes: Encapsulation Challenges for Wafer Level Packaging
Article notes should be on separate sheets

Source Title	IEEE
Source citation (APA Format)	Th, E. K., Hao, J. Y., Ding, J. P., Li, Q. F., Chan, W. L., Ho, S. C., Huang, H. M., & Jiang, Y. J. (2009). Encapsulation challenges for wafer level packaging. *2009 11th Electronics Packaging Technology Conference*, 903–908. https://doi.org/10.1109/EPTC.2009.5416414
Original URL	https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5416414&casa_token=2m9Fli3vxxsAAAAA:jdI75XDxP8Wh0KyamB__Hv1DQrhDTsjHzVgOKja-KkwO1OLV2Y-vQNOClC6kOjowUFvEZoU
Source type	Conference Paper
Keywords	Key words: WLP (Wafer Level Package), Wafer Level Molding (WLM), Die Shift (DS), Warpage, Mold Bleed Flashing (MBF), Co-planarity, Voiding, Tape crinkle Incomplete Filling, PEMs (plastic encapsulated microelectronics)
#Tags	
Summary of key points + notes (include methodology)	this article is mainly about the pros and cons of WLP or water l level package which is this type of technology used in semiconductors. It allows for the semiconductor manufacturing with the packaged before the semiconductor is cut. The pros to this method is that the Z or height is a lot smaller, higher I / o density there will be a better performance by the semiconductor and the heat distribution is going to be better on the semiconductor and lastly it's going to be a lot more cost effective in the actual production costs as there's going to be a lot less wasted material throughout the production process. There is a problem with this though and that is that this technology is a little bit secretive. A lot of the know how of this technology is only known by the largest companies who have already been able to do this since they're so large and rich. This article went into a lot of detail on the problems that they had to fix and some that they couldn't and there's a lot of companies were doing this a lot added a lot more of an advanced level.
Research Question/Problem/ Need	What are the challenges that come from usoing WLP and what are the pros and cons?

Important Figures	 **Figure 3: Encapsulation System**

Y (mm)
X (mm)
Displacement (microns)
0
100
200
300
400
500
600

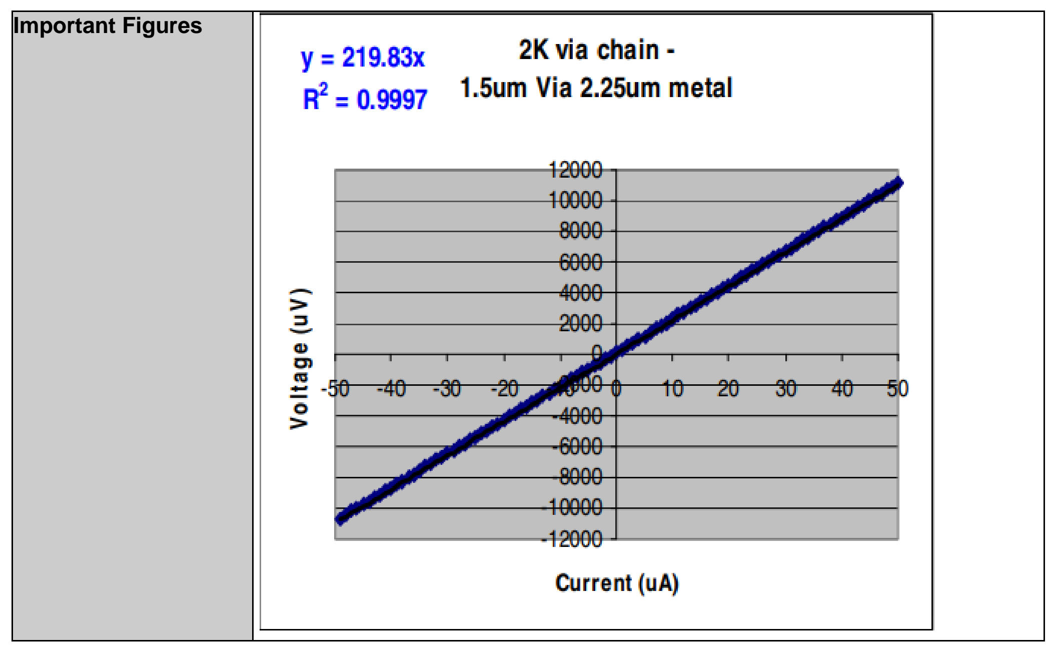
	 Figure 9: Die Shift Figure 10: UBM Due to Die Shift
VOCAB: (w/definition)	DIE SHIFT: a mistake during the manufacturing process where one of the layers shift over Film Wrinkle: the process of the wrinkling as the substrate deforms over time.
Cited references to follow up on	
Follow up Questions	why aren't some companies giving access to this technology? How did they do the experiment exactly? What are the implications to the actual industry and bases of semiconductors.

Article #9 Notes: Infrared Microscopy for Overlay and Defect Metrology on 3D-Interconnect Bonded Wafers

Article notes should be on separate sheets

KEEP THIS BLANK AND USE AS A TEMPLATE

Source Title	Infrared Microscopy for Overlay and Defect Metrology on 3D-Interconnect Bonded Wafers
Source citation (APA Format)	Rudack, A. C., Kong, L. W., & Baker, G. G. (2010). Infrared microscopy for overlay and defect metrology on 3D-interconnect bonded wafers. *2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, 347–352. https://doi.org/10.1109/ASMC.2010.5551481
Original URL	https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5551481&casa_token=ocb8MH270nAAAAAA:vXZ0DLKFP495BC17fhqSgtqju_I92Bj9arpFaChLBClV5P7YgOfb0j2qT9Fj64CFBu5v_Uw
Source type	Conference Paper
Keywords	
#Tags	
Summary of key points + notes (include methodology)	in this article they again used IR to measure the effectiveness of the wafer bonding period this time instead of just looking for voids they also looked at how symmetrical the pieces were put on top of each other to make sure that they were in order while also looking for defects like voids. So what they did was they attempted to see if there is a correlation between how well aligned it was and the amount of defects to the yield. They found that if it's more than 2.5 micrometers off that there could be an electrical failure so you need it to be really well aligned for it to be a successful wafer bonding and for the computer chip to be able to be as ideal as possible. They also found that the voids can be changed throughout the whole process of phrases bonding. All in all using IR is a very good method of looking at wafer bonding.
Research Question/Problem/ Need	How can IR be used to measure alignment and defects of wafer bonding.

Important Figures	

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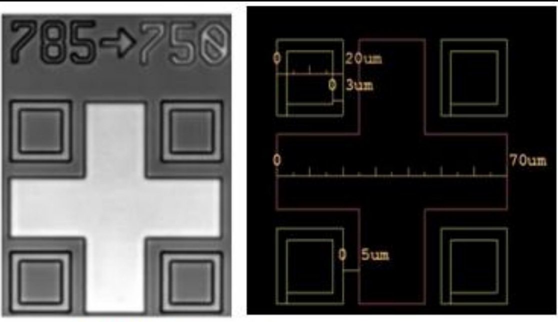
<tr><td></td><td>

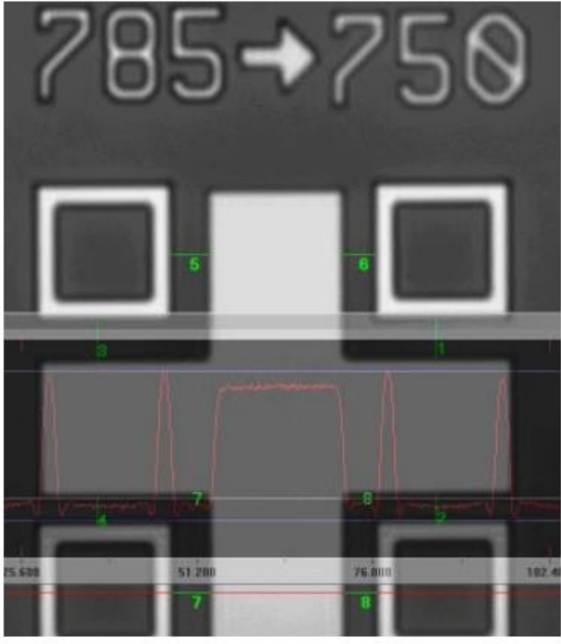
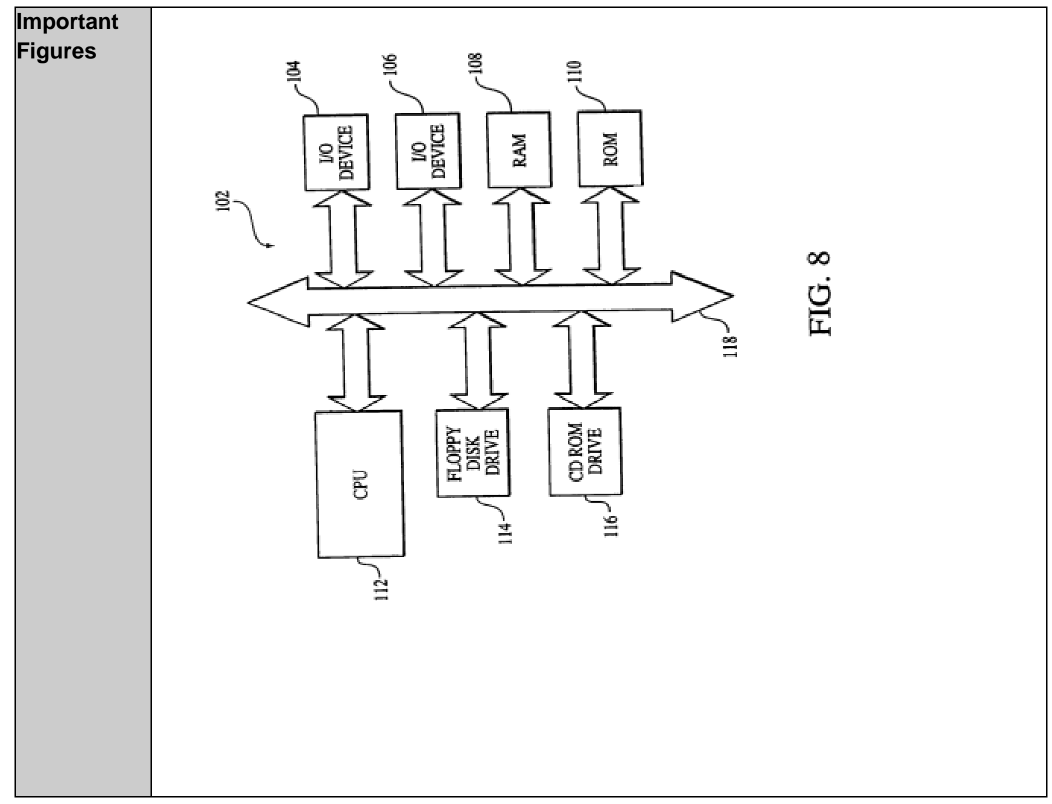
Combined fiducials Ideal alignment for overlay calculation
Figure 2. Combined alignment fiducials enabling overlay calculations of bonded wafer pairs when viewed using IR microscopy


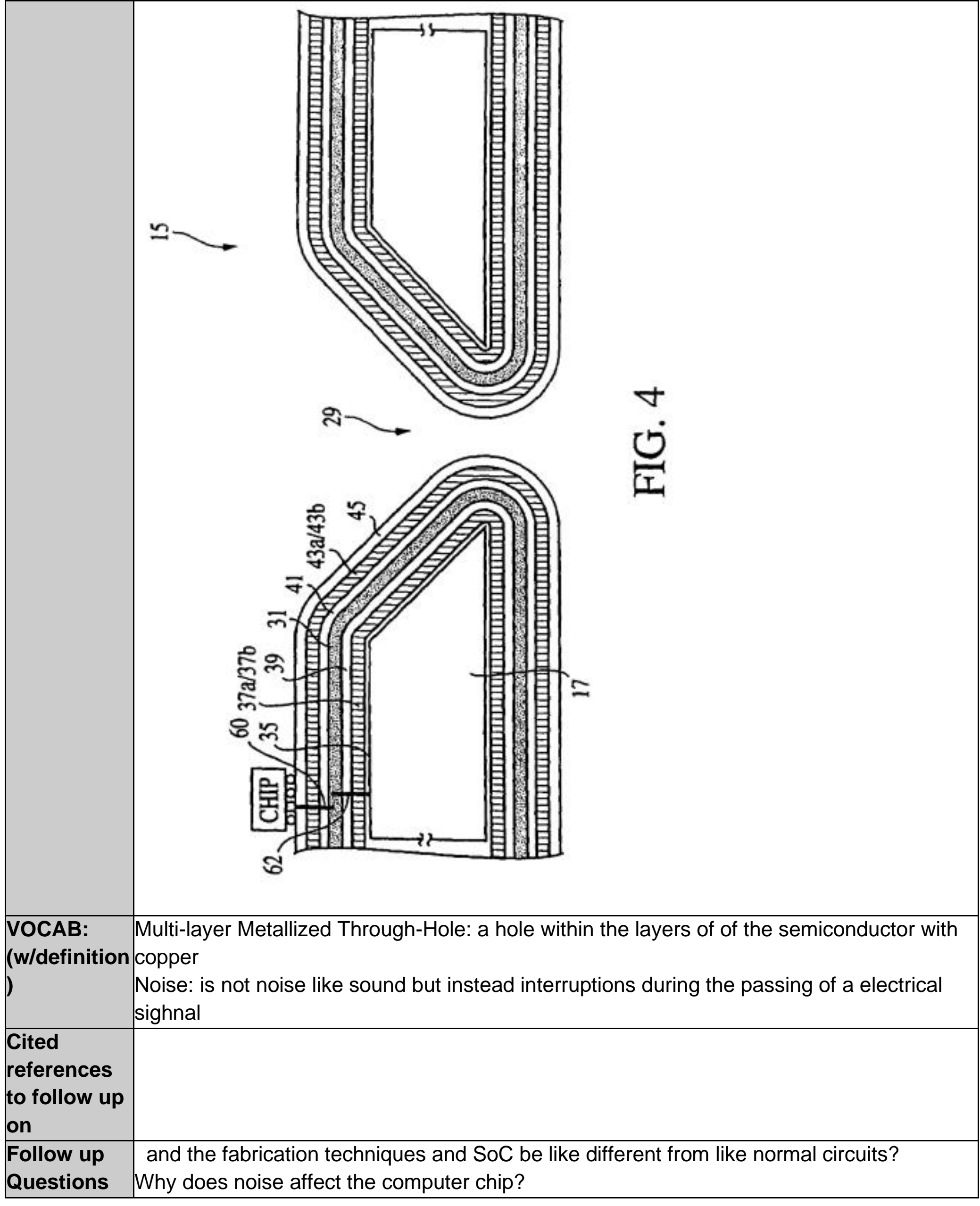
Figure 2a . Combined alignment fiducial measurements by IR metrology system enabling overlay calculations</td></tr>
<tr><td>VOCAB: (w/definition)</td><td>Microscopy: The use of actualy measuring something accurately like using a microscope
Overlay alignment: this is the alignment of each wafer on top of one another.</td></tr>
</table>

Cited references to follow up on	
Follow up Questions	How exactly do they change the voids? Why does the allighnment make an affect on its affection? What are the challenges of finding defects within ir metrology?

Patent #1 Notes: SYSTEM-ON-A-CHIP WITH MULTI-LAYERED METALLIZED THROUGH-HOLE INTERCONNECTION
Article notes should be on separate sheets

Source Title	SYSTEM-ON-A-CHIP WITH MULTI-LAYERED METALLIZED THROUGH-HOLE INTERCONNECTION
Source citation (APA Format)	T. Mimura, C. Christensen, Ahn et al. (2004). System-on-a-chip with multi-layered metallized through-hole interconnection. Patent Application No. 10/784,233. https://www.uspto.gov/patent/
Original URL	https://patents.google.com/patent/US7294921B2/en?q=(Semiconductor+manufacturing)&oq=Semiconductor+manufacturing&page=4
Source type	Patent
Keywords	
#Tags	
Summary of key points + notes (include methodology)	homeward bound so basically this pattern was about trying to mass produce a SoC. This is like a computer chip that is a Jack of all trades as it does basically everything that it should do. The problem with this is because of the so many processes going into creating this chip which leads it to being extremely inefficient as all those processes aren't very efficient to do together as there could be a multitude of issues. So this patent is basically patenting manufacturing strategy which they believe will be a better way to make a SoC. This invention basically has a couple things First off there's multi layered metalization as this technology uses multiple layers of wiring and insulations basically within the chip carrier to basically make it more efficient electrically it also has a short wiring paths so that it has the least amount of distance that the signals have to travel and also the controlled low empdancewiring ensures stable power.
Research Question/Problem/ Need	developing a SoC in the most efficient manufacturing process possible.

Important Figures	 FIG. 8

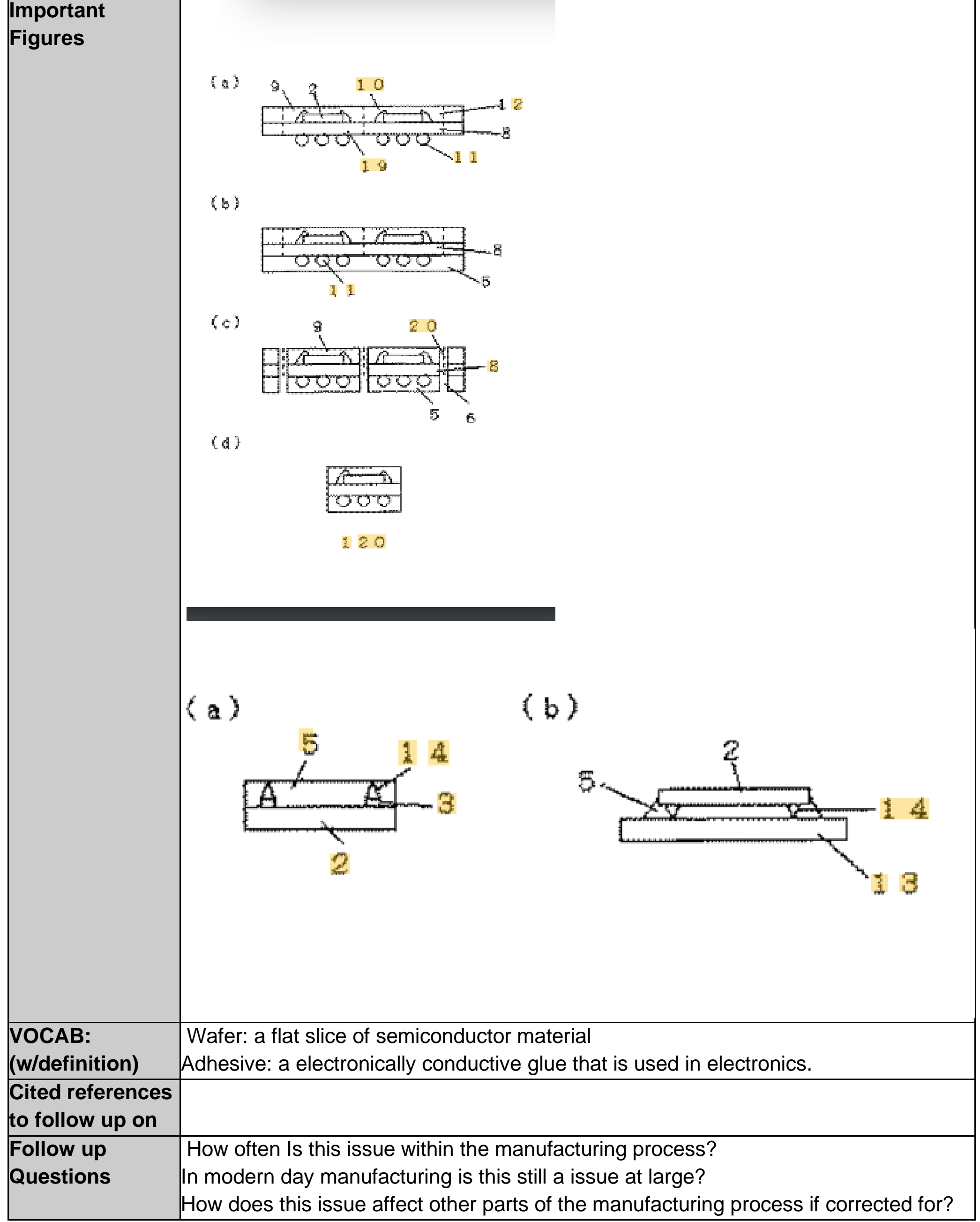
	 FIG. 4
VOCAB: (w/definition)	Multi-layer Metallized Through-Hole: a hole within the layers of of the semiconductor with copper Noise: is not noise like sound but instead interruptions during the passing of a electrical sighnal
Cited references to follow up on	
Follow up Questions	and the fabrication techniques and SoC be like different from like normal circuits? Why does noise affect the computer chip?

	What is the benefit of actually making an SoC if the manufacturing process is going to be worse instead of just making separate parts.

Patent #2 Notes: Method for manufacturing semiconductor device

Article notes should be on separate sheets

Source Title	Method for manufacturing semiconductor device
Source citation (APA Format)	Takahashi, A., & Ishida, Y. (2004). *Method for manufacturing semiconductor device* (Japan Patent Office Patent). https://patents.google.com/patent/JP2004311603A/en?oq=JP2004311603A.pdf
Original URL	https://patents.google.com/patent/JP2004311603A/en?oq=JP2004311603A.pdf
Source type	Patent
Keywords	Doping Defect p-type doping n-type doping
#Tags	
Summary of key points + notes (include methodology)	There is a problem basically, thin wafer's cannot be pasted ontop of a dicing sheet. The reason for this is normal adghesive that is seen within these semi conductors hardens causing it to be unable to be pasted onto the dicing sheet. The method bascall added a thin layer ontop and put it at its melting point. So doing this lead to it being a able to go again t the current problem succsefully.So basically this article talks about a problem in the semi conductor manufacturing problem caused by adhesive and to solve this issue that can add a layer boil it and the adhesive will still allow the wafer to be put to the dicing sheet without messing up the waer withi the process.
Research Question/Problem/ Need	Is their a way in the manufacturing process to maike it so wafer bonding will be able to be diced by sheet.

Important Figures	
VOCAB: (w/definition)	Wafer: a flat slice of semiconductor material Adhesive: a electronically conductive glue that is used in electronics.
Cited references to follow up on	
Follow up Questions	How often Is this issue within the manufacturing process? In modern day manufacturing is this still a issue at large? How does this issue affect other parts of the manufacturing process if corrected for?

Article #11 Notes: Defects in Semiconductors: Some Fatal, Some Vital

Article notes should be on separate sheets

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Source Title	Defects in Semiconductors:Some Fatal, Some Vital
Source citation (APA Format)	*Defects in Semiconductors: Some Fatal, Some Vital*. (n.d.). https://doi.org/10.1126/science.281.5379.945
Original URL	https://www.science.org/doi/epdf/10.1126/science.281.5379.945
Source type	Journal entry
Keywords	Doping: The process of introducing impurtoes too a semiconductor to allow for the flow of electricty to change Defect: Impurties in the sehymiconductor crystal structure that influence electrical flow p-type doping: adding impurities that create holes (positive charge) n-type doping: adding impurities that contribute free electrons (negative charge)
#Tags	
Summary of key points + notes (include methodology)	This article is about the change of semiconductors doping overtime and newer more advanced doping strategies and the miniaturization and defect control techniques of semiconductors. They talk about the use techniques of ion implantation and thermal annealing and the challenges of achieving an efficient p-type in some materials like GaN. Then it talks about the effects of dislocation on device performance and the effect it has on carrier lifetime. Than it talks about defect mitigation methods like gattering and passivation. Than we began too see some great results from new materials like dislocated GaN enabling blue light diodes and lasers.Than we began to delve back into advanced techniques in controlling defects in Si and Ge semiconductors by using lithium and hydrogen passively. This article the looks at isotompic composition and the development of emtal semiconductor interfaces and metastble defectles Dx cenyrt and EL@ defect are covers. The defects seen before influence the optoelectronic properties in group III-V semiconductor. Now we just conclude by talking about the change in doping overtime and the advancement going on in the field.

Research Question/Problem/ Need	The history and advancement of using doping too improve a semiconductor.
Important Figures	**Fig. 1.** Range of electrical resistivities of pure and donor-doped silicon single crystals shown in comparison with metals and insulators. **Fig. 2.** Atomic geometry and charge density contour surface of a nitrogen vacancy in GaN. Gallium atoms are green, nitrogen is blue, and the defect wave function is shown in pink. The strong interaction of the Ga dangling bonds pushes the donor level up into the conduction band; reprinted with permission from (*8*).

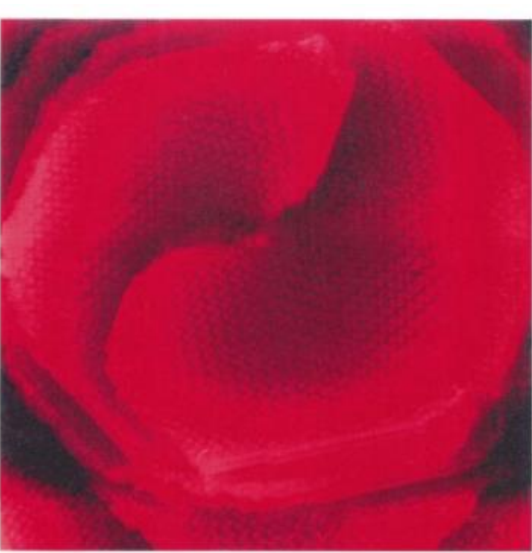
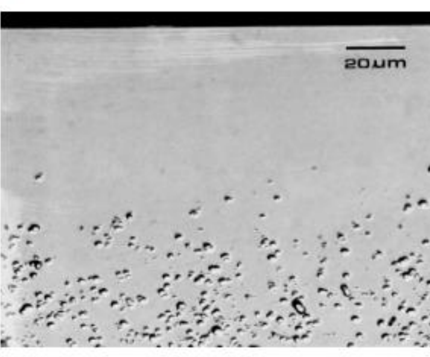


Fig. 3. Scanning tunneling micrograph of a single screw dislocation on a GaN crystal surface of wurtzite structure. Two Ga-N bilayer growth fronts surround the dislocation, and several reconstructed surface domains are clearly visible; reprinted with permission from (*13*).

Fig. 4. Cross-sectional view of the defect-free, near-surface region of a silicon wafer. The lower portion of the figure shows silicon dioxide precipitates used for impurity gettering; reprinted with permission from (*15*).



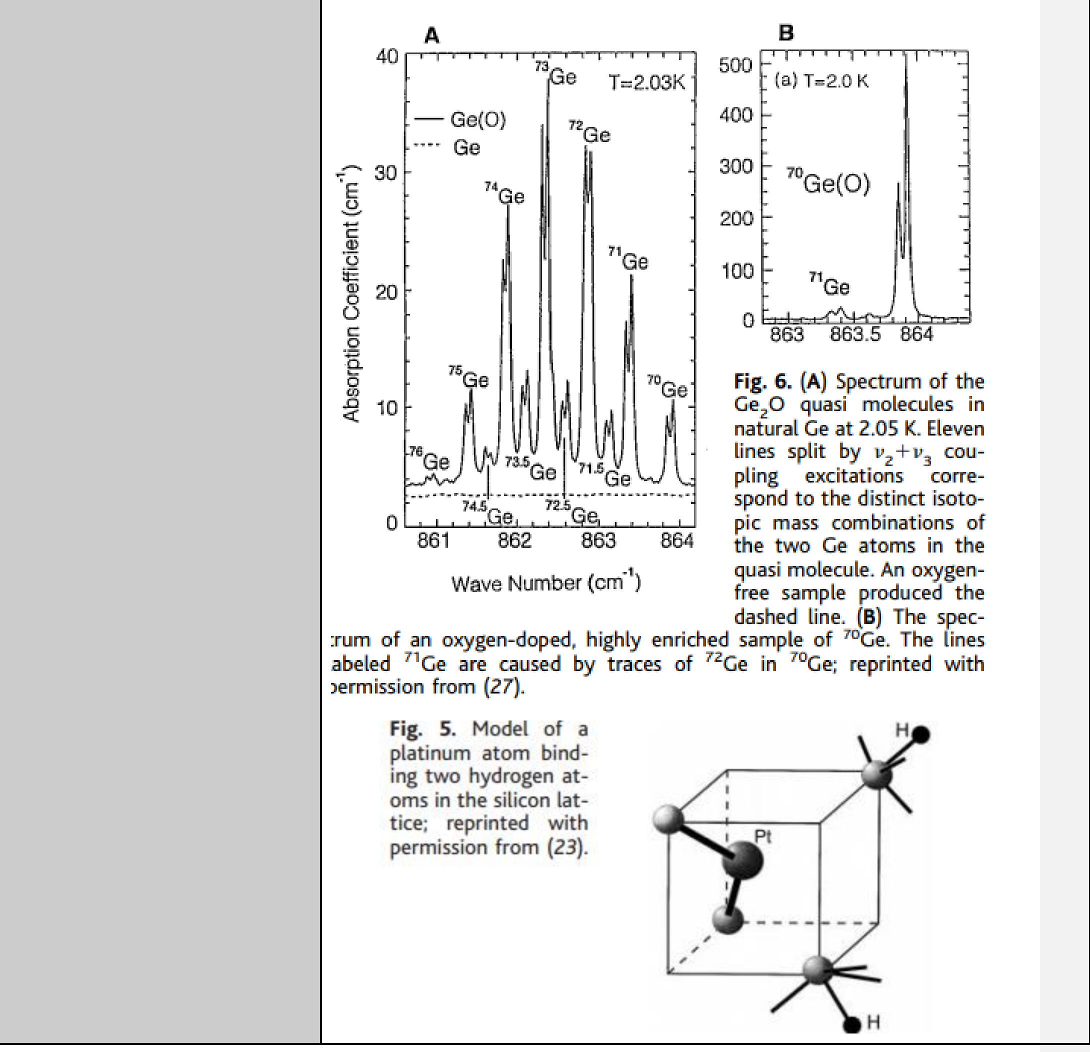
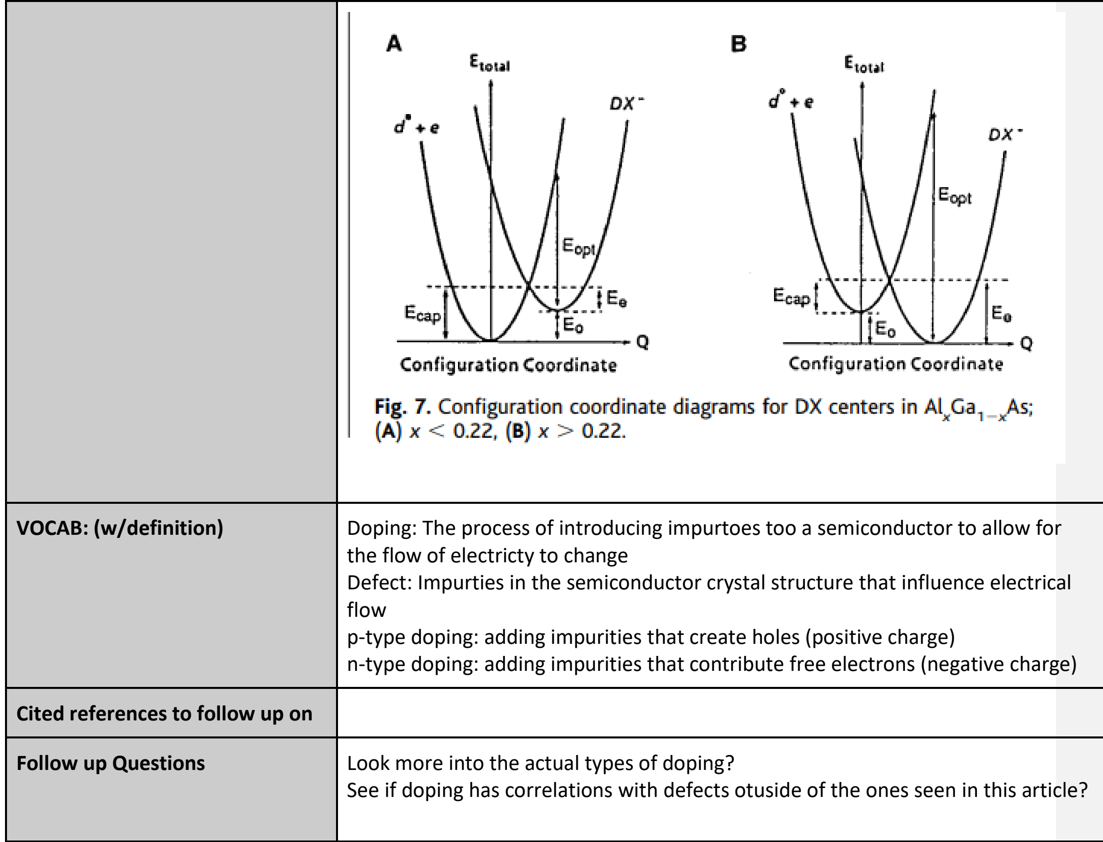


Fig. 6. (**A**) Spectrum of the Ge_2O quasi molecules in natural Ge at 2.05 K. Eleven lines split by $\nu_2+\nu_3$ coupling excitations correspond to the distinct isotopic mass combinations of the two Ge atoms in the quasi molecule. An oxygen-free sample produced the dashed line. (**B**) The spectrum of an oxygen-doped, highly enriched sample of ^{70}Ge. The lines labeled ^{71}Ge are caused by traces of ^{72}Ge in ^{70}Ge; reprinted with permission from (*27*).

Fig. 5. Model of a platinum atom binding two hydrogen atoms in the silicon lattice; reprinted with permission from (*23*).

	 **Fig. 7.** Configuration coordinate diagrams for DX centers in $Al_xGa_{1-x}As$; **(A)** $x < 0.22$, **(B)** $x > 0.22$.
VOCAB: (w/definition)	Doping: The process of introducing impurtoes too a semiconductor to allow for the flow of electricty to change Defect: Impurties in the semiconductor crystal structure that influence electrical flow p-type doping: adding impurities that create holes (positive charge) n-type doping: adding impurities that contribute free electrons (negative charge)
Cited references to follow up on	
Follow up Questions	Look more into the actual types of doping? See if doping has correlations with defects otuside of the ones seen in this article?

Article #12 Notes: Automatic classification of C-Sam Voids for Root cause Identification of Bonding Yield Degradation

Article notes should be on separate sheets

Source Title	Automatic Classification of C-SAM Voids for Root Cause Identification of Bonding Yield Degradation
Source citation (APA Format)	Baderot, J., Garrais, S., Martinez, S., Foucher, J., Eto, R., Tanida, K., Yasui, T., & Tanaka, T. (2023). Automatic Classification of C-SAM Voids for Root Cause

	Identification of Bonding Yield Degradation. *IEEE Transactions on Semiconductor Manufacturing*, *36*(4), 537–542. IEEE Transactions on Semiconductor Manufacturing. https://doi.org/10.1109/TSM.2023.3281135
Original URL	Automatic Classification of C-SAM Voids for Root Cause Identification of Bonding Yield Degradation | IEEE Journals & Magazine | IEEE Xplore
Source type	Journal Article
Keywords	C-Sam,
#Tags	
Summary of key points + notes (include methodology)	Within this article we see the use of c-sam too basically scan for voids and fid where all the voids are automatically by adding an alagaromthimo ontop of already using c sam within thew semionductor. Now that they can use an algorithm the computer can process faster if the void is fatal or not compared to comparebal methods like ai data sets and such. C sam is different than normal sam as it is constant depth mode measuring looking for voids at the same deopth theoufh the whole thing. The algorithms classify voids based on shape and size and are similar to my project idea. With this detection they were able to increase the semiconudtor yeild. They proposed qualty metric status to see what size and lengths had value within the algorithm to classify the semiconductor based on the void. This has major industry effects and can be used across the semiconductor industry within the future
Research Question/Problem/ Need	

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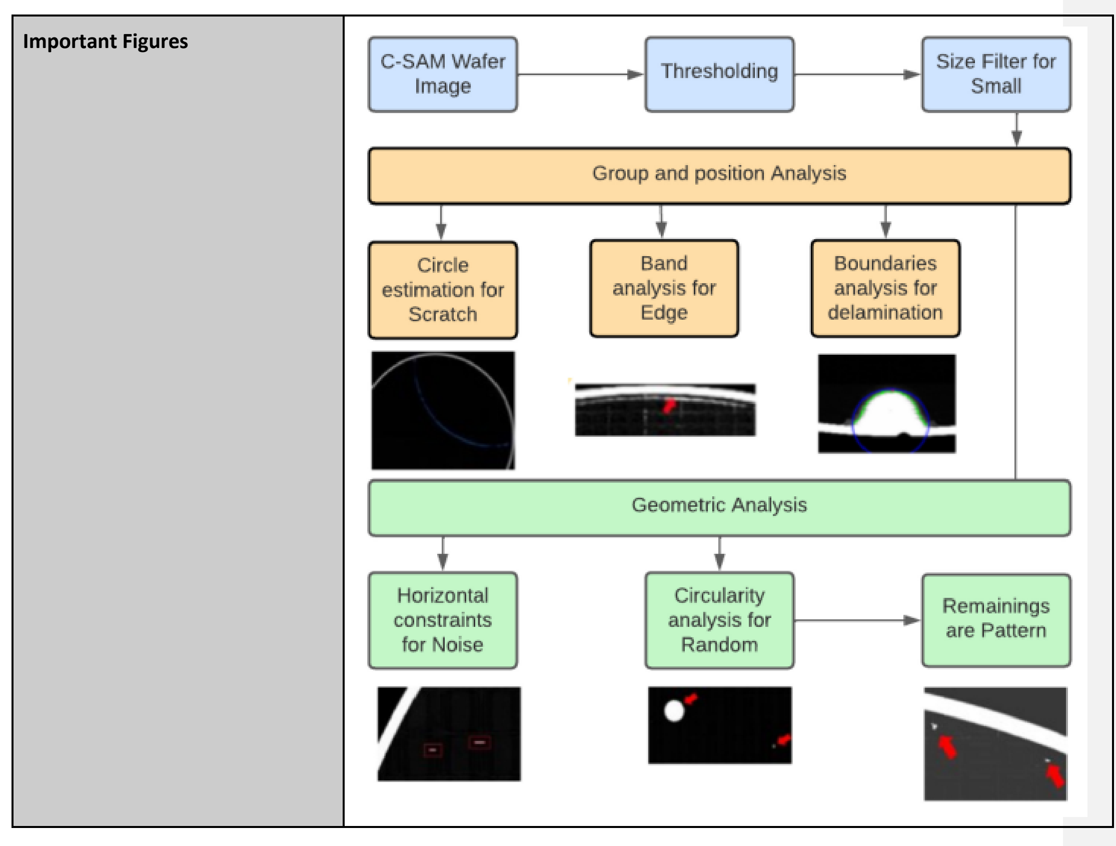
<td>Important Figures</td>
<td>
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TABLE I
MEASUREMENT IN FUNCTION OF DEFECT TYPE. "X" IS DEFINING WHICH MEASUREMENT IS COMPUTED FOR EACH DEFECT TYPE

Measurement	**Defect Type**			
	Scratch	Edge	Delamination	Geometric
Area/CalcArea	X	X	X	X
Arc Length	X	X		
Max Width	X	X	X	
Centroid			X	X
Length			X	X
Geometric				X

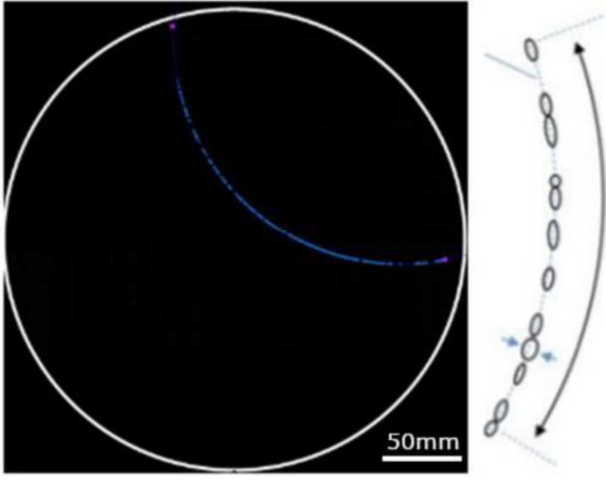


Fig. 4. Illustration of a scratch defect in blue on the left. Small pink dots are visible to show the extreme points for the arc length. On the right a more synthetic illustration explain with the curved arrow the arc length measurement and blue arrows the max width.

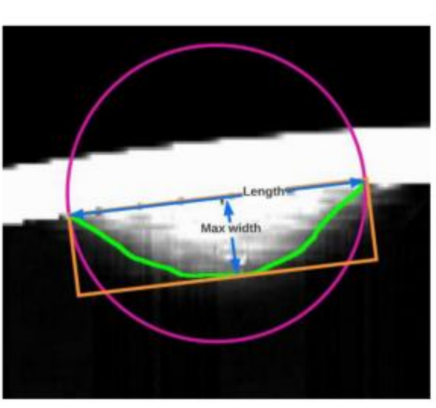
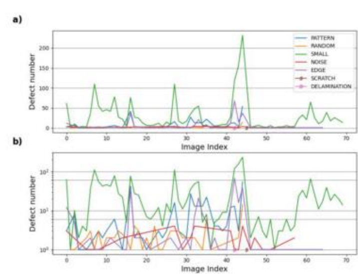


Fig. 5. Illustration of max width and length on a delamination defect. The width of the smallest rectangle enclosing the defect is the max width. The diameter of the enclosing circle correspond to the length.

TABLE II
CONFUSION MATRIX OF THE PROPOSED METHOD. "ADC" MEANS AUTOMATIC DEFECT CLASSIFICATION BY THE TOOL, AND "MANUAL CLASS" MEANS CLASSIFICATION BY AN ENGINEER

		ADC Class							
	Count	Delamination	Noise	Pattern	Random	Scratch	Small	Total	Row accuracy %
Manual class	Delamination	3	0	0	0	0	0	3	100.0%
	Noise	0	38	0	0	0	0	38	100.0%
	Pattern	0	1	198	9	0	0	208	95.2%
	Random	0	4	67	79	0	0	150	52.7%
	Scratch	0	0	0	0	3	0	3	100.0%
	Small	0	0	0	0	0	3552	3552	100.0%
	Total	3	43	265	88	3	3552	3954	
	Col accuracy %	100.0%	88.4%	74.7%	89.8%	100.0%	100.0%		98.0%



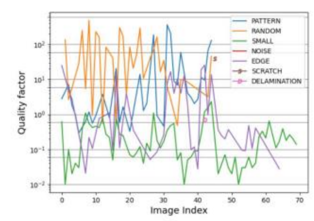
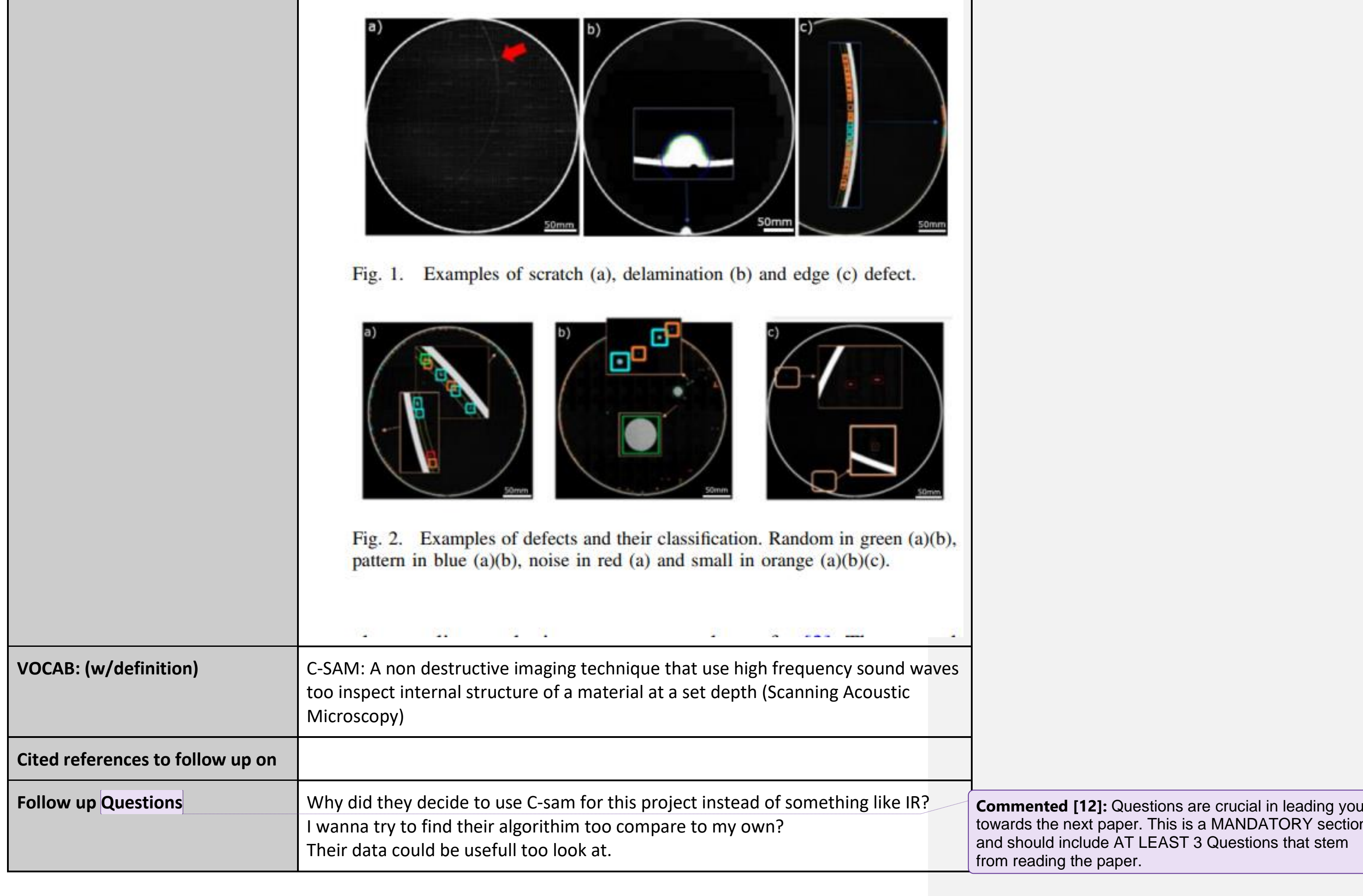


Fig. 7. Illustration of a quality factor proposition based on the defect number and calculated area in logarithmic scale.

	 Fig. 1. Examples of scratch (a), delamination (b) and edge (c) defect. Fig. 2. Examples of defects and their classification. Random in green (a)(b), pattern in blue (a)(b), noise in red (a) and small in orange (a)(b)(c).
VOCAB: (w/definition)	C-SAM: A non destructive imaging technique that use high frequency sound waves too inspect internal structure of a material at a set depth (Scanning Acoustic Microscopy)
Cited references to follow up on	
Follow up Questions	Why did they decide to use C-sam for this project instead of something like IR? I wanna try to find their algorithim too compare to my own? Their data could be usefull too look at.

Commented [12]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #13 Notes: Impact of Bonding Layer Voids Distribution Uniformity on the Thermal Performance of Light-Emitting Diode

Article notes should be on separate sheets

Source Title	Impact of Bonding Layer Voids Distribution Uniformity on the Thermal Performance of Light-Emitting Diode
Source citation (APA Format)	Yu, B., Liu, H., Yuan, Y., Li, J., Guo, J., Ding, X., & Li, Z.-T. (2024). Impact of Bonding Layer Voids Distribution Uniformity on the Thermal Performance of Light-Emitting Diode. *IEEE Transactions on Electron Devices*, *71*(3), 1980–1986. IEEE Transactions on Electron Devices. https://doi.org/10.1109/TED.2024.3351109
Original URL	
Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article describes a process for identifying voids/defects in the solder balls between electronic devices and circuit boards using automation. Automation reduces time it takes to scan a board, does a better job detecting voids and not detecting false positives. Solder balls are the conductive material used to connect electronic devices to the circuit board. The voids in the solder balls can cause the electronic devices to not work correctly. Usually voids are detected manually using X-ray. Manual detection of voids is not reliable because of other components and obstacles that can impact the image. Manal detection of voids can miss voids or cause false positives.
Research Question/Problem/ Need	Automating the use of x-ray too improve semiconduct

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<td>Important Figures</td>
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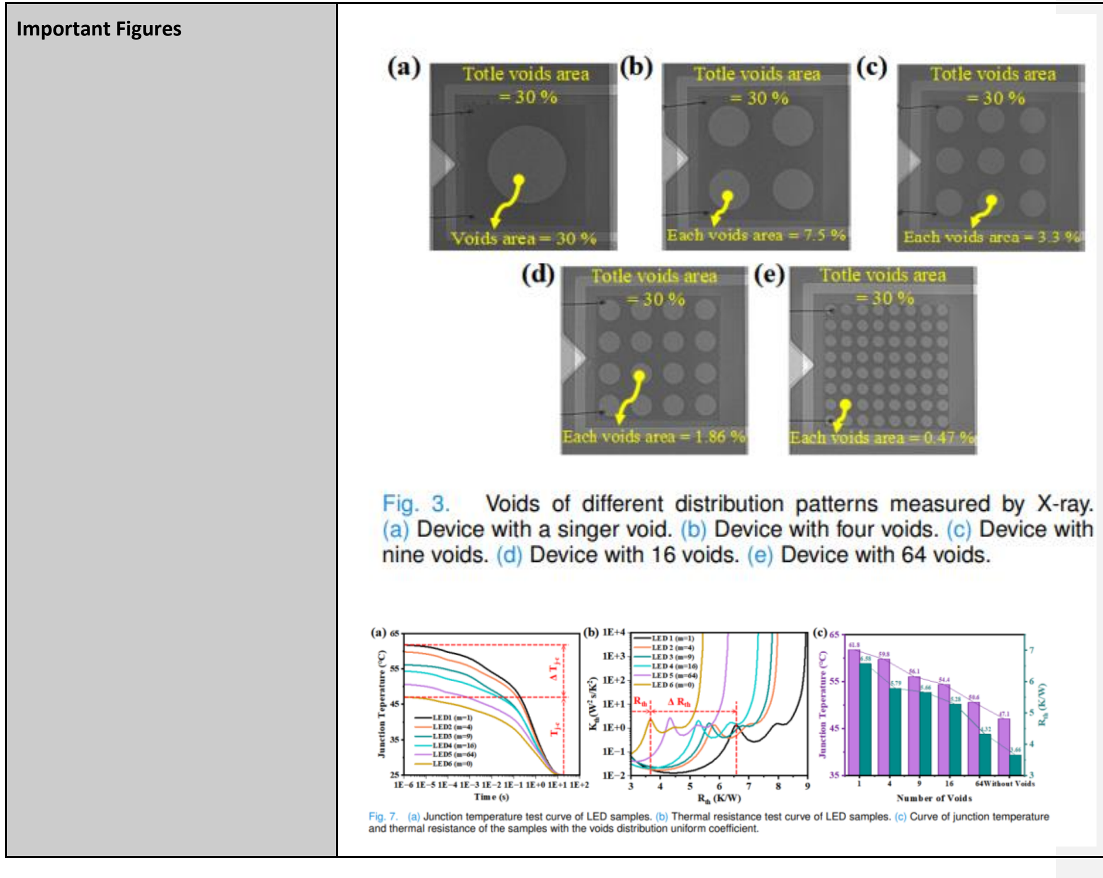

Fig. 3. Voids of different distribution patterns measured by X-ray. (a) Device with a singer void. (b) Device with four voids. (c) Device with nine voids. (d) Device with 16 voids. (e) Device with 64 voids.

Fig. 7. (a) Junction temperature test curve of LED samples. (b) Thermal resistance test curve of LED samples. (c) Curve of junction temperature and thermal resistance of the samples with the voids distribution uniform coefficient.
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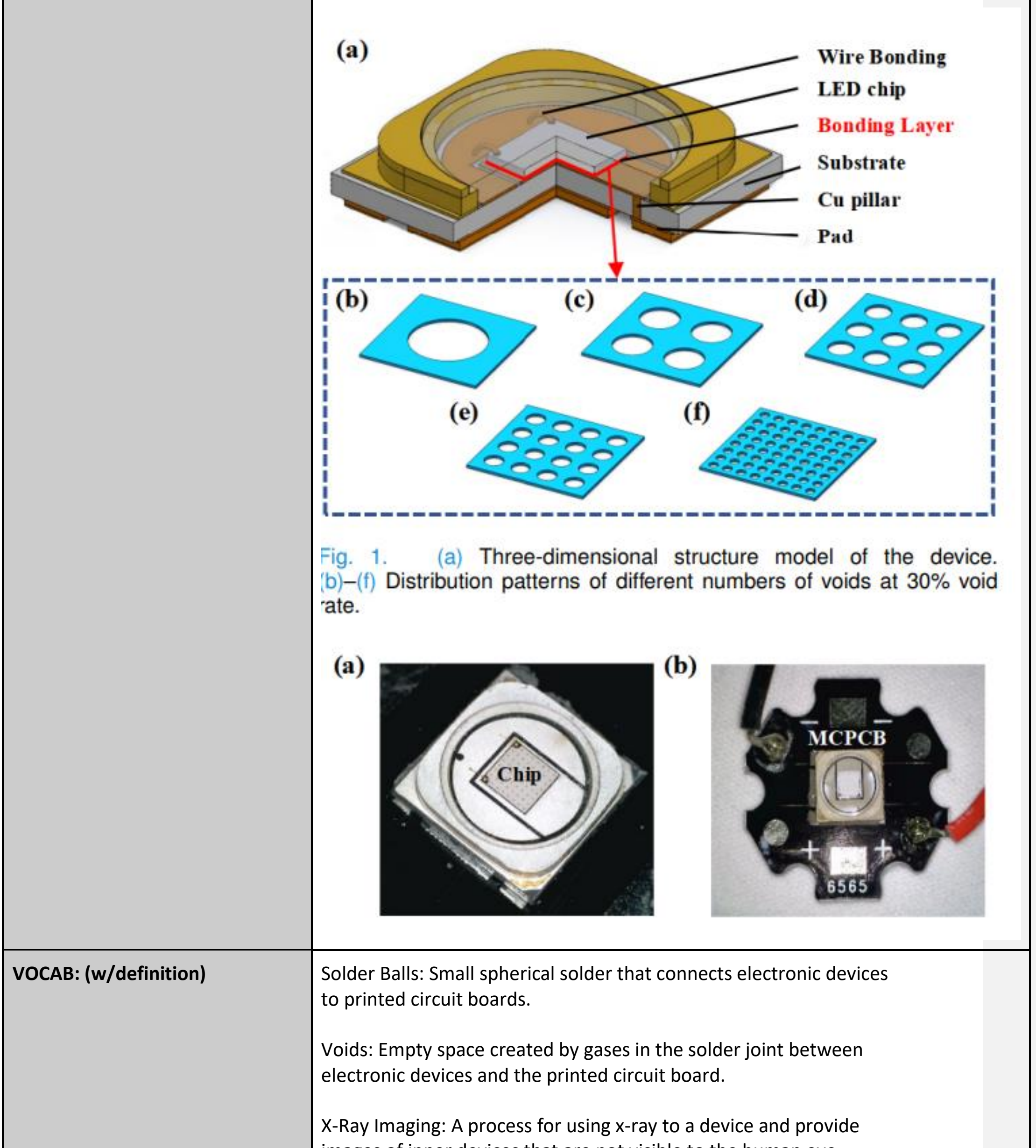
	 Fig. 1. (a) Three-dimensional structure model of the device. (b)–(f) Distribution patterns of different numbers of voids at 30% void rate.
VOCAB: (w/definition)	Solder Balls: Small spherical solder that connects electronic devices to printed circuit boards. Voids: Empty space created by gases in the solder joint between electronic devices and the printed circuit board. X-Ray Imaging: A process for using x-ray to a device and provide images of inner devices that are not visible to the human eye.

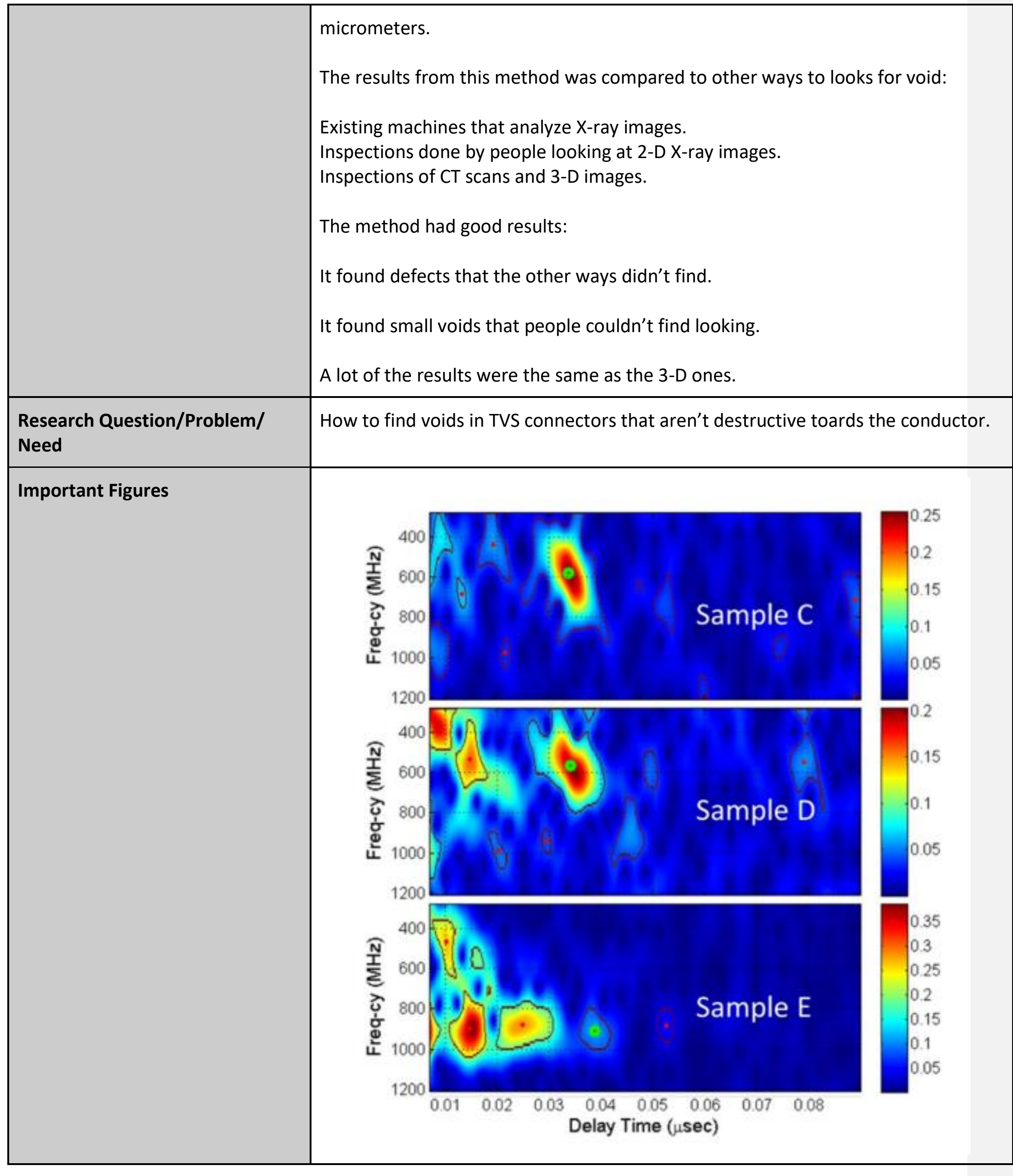
Cited references to follow up on	
Follow up Questions	Can X-Ray imaging be used to detect other types of defects? What other imaging technologies can be used to detect voids/defects? What are the most common causes of manufacturing failures?

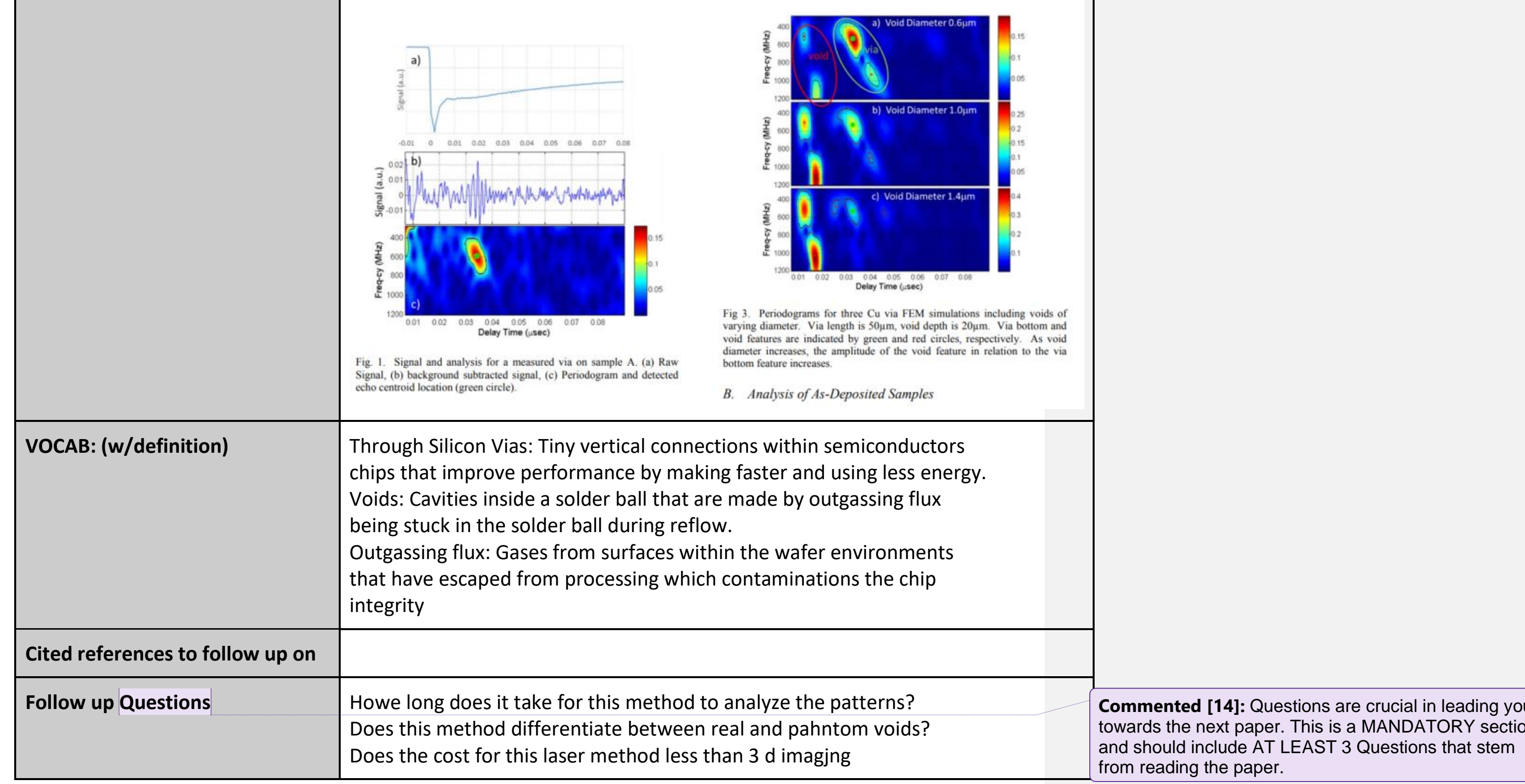
Commented [13]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #14 Notes: Non-Destructive Acoustic Metrology and Void Detection in 3x50µm TSV

Article notes should be on separate sheets

Source Title	Non-Destructive Acoustic Metrology and Void Detection in 3x50µm TSV
Source citation (APA Format)	Mair, R., Kotelyanskii, M., Mehendale, M., Ru, X., Mukundhan, P., Kryman, T., Liebens, M., Van Huylenbroeck, S., Haensel, L., Miller, A., Beyne, E., & Murray, T. (2016). Non-destructive acoustic metrology and void detection in 3×50µm TSV. *2016 27th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, 54–59. https://doi.org/10.1109/ASMC.2016.7491103
Original URL	https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7491103
Source type	Journal Article
Keywords	Through Silicon Vias, Voids Outgassing
#Tags	
Summary of key points + notes (include methodology)	This article explains how voids in TVS connectors on semiconductors can be found using acoustic metrology. This is important because voids in semiconductor chips can cause them not to work to right. Lasers and soundwaves can find voids in TVS without being destructive to chips and the article explains that lasers and sound waves can find the voids. The laser and sound waves go through the TVS and then they see how the waves bounce. It makes different patterns and then you can see how they are the same and not same and be able to analyze where are the voids. This is a non-destructive method because the laser and sound doesn't hurt the chip but can find the voids. It is a good method also because it can find defects that are really small like 0.4

	micrometers. The results from this method was compared to other ways to looks for void: Existing machines that analyze X-ray images. Inspections done by people looking at 2-D X-ray images. Inspections of CT scans and 3-D images. The method had good results: It found defects that the other ways didn't find. It found small voids that people couldn't find looking. A lot of the results were the same as the 3-D ones.
Research Question/Problem/ Need	How to find voids in TVS connectors that aren't destructive toards the conductor.
Important Figures	

	 Fig. 1. Signal and analysis for a measured via on sample A. (a) Raw Signal, (b) background subtracted signal, (c) Periodogram and detected echo centroid location (green circle). Fig 3. Periodograms for three Cu via FEM simulations including voids of varying diameter. Via length is 50μm, void depth is 20μm. Via bottom and void features are indicated by green and red circles, respectively. As void diameter increases, the amplitude of the void feature in relation to the via bottom feature increases. *B. Analysis of As-Deposited Samples*
VOCAB: (w/definition)	Through Silicon Vias: Tiny vertical connections within semiconductors chips that improve performance by making faster and using less energy. Voids: Cavities inside a solder ball that are made by outgassing flux being stuck in the solder ball during reflow. Outgassing flux: Gases from surfaces within the wafer environments that have escaped from processing which contaminations the chip integrity
Cited references to follow up on	
Follow up Questions	Howe long does it take for this method to analyze the patterns? Does this method differentiate between real and pahntom voids? Does the cost for this laser method less than 3 d imagjng

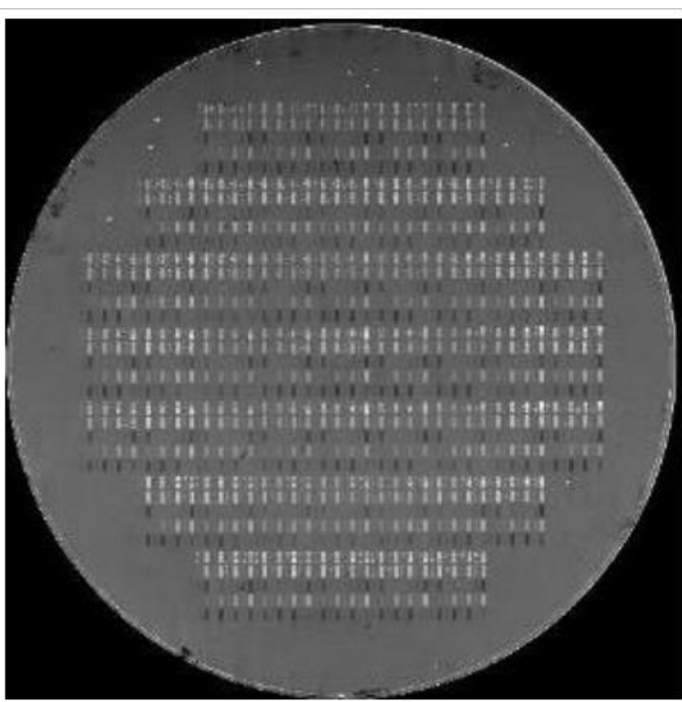
Commented [14]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #14 Notes: Infrared Optical Solutions for Void Inspection of Bonded Wafers

Article notes should be on separate sheets

Source Title	Infrared Optical Solutions for Void Inspection of Bonded Wafers
Source citation (APA Format)	Nádudvari, G., Kiss, Z., Dobos, C., Bodoky, L., Kovács, Z., Molnár, G., Száz, D., Poppa, S., & Balogh, I. (2024). Infrared Optical Solutions for Void Inspection of Bonded Wafers. *2024 IEEE 10th Electronics System-Integration Technology*

	Conference (ESTC), 1–4. https://doi.org/10.1109/ESTC60143.2024.10712076
Original URL	https://ieeexplore.ieee.org/abstract/document/10712076?casa_token=DWBJYYfLRzUAAAAA:AVhqEHva5GkLniqAUIq25WSSbIMniC9JQGViTirKR6qf9Eo1gycZHimXE_S8QhKwttuyQyk
Source type	Journal Articlee
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article is about finding new ways of detecting voids in semiconductors using infrared optical techniques that are available. This is important because voids can lead to device failure. Traditional methods of finding voids have limitations especially when a wafer is thick or there is metal blocking light. Infrared light through the use of Polarized Stress Imaging can look through the silicon wafer to find voids and their associated stress fields. By being able to see thorough the silicon with infrared light the authors could find the gaps. They did this in the following ways: · One method found voids in general. · One method looked to find the stress patterns caused by the defects. · One method was a zoom to find miniscule voids. The study had good results and showed that IR was highly effective for detecting voids and stress.
Research Question/Problem/ Need	Find new ways to detet voids in semiconductors

Important Figures	 Fig. 2. 1.25X magnification IRI fullmap of sample A that contain 40 nm deep artificial voids. Large process induced voids are visible on non-patterned reas as well as a delamination ring along the wafer edge.

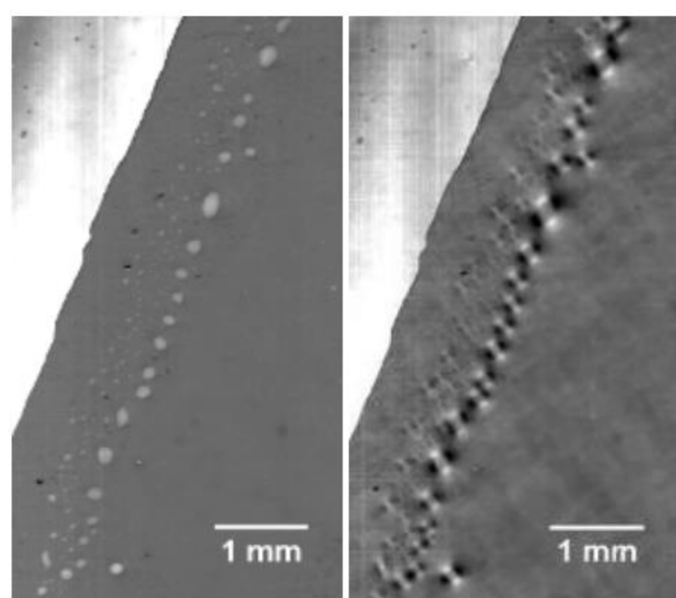
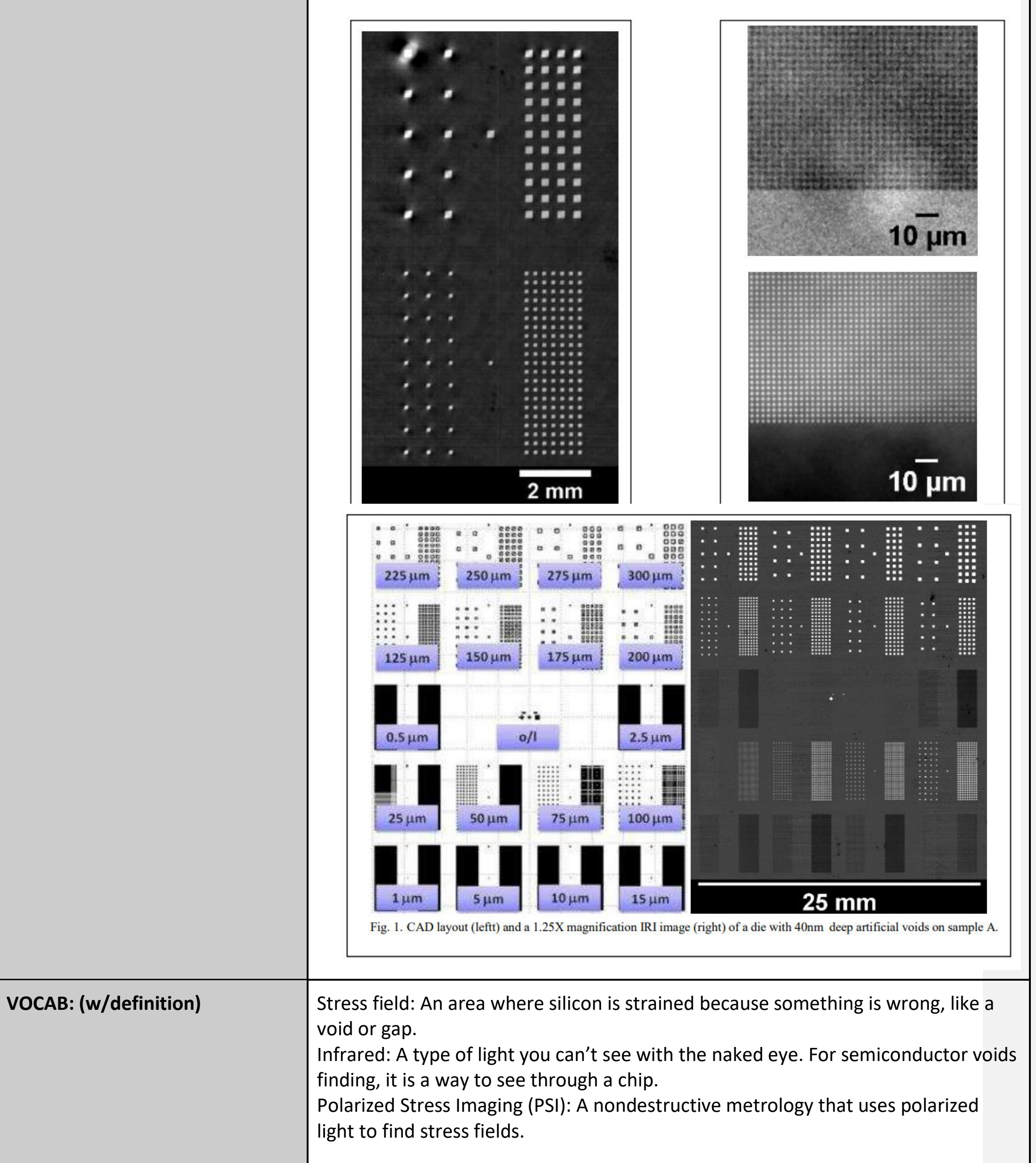


Fig. 4. 5X magnification IRI image of the wafer edge on sample B (left) and the image of the same site in stress enhanced mode (right). The delamination ring can be seen on the upper left corners. Process induced voids of various sizes run along the wafer edge next to the delamination.

	 Fig. 1. CAD layout (leftt) and a 1.25X magnification IRI image (right) of a die with 40nm deep artificial voids on sample A.
VOCAB: (w/definition)	Stress field: An area where silicon is strained because something is wrong, like a void or gap. Infrared: A type of light you can't see with the naked eye. For semiconductor voids finding, it is a way to see through a chip. Polarized Stress Imaging (PSI): A nondestructive metrology that uses polarized light to find stress fields.

Cited references to follow up on	
Follow up Questions	Does the heat from the IR affect the chip? How much expertise does someone need to use these IR methods Can this method differentiate between real and phantom voids?

Commented [15]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #15 Notes: Voids, Cracks, and Hot Spots in Die Attach

Article notes should be on separate sheets

Source Title	). Voids, Cracks, and Hot Spots in Die Attach
Source citation (APA Format)	Carlson, R. O., Yerman, A. J., Burgess, J. F., & Neugebauer, C. A. (1983). Voids, Cracks, and Hot Spots in Die Attach. *21st International Reliability Physics Symposium*, 138–141. https://doi.org/10.1109/IRPS.1983.361974
Original URL	https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4208495
Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article basically delve into how defects like voids and cracks and solar layers of semiconductors can affect the performance of the semiconductor, and how reliable that semiconductor will be in the long run. Shoulder layers are crucial for connecting parts of a semiconductor device and for helping it release heat, but voids and cracks in this layer can grow overtime because of the temperature changes when a semiconductor is on leading to problems like over a heating and just making the semiconductor less efficient so the research researchers talk about two types of avoids, cold, voids, and voids cold voids block, both heat and electricity in some spots, making the currents go through the smallest region possible this can lead to the device not heating up correctly and it'll just be less efficient as a Else. It is a hot Theut or a hotspot so they allow electricity to pass but block heat flow this makes it so that all the heat gets together and making super hotspots that can overheat like a specific part of the semiconductor and they're

	especially dangerous because high temperatures are only gonna worsen overtime which will lead to device failure and a lot of cases. This article then talks about ways to see that this problem is occurring and how they can minimize it they talk about how they can see it using x-ray imaging to detect the voids and solder layers and different soldering materials and techniques that could help reduce the formation avoids if we can address these defects and understand them, we can make semiconductors more reliable.
Research Question/Problem/ Need	Attempt to findout when different failures occur and what voids cause them
Important Figures	
VOCAB: (w/definition)	Voids: airpokets in semicondter layers Hot spots: a area on a semiconductor is overheatin
Cited references to follow up on	
Follow up Questions	Why did they decide to lock in on the die part of the semiconductor. How would they actually test the semiconductors. Where can I find their excel sheet?

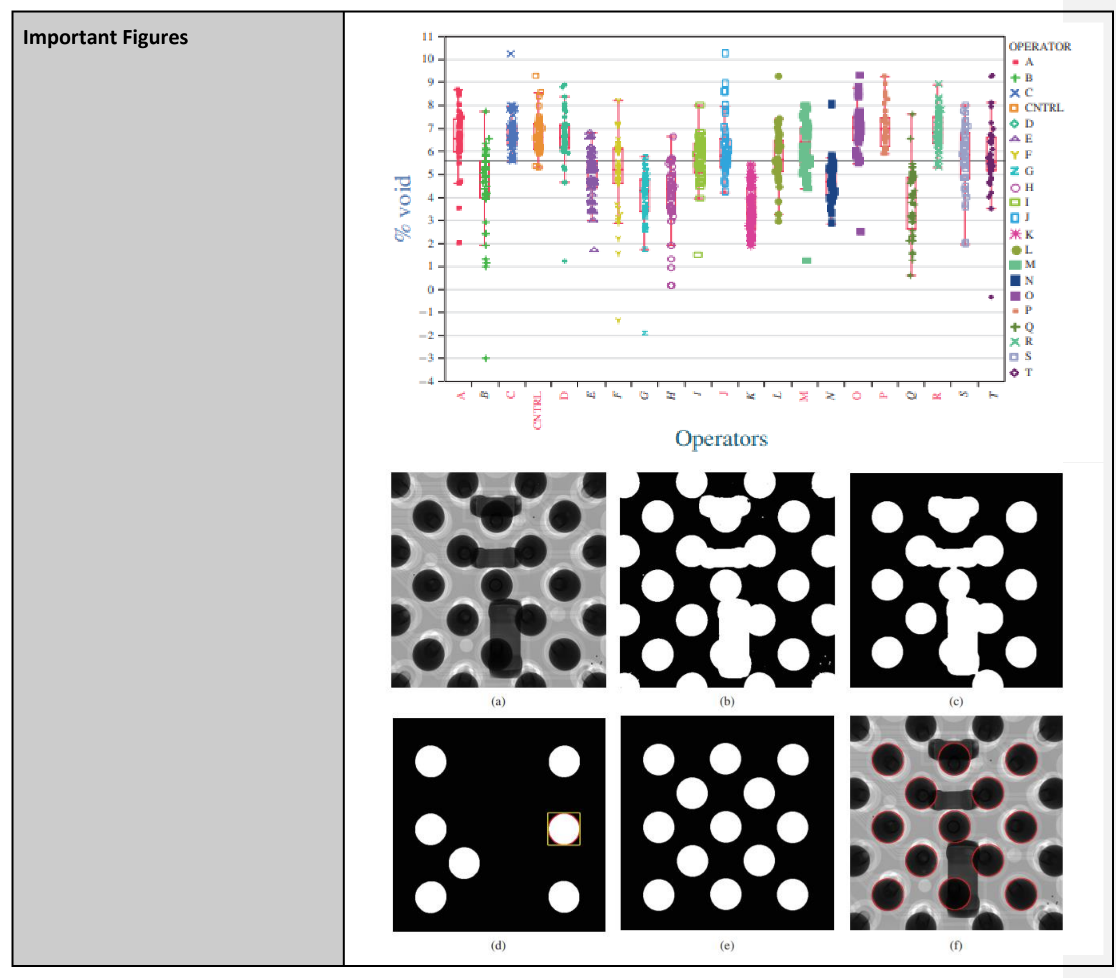
Commented [16]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

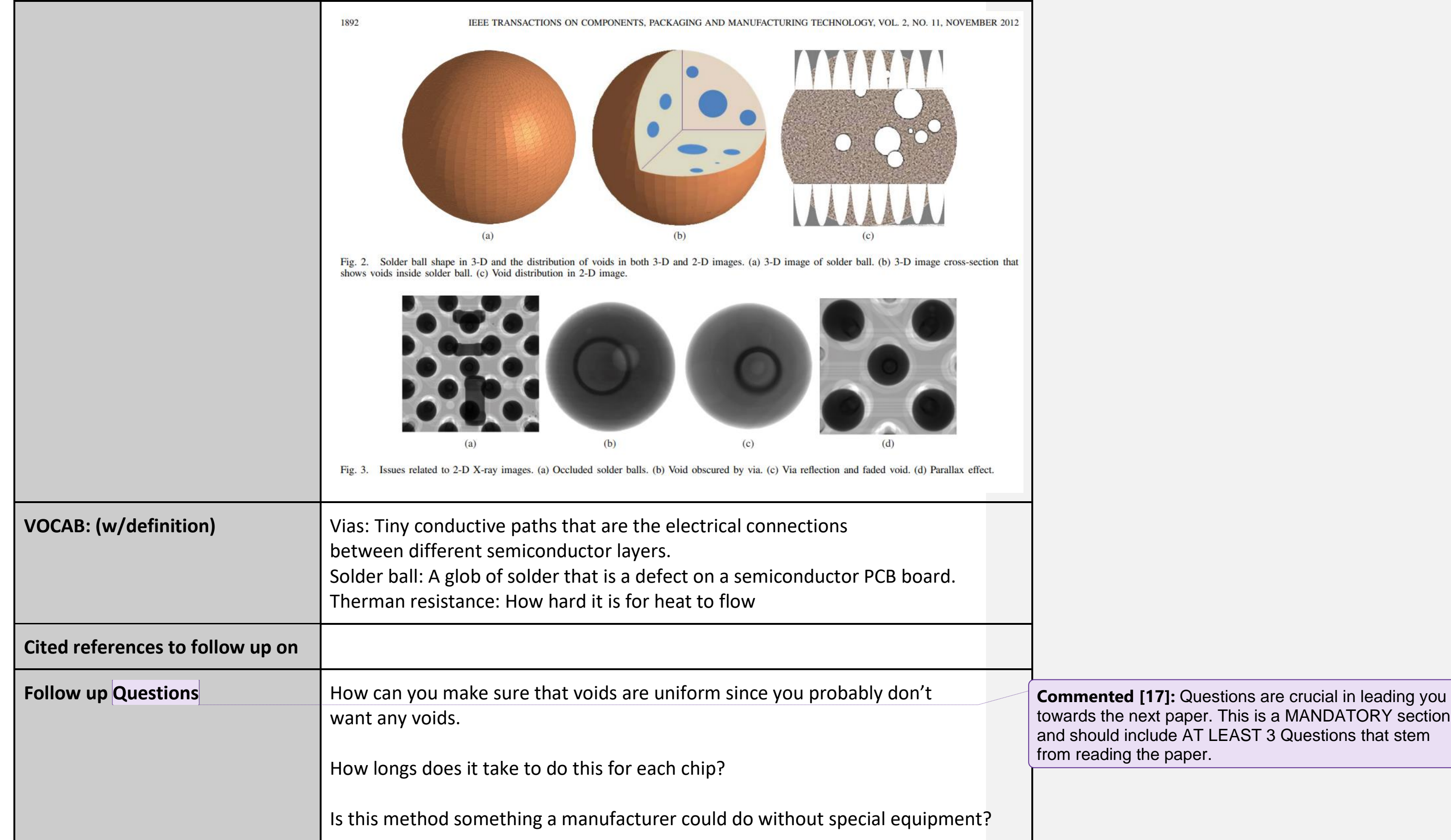
Article #16 Notes: Automated Void Detection in Solder Balls in the Presence of Vias and Other Artifacts

Article notes should be on separate sheets

Source Title	Automated Void Detection in Solder Balls in the Presence of Vias and Other Artifacts
Source citation (APA Format)	Said, A. F., Bennett, B. L., Karam, L. J., Siah, A., Goodman, K., & Pettinato, J. S. (2012). Automated Void Detection in Solder Balls in the Presence of Vias and Other Artifacts. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, *2*(11), 1890–1901. IEEE Transactions on Components, Packaging and Manufacturing Technology. https://doi.org/10.1109/TCPMT.2011.2182613
Original URL	https://ieeexplore.ieee.org/abstract/document/6317150?casa_token=5qeFiwovZvIAAAAA:sA7os3ilvxLfX0e6WTFLfrqy2rXJ-6mIlZ-iC0k5SiOeU0bnkmS8_X-DZkZGUyq0PB_J_0Q

Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article is about finding an improved automatic method for finding semiconductor voids with minimal phantom void creation. The article is mostly about finding voids within bonding layer of light-emitting diodes (LEDs) on their ability to dissipate heat effectively. LEDs get hot during operation and can slow performance if it gets too hot and lead to failure. The method in this article calculates a "void distribution uniformity coefficient" to calculate how even the voids are. They found that when voids are even, the bonding layer takes the heat flow better and the LED doesn't get as hot which means they will faill less. The method is done by the following: Identifying solder balls: Each solder ball is located in a way that work even with things that make it hard to find them, like bad lighting. Finding vias: This is important because it can mess up the results. Tracing defects: Edges of defects are traced and the missing outlies get filled in. Remove irrelevant things: The method ignores reflections or things so they don't mess up the result. The testing done by the authors were validated using Xrays. It found that if they could improve void distribution uniformity temeraturs on the chip went down 18% and thermal resistance was 34% bett
Research Question/Problem/ Need	Is it possible to improve heat resitance to improve failue rate of chips

Important Figures	

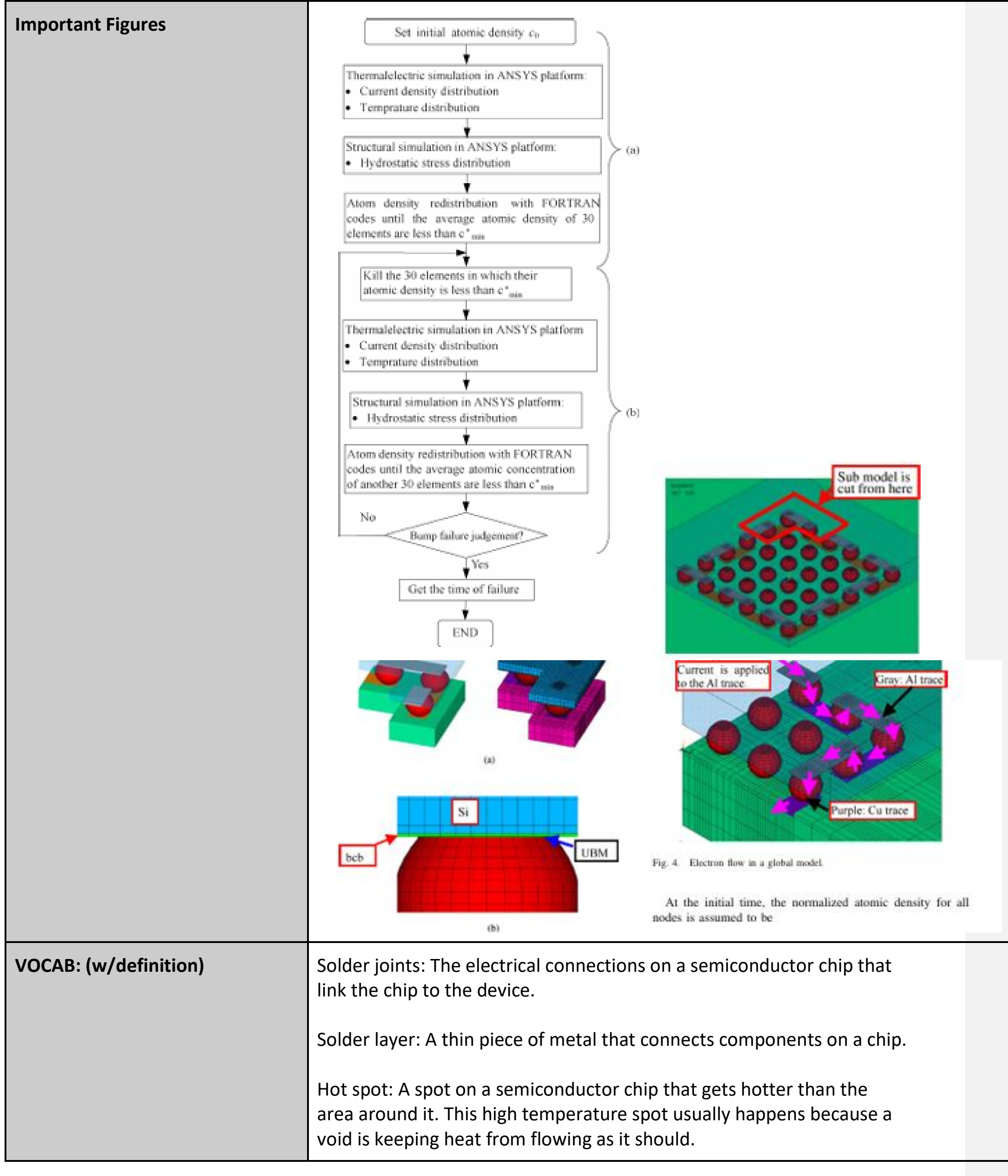
	 Fig. 2. Solder ball shape in 3-D and the distribution of voids in both 3-D and 2-D images. (a) 3-D image of solder ball. (b) 3-D image cross-section that shows voids inside solder ball. (c) Void distribution in 2-D image. Fig. 3. Issues related to 2-D X-ray images. (a) Occluded solder balls. (b) Void obscured by via. (c) Via reflection and faded void. (d) Parallax effect.
VOCAB: (w/definition)	Vias: Tiny conductive paths that are the electrical connections between different semiconductor layers. Solder ball: A glob of solder that is a defect on a semiconductor PCB board. Therman resistance: How hard it is for heat to flow
Cited references to follow up on	
Follow up Questions	How can you make sure that voids are uniform since you probably don't want any voids. How longs does it take to do this for each chip? Is this method something a manufacturer could do without special equipment?

Commented [17]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #17 Notes: Prediction of Electromigration Induced Voids and Time to Failure for Solder Joint of a Wafer Level Chip Scale Package

Article notes should be on separate sheets

Source Title	Prediction of Electromigration Induced Voids and Time to Failure for Solder Joint of a Wafer Level Chip Scale Package.
Source citation (APA Format)	Liu, Y., Zhang, Y., & Liang, L. (2010). Prediction of Electromigration Induced Voids and Time to Failure for Solder Joint of a Wafer Level Chip Scale Package. *IEEE Transactions on Components and Packaging Technologies*, *33*(3), 544–552. IEEE Transactions on Components and Packaging Technologies. https://doi.org/10.1109/TCAPT.2010.2042717
Original URL	https://ieeexplore.ieee.org/abstract/document/5462959?casa_token=ywq_mFMoLwsAAAAA:Ahkoyae8brwQ-RuGZVB_ZDZy1zdA6ezX_lU9pyv8GLtoqv999UXFQVOm-P9WPBoy9F5ZYG0
Source type	Journal Article
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article discusses a new method for predicting when and where voids will happened in solder joints for semiconductor chips. This is needed because voids can cause devices to fail. The soldering on a chip can have its atoms shift after a long period of time due to the electrical current and voids will form. This article uses a model to show how voids happen and incorporates a new way of incorportating things like electrical current and heat over time and their impact. The article explains how the model can predict the exact location and size of voids and can tell how long until failure. They tested their model with different materials and learned that some materials perform better than others. Solder joints made of lead did not work as well as solder joints with non-lead. Their research also showed that the shape can have an impact, too. The idea is that understanding these things can help semiconductor manufacturers design chips with solder joints using proper materials and in the best shapes to reduce void and failures.
Research Question/Problem/ Need	Can you predict where and when voids will happened in a semiconductor?

Important Figures	 Fig. 4. Electron flow in a global model. At the initial time, the normalized atomic density for all nodes is assumed to be
VOCAB: (w/definition)	Solder joints: The electrical connections on a semiconductor chip that link the chip to the device. Solder layer: A thin piece of metal that connects components on a chip. Hot spot: A spot on a semiconductor chip that gets hotter than the area around it. This high temperature spot usually happens because a void is keeping heat from flowing as it should.

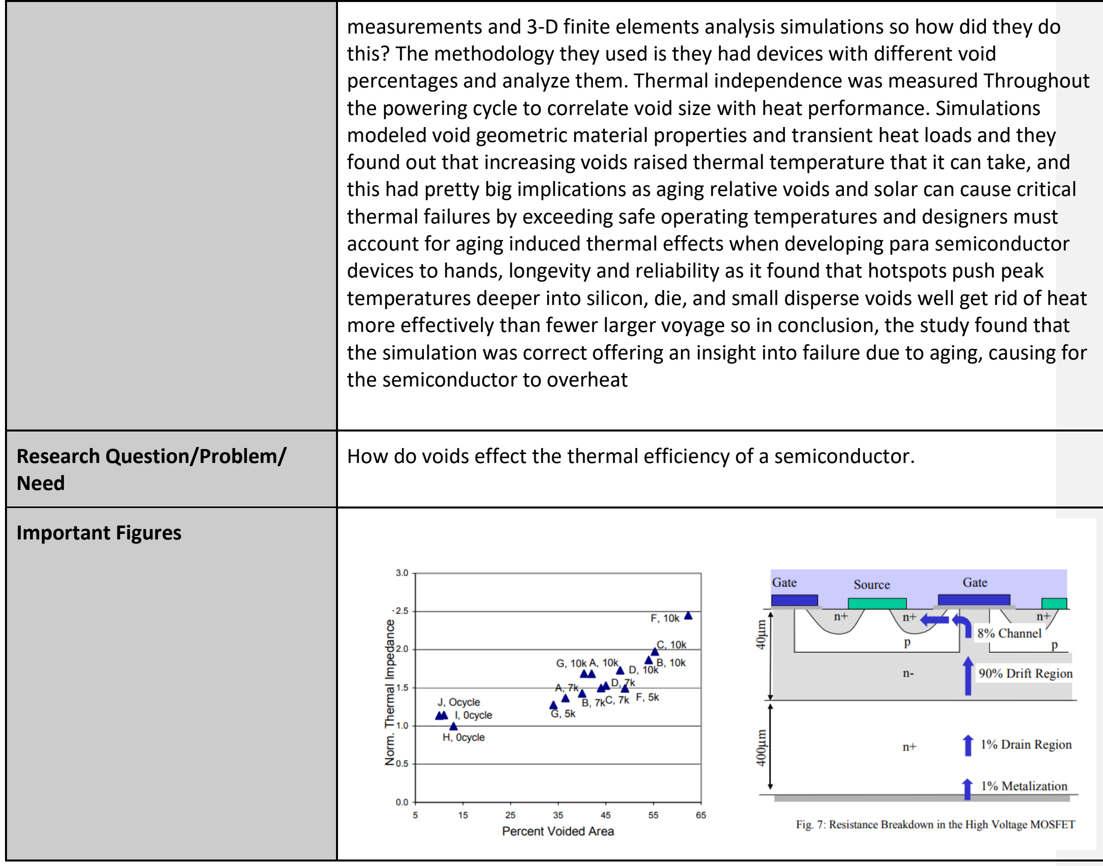
Cited references to follow up on	
Follow up Questions	What materials are typically used for solder joints? How much more time to failure does changing the shape or material give you? Can this method help prevent voids from forming at all?

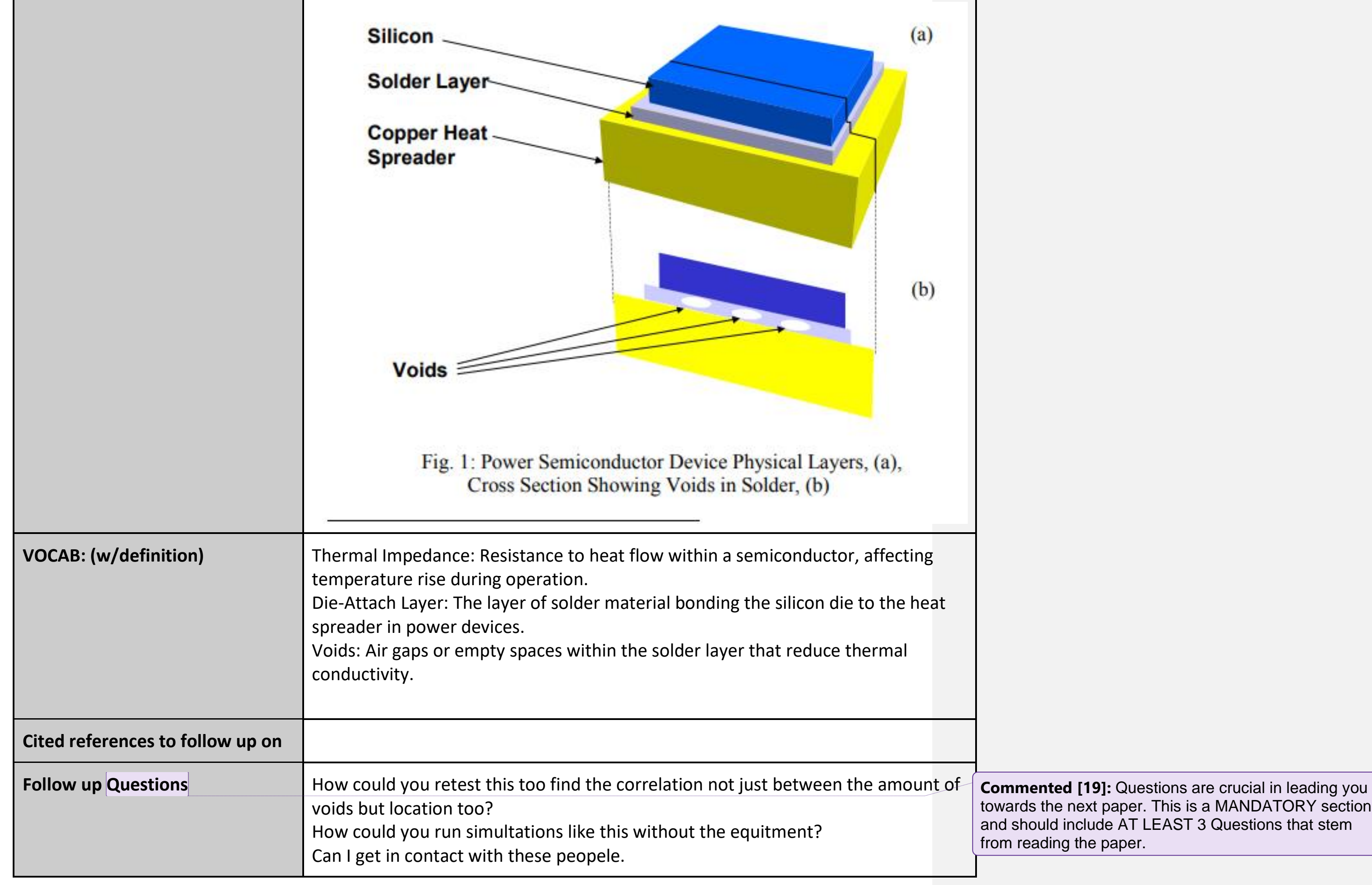
Commented [18]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #18 Notes: Experimental measurement and simulation of thermal performance due to aging in power semiconductor devices

Article notes should be on separate sheets

Source Title	). Experimental measurement and simulation of thermal performance due to aging in power semiconductor devices
Source citation (APA Format)	Katsis, D. C., & van Wyk, J. D. (2002). Experimental measurement and simulation of thermal performance due to aging in power semiconductor devices. *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, *3*, 1746–1751 vol.3. https://doi.org/10.1109/IAS.2002.1043769
Original URL	
Source type	
Keywords	
#Tags	
Summary of key points + notes (include methodology)	Basically, this article talks about how aging impacts the thermal performance of power, semiconductors and focuses more on void formation in solar, die attach layer. To began to talked about power cycling, causing mechanical stress and semiconductor devices leading to cracks and voids in the solid layers between the silicon and the heat spreader, and these voids reduce the thermal conductivity by this creating hotspots lowering the devices reliability overtime. So what the study was trying to investigate with the relationship between voided area and the diet touch layer and the thermal performance of MOSFETs using experimental

	measurements and 3-D finite elements analysis simulations so how did they do this? The methodology they used is they had devices with different void percentages and analyze them. Thermal independence was measured Throughout the powering cycle to correlate void size with heat performance. Simulations modeled void geometric material properties and transient heat loads and they found out that increasing voids raised thermal temperature that it can take, and this had pretty big implications as aging relative voids and solar can cause critical thermal failures by exceeding safe operating temperatures and designers must account for aging induced thermal effects when developing para semiconductor devices to hands, longevity and reliability as it found that hotspots push peak temperatures deeper into silicon, die, and small disperse voids well get rid of heat more effectively than fewer larger voyage so in conclusion, the study found that the simulation was correct offering an insight into failure due to aging, causing for the semiconductor to overheat
Research Question/Problem/ Need	How do voids effect the thermal efficiency of a semiconductor.
Important Figures	 Fig. 7: Resistance Breakdown in the High Voltage MOSFET

	 Fig. 1: Power Semiconductor Device Physical Layers, (a), Cross Section Showing Voids in Solder, (b)
VOCAB: (w/definition)	Thermal Impedance: Resistance to heat flow within a semiconductor, affecting temperature rise during operation. Die-Attach Layer: The layer of solder material bonding the silicon die to the heat spreader in power devices. Voids: Air gaps or empty spaces within the solder layer that reduce thermal conductivity.
Cited references to follow up on	
Follow up Questions	How could you retest this too find the correlation not just between the amount of voids but location too? How could you run simultations like this without the equitment? Can I get in contact with these peopele.

Commented [19]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #19 Notes: Evaluation of Hybrid Bonding Interface Quality by Contact Resistivity Measurement

Article notes should be on separate sheets

Source Title	Evaluation of Hybrid Bonding Interface Quality by Contact Resistivity Measurement
Source citation (APA Format)	Jourdon, J., Lhostis, S., Moreau, S., Bresson, N., Salomé, P., & Frémont, H. (2019). Evaluation of Hybrid Bonding Interface Quality by Contact Resistivity Measurement. *IEEE Transactions on Electron Devices*, *66*(6), 2699–2703. IEEE Transactions on Electron Devices. https://doi.org/10.1109/TED.2019.2910528
Original URL	https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8698310
Source type	
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This article is about hybrid bonding and how it can be used to tell the quality of connections in a semiconductor chip. The quality is important because the higher the quality the better the performance of the devices. This is because a poor connection gets hotter faster due to increased electrical resistance and this can impact device performance. Hybrid bonding measures how well electrical is flowing a the bonding interface which means that if you know it is bad, you know you will have more voids. If you can find ways to ensure the electrical connections are good, the better off you will be. They used a 3-D Cross Kelvin Resistor to measures how electricity flows across the bonded layers. After a lot of testing, the found that small voids can cause failures over time. The results of their modeling showed that hybrid bonding is a good method for making a stronger bonding interface with better electrical connections and less voids.
Research Question/Problem/ Need	Weather rimproving the quality of the bonding interphase could reduce chip failure.

Important Figures

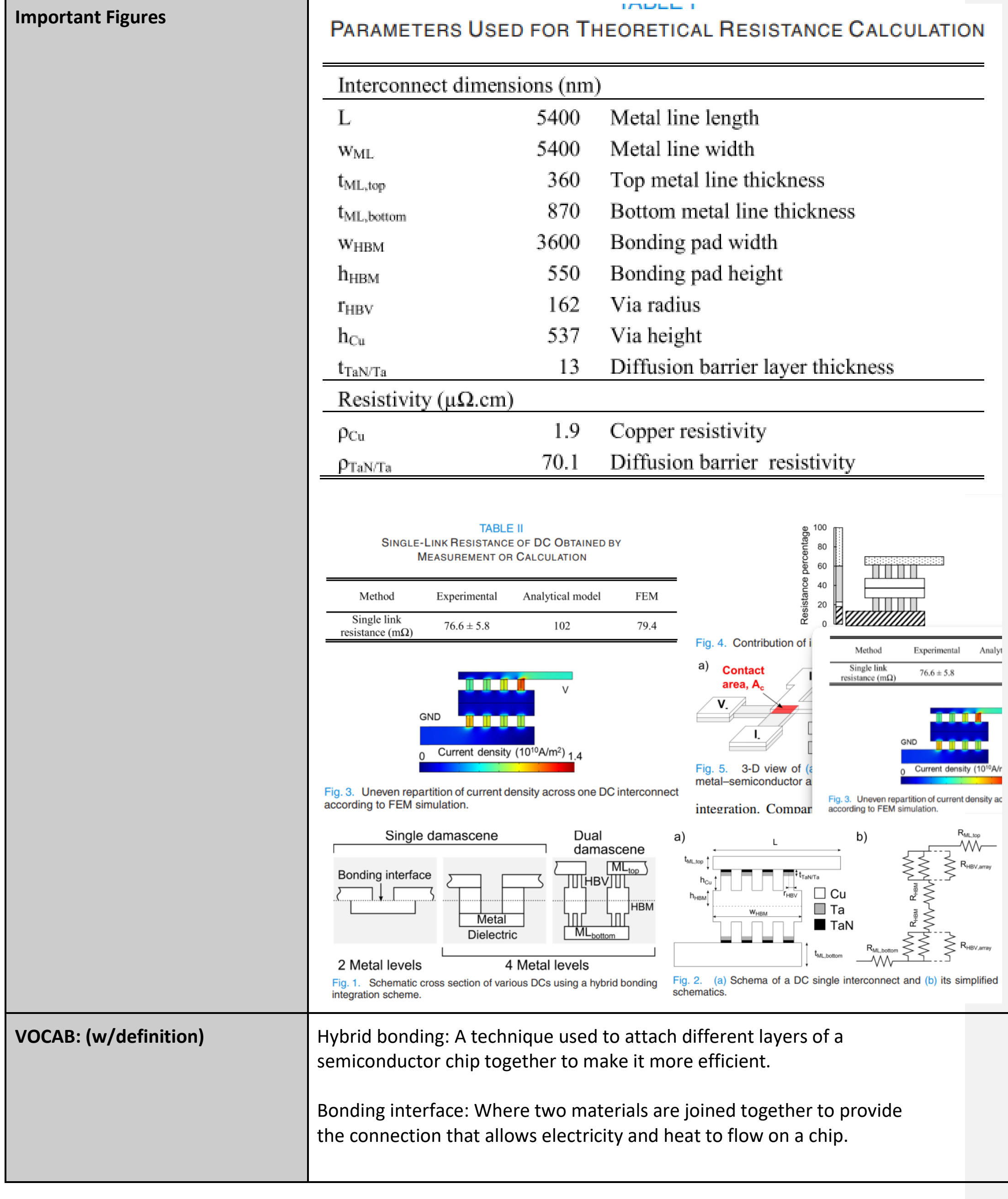


TABLE I

PARAMETERS USED FOR THEORETICAL RESISTANCE CALCULATION

Interconnect dimensions (nm)		
L	5400	Metal line length
w_{ML}	5400	Metal line width
$t_{ML,top}$	360	Top metal line thickness
$t_{ML,bottom}$	870	Bottom metal line thickness
w_{HBM}	3600	Bonding pad width
h_{HBM}	550	Bonding pad height
r_{HBV}	162	Via radius
h_{Cu}	537	Via height
$t_{TaN/Ta}$	13	Diffusion barrier layer thickness
Resistivity (μΩ.cm)		
ρ_{Cu}	1.9	Copper resistivity
$\rho_{TaN/Ta}$	70.1	Diffusion barrier resistivity

TABLE II

SINGLE-LINK RESISTANCE OF DC OBTAINED BY MEASUREMENT OR CALCULATION

Method	Experimental	Analytical model	FEM
Single link resistance (mΩ)	76.6 ± 5.8	102	79.4

Fig. 3. Uneven repartition of current density across one DC interconnect according to FEM simulation.

Fig. 4. Contribution of i

Fig. 5. 3-D view of (a metal–semiconductor a

integration. Compar

Fig. 1. Schematic cross section of various DCs using a hybrid bonding integration scheme.

Fig. 2. (a) Schema of a DC single interconnect and (b) its simplified schematics.

VOCAB: (w/definition)

Hybrid bonding: A technique used to attach different layers of a semiconductor chip together to make it more efficient.

Bonding interface: Where two materials are joined together to provide the connection that allows electricity and heat to flow on a chip.

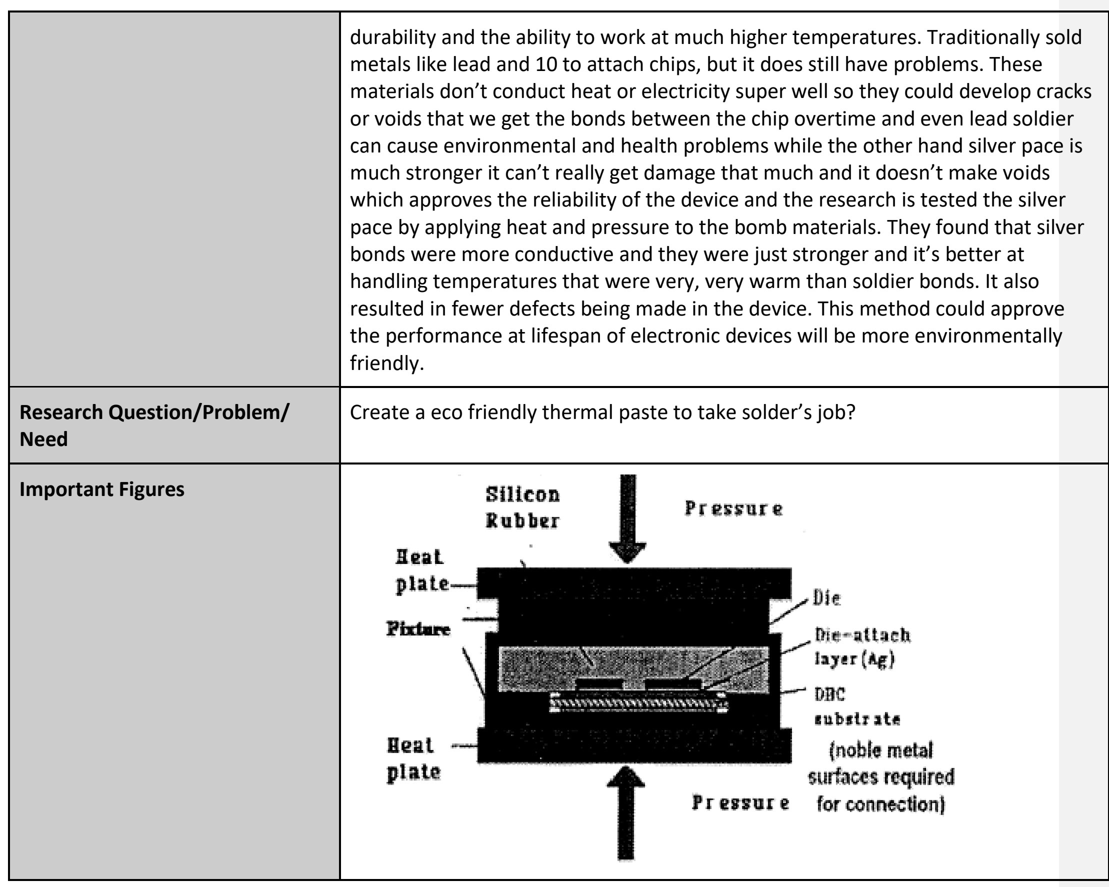
	Electrical resistance: How much the bonding interface impacts the flow of electricity.
Cited references to follow up on	
Follow up Questions	Will making a higher quality bonding interface increase costs to semiconductor manufacturers? Is the 3-D Cross Kelvin Resistor machine used something all manufacturers have already? Is poor quality bonding interfaces common enough to make this process worthwhile?

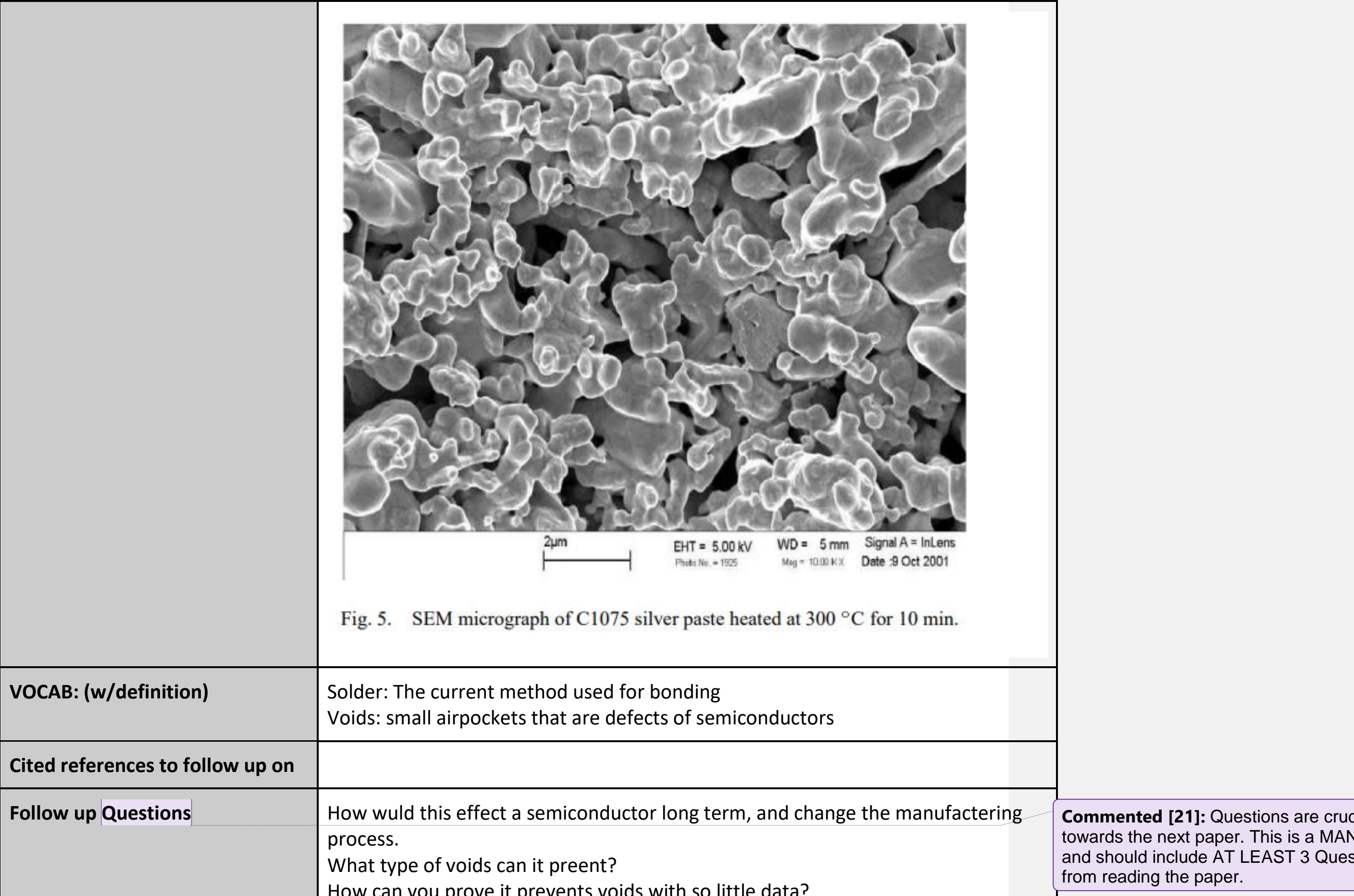
Commented [20]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.

Article #20 Notes: Title

Article notes should be on separate sheets

Source Title	Pressure-assisted low-temperature sintering of silver paste as an alternative die-attach solution to solder reflow
Source citation (APA Format)	Zhang, Z., & Lu, G.-Q. (2002). Pressure-assisted low-temperature sintering of silver paste as an alternative die-attach solution to solder reflow. *IEEE Transactions on Electronics Packaging Manufacturing*, *25*(4), 279–283. IEEE Transactions on Electronics Packaging Manufacturing. https://doi.org/10.1109/TEPM.2002.807719
Original URL	https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1176910
Source type	JOURNAL ARTICLE
Keywords	
#Tags	
Summary of key points + notes (include methodology)	This articial basically talks about a way to attach chips an electronic devices, using like a silver paste instead of traditional sold are and this process is called pressure, assisted low temperature, centering, and involves pressing and heating silver paste to create a strong bond between the chip and the base of the chip. This method has a lot of benefits to it compared to the old method of soldering as it’s better with heat and it allows for electricity to flow better there is higher

	durability and the ability to work at much higher temperatures. Traditionally sold metals like lead and 10 to attach chips, but it does still have problems. These materials don't conduct heat or electricity super well so they could develop cracks or voids that we get the bonds between the chip overtime and even lead soldier can cause environmental and health problems while the other hand silver pace is much stronger it can't really get damage that much and it doesn't make voids which approves the reliability of the device and the research is tested the silver pace by applying heat and pressure to the bomb materials. They found that silver bonds were more conductive and they were just stronger and it's better at handling temperatures that were very, very warm than soldier bonds. It also resulted in fewer defects being made in the device. This method could approve the performance at lifespan of electronic devices will be more environmentally friendly.
Research Question/Problem/ Need	Create a eco friendly thermal paste to take solder's job?
Important Figures	

	 Fig. 5. SEM micrograph of C1075 silver paste heated at 300 °C for 10 min.
VOCAB: (w/definition)	Solder: The current method used for bonding Voids: small airpockets that are defects of semiconductors
Cited references to follow up on	
Follow up Questions	How wuld this effect a semiconductor long term, and change the manufactering process. What type of voids can it preent? How can you prove it prevents voids with so little data?

Commented [21]: Questions are crucial in leading you towards the next paper. This is a MANDATORY section and should include AT LEAST 3 Questions that stem from reading the paper.