Dual Eulerian Graphs

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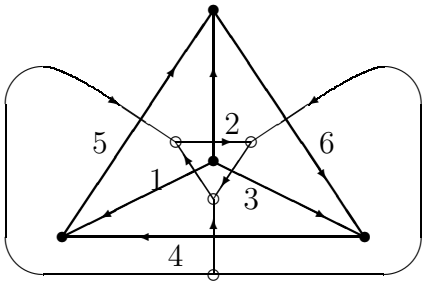
Abstract

A dual-eulerian graph is a plane graph which has an ordering defined on its edge set which forms simultaneously an Euler circuit in the graph and an euler circuit in the dual graph. Dual-eulerian graphs were defined and studied in the context of silicon optimization of cmos layouts. In this paper we examine the connections between the dual eulerian property, Petrie walks, and the connectivity of the graph. We will also consider the dual-eulerian property for graphs embedding in surfaces of higher genus.

1 Introduction

A *plane graph* is a planar graph G together with a particular embedding of G into the plane, which we will usually regard as an embedding into the sphere to avoid distinguishing the exterior face. An embedding of a graph in any surface is *regular* if the interiors of the faces are homeomorphic to open disks (i.e., have no handles). A convenient way to represent a regularly embedded graph in an orientable surface is via a *rotation system.* Arbitrarily orient each edge and to each vertex v we can associate the cycle of signed edges obtained by reading off counterclockwise the edges incident to v and taking the edge to be positive if it is oriented toward v and negative otherwise. The vertex permutation $\mathcal{V}$ is the product of the disjoint cycles corresponding to the vertex set V, and is a permutation of the set $E \cup (-E)$. The edge permutation $\mathcal{E}$ transposes each edge and its negative. The cycles of the face permutation $\mathcal{F}$ are found by reading around the boundary of each each face counterclockwise



$\mathcal{V} = (\bar{3}\bar{2}\bar{1})(1\bar{5}4)(2\bar{6}5)(3\bar{4}6)$

$\mathcal{E} = (1\bar{1})(2\bar{2})(3\bar{3})(4\bar{4})(5\bar{5})(6\bar{6})$

$\mathcal{F} = (1\bar{4}\bar{3})(2\bar{5}\bar{1})(3\bar{6}\bar{2})(456).$

Figure 1: A rotation system for a tetrahedron.

with the opposingly oriented edges assigned a negative. See Figure 1. We will notate the negative of the edge e by $\bar{e}$. Our permutations will act on the right. The rotation system determines the graph, surface and embedding up to homeomorphism. One need only specify the vertex or face permutation since one has the relation $\mathcal{FEV} = 1$. If the edges of the dual graph are oriented by turning the edges of G counterclockwise and using the same symbols, then the rotation system of the dual is $(\mathcal{F}^*, \mathcal{E}^*, \mathcal{V}^*)$ with vertex permutation $\mathcal{F}^* = \mathcal{F}$, edge permutation $\mathcal{E}^* = \mathcal{E}$ and face permutation $\mathcal{V}^* = \mathcal{EVE}$. For the example of Figure 1, with the dual graph distinguished by hollow vertices, we have vertices $\mathcal{F}^* = (1\bar{4}\bar{3})(2\bar{5}\bar{1})(3\bar{6}\bar{2})(456)$, edges $\mathcal{E}^* = (1\bar{1})(2\bar{2})(3\bar{3})(4\bar{4})(5\bar{5})(6\bar{6})$, and faces $\mathcal{V}^* = (321)(\bar{1}5\bar{4})(\bar{2}6\bar{5})(\bar{3}4\bar{6})$. (Note that for the double dual we have $\mathcal{V}^{**} = \mathcal{EVE}$ and $\mathcal{F}^{**} = \mathcal{EFE}$ since the second turn reverses the orientation of the edges.) For details on rotation systems see [5]

A circuit or walk in a graph is called *eulerian* if it contains all the edges of G and a graph is called *eulerian* if it has an euler circuit. A graph is eulerian if and only if all its vertices have even valence. If a bipartite graph is embedded in a surface, then G^* is eulerian. If G is embedded in the plane, then the converse is also true.

A graph embedded in a surface is said to be *dual-eulerian* if it has an eulerian circuit (walk) $e_1, \ldots, e_k$ such that $e_1^*, \ldots, e_k^*$ form an euler circuit (walk) in G^*. Dual eulerian graphs were introduced in [9] as an aid in the efficient design of Complimentary Metal-Oxide Semi-conductor (CMOS) Very Large Scale Integrated (VLSI) circuits, and subsequent work has had this application in mind. In integrated circuit design, a logic fuction can be implemented by means of a functional cmos cell consisting of a row of p-mos transistors and a row of n-mos transistors, corresponding to the p-mos and n-mos sides of the circuit. The p-mos and n-mos sides are dual to one an-

other. In the graph model corresponding to such a circuit, every gate/drain potential is represented by a vertex and every transistor is represented by an edge connecting source and drain vertices. In order to omptimize circuit performance and layout efficiency, transistors are alligned vertically with a separation area required between physically adjacent transistors which are not connected. An optimal layout is obtained by minimizing the number of separations, which means that we are looking for an Eulerian path in the graph model of the p-mos side vertices which is at the same time an Eulerian path on the n-mos side. This leads to the definition of the dual-Eulerian property. For details on the layout of cmos function arrays, see [9].

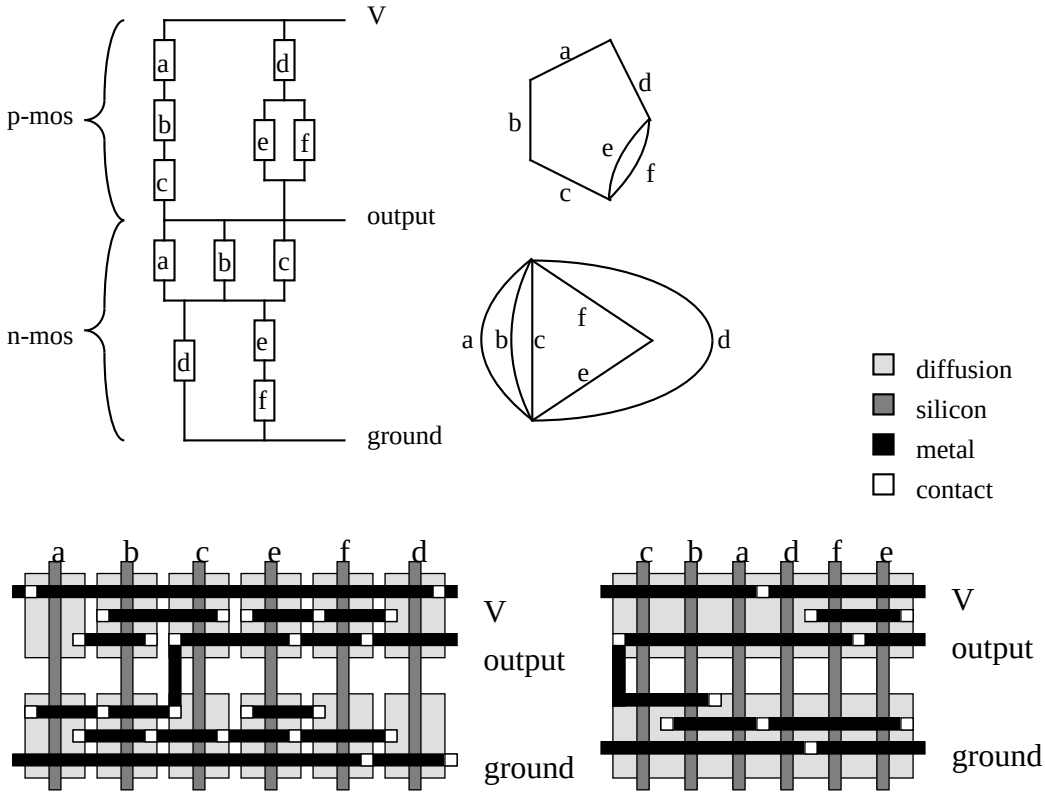


Figure 2: A cmos circuit, its graph, layout, and optimal layout

Many papers have studied the case of series-parallel graphs, [4, 6, 7, 9], and in [2] is found a polynomial algorithm for deciding whether a 2-connected plane graph is dual-eulerian or not. The problem of determining the minimum number of disjoint Euler paths is NP-hard [10]. Also non-dual circuit topologies have been studied [11].

2 Petrie Paths and dual eulerian graphs.

Given a graph embedded in a surface, if two consecutive edges of a walk are consecutive edges along the boundary of a face, then we say that they form a *turn*. That face lies on the same side of both edges and we call the turn a *right turn* or a *left turn* depending on which side the face lies as we move along the edges of the walk. If the two edges meet at a vertex of valence two, then they will be simultaneously both a left and a right turn. If a pair of edges forms a left turn with respect to a walk w, then they form right turn with respect to the reverse walk, and vise versa. A *Petrie walk* is a walk such that every two consecutive edges are a turn, and the turns alternate left and right. A *Petrie circuit* is a closed Petrie walk. We will often indicate the turns in a petrie walk by a small arc at the turns, see Figure 3. In terms of a

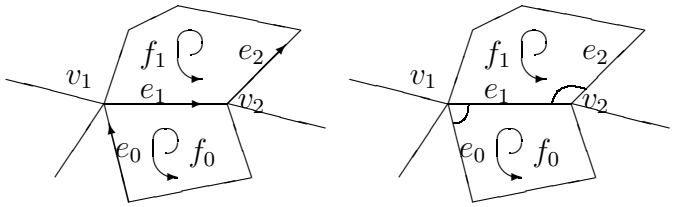


Figure 3:

rotation system, a walk is a list of signed edges, $e_1, e_2, \ldots, e_k$ with the edge labelled positive if it points in the direction of w and negative otherwise. If w is a petrie walk, then at the left turns, such as at face f_1 in Figure 3, we have $e_{i+1} = e_i\mathcal{F}$, while at the right turns, such as at face f_0, we have $\bar{e}_i = \bar{e}_{i+1}\mathcal{F}$, or $e_{i+1} = e_i\mathcal{E}\mathcal{F}^{-1}\mathcal{E}$. Thus the signed edges of a petrie walk are characterized by

$$e_0 \xrightarrow{\mathcal{F}} e_1 \xrightarrow{\mathcal{E}\mathcal{F}^{-1}\mathcal{E}} e_2 \xrightarrow{\mathcal{F}} e_3 \xrightarrow{\mathcal{E}\mathcal{F}^{-1}\mathcal{E}} e_4 \cdots$$

THEOREM 1 *Suppose a graph G embedded in an orientable surface has an Euler Petrie walk (circuit) $w = (e_1, \ldots, e_n)$, then w is a dual-eulerian walk (circuit) for G.*

PROOF: Choose a rotation system for the embedding. If we have a petrie walk

$$e_0 \xrightarrow{\mathcal{F}} e_1 \xrightarrow{\mathcal{E}\mathcal{F}^{-1}\mathcal{E}} e_2 \xrightarrow{\mathcal{F}} e_3 \xrightarrow{\mathcal{E}\mathcal{F}^{-1}\mathcal{E}} e_4 \cdots$$

Then $e_{2k} \xrightarrow{\mathcal{F}} e_{2k+1}$ implies $e_{2k+1} = e_{2k}\mathcal{V}^{-1}\mathcal{E}$, or $\bar{e}_{2k+1} = e_{2k}\mathcal{V}^{-1}$, so $\bar{e}_{2k+1} = e_{2k}(\mathcal{E}(\mathcal{V}^*)^{-1}\mathcal{E})$. Similarly, $e_{2k-1} \xrightarrow{\mathcal{E}\mathcal{F}^{-1}\mathcal{E}} e_{2k}$ implies $e_{2k} = e_{2k+1}\mathcal{E}\mathcal{F}^{-1}\mathcal{E}$, or $e_{2k} = e_{2k-1}\mathcal{V}\mathcal{E}$, so $e_{2k} = \bar{e}_{2k-1}\mathcal{E}\mathcal{V}\mathcal{E} = \bar{e}_{2k-1}\mathcal{V}^*$. Thus

$$e_0 \xrightarrow{\mathcal{E}(\mathcal{V}^*)^{-1}\mathcal{E}} \bar{e}_1 \xrightarrow{\mathcal{V}^*} e_2 \xrightarrow{\mathcal{E}(\mathcal{V}^*)^{-1}\mathcal{E}} \bar{e}_3 \xrightarrow{\mathcal{V}^*} e_4 \cdots$$

and $(e_0, \bar{e}_1, e_2, \bar{e}_3, \ldots)$ is an euler petrie walk in G^*. □

The converse of Theorem 1 is not true. Tracing out the figure eight graph in Figure 4 in the usual way is a dual-eulerian circuit which is not a petrie

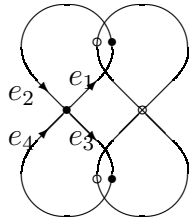


Figure 4: A non-petrie dual-eulerian circuit.

circuit. It does, however, have a petrie circuit, which by Theorem 1 is another dual eulerian circuit. The remainder of this section and much of Section 4 will be devoted to proving this partial converse to Theorem 1

THEOREM 2 *If a plane graph G has a dual-eulerian circuit w, then G has a dual-eulerian circuit w' which is also a petrie circuit.*

Thus to decide whether a plane graph has a dual-eulerian circuit we need only check for petrie circuits, which we may do by starting at any edge and proceeding turning left-right-left-... in succession until we return to the start, the maximal Petrie path being determined by the initial choice of left or right. If we have spanned the edges we are done. If not, then we need only check

the maximal Petrie walk starting with the other turn. This should simplify the algorithm of [2].

The requirement in Theorem 2 that G be planar is necessary, as we see in Figure 5a, which is a dual eulerian graph on the torus with no eulerian

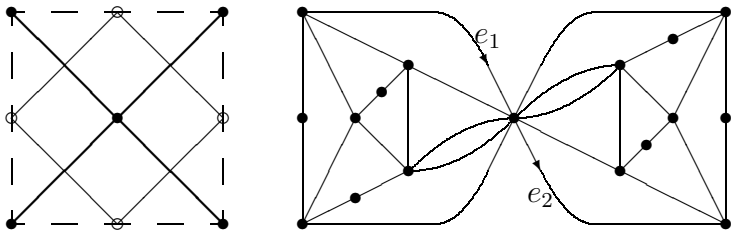


Figure 5:

petrie circuit. It is also necessary in Theorem 2 that we restrict to dual eulerian circuits, as we see in Figure 5b which shows a plane graph with a dual-eulerian walk in which e_2 follows e_1, but no eulerian petrie walk. If we restrict ourselves to 2-connected planar graphs, however, the only possible dual-eulerian walks are petrie walks, and the converse of Theorem 1 is true.

THEOREM 3 *If a 2-connected plane graph G has a dual-eulerian walk (circuit) w, then w is also an eulerian petrie walk (circuit).*

PROOF: Suppose there is an euler circuit, and use it and its dual to orient the edges of G and G^*. Suppose e is an edge of the euler circuit with initial vertex v_0 and terminal vertex v_1, and suppose for the moment that both have valence at least three, and that the edge dual to e is oriented from f_0 to f_1. The situation is as in Figure 6. By 2-connectivity, no vertex occurs

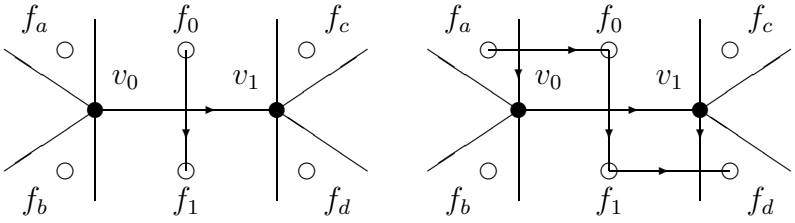


Figure 6:

twice along the boundary of any face, so every face is incident at a vertex

with exactly 2 edges, (since there are no loops.) Thus the edge previous to e in the dual-eulerian circuit must cross the edge bounding f_0 and f_a, and similarly the edge following e must cross the unique edge incident to v_1 bounding f_d and f_1, so the dual-eulerian path must turn left at v_0 and right at v_1.

Now we consider the case of vertices of valence 2, at which turning left and right have the same effect. If G is just a cycle, then as we traverse the cycle the dual circuit alternates back and forth between the inside and outside face, hence the circuit must have even length and me may make a left-right assignment on the cycle. If G is not a cycle, let $v_0, \ldots, v_n$ be consecutive vertices along the dual-eulerian walk so that $v_1, \ldots, v_{n-1}$ have valence 2, and v_0 and v_1 have valence at least 3, and that the edge dual to e is oriented from f_0 to f_1. By 2-connectivity, $v_0 \neq v_n$. If n is even, then the situation is as in Figure 7a. As before, the edge previous to v_0 bounds f_0 and f_a and the

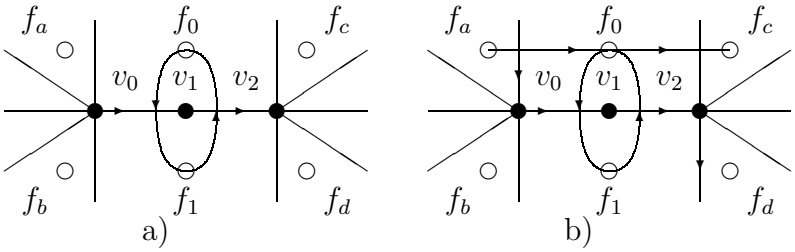


Figure 7:

dual-eulerian circuit makes a left turn at v_0. As we move from v_0 to v_n to dual path alternates from f_0 to f_1, ending at f_0, and so the path must make a another left turn at v_n. Since n is even, we can simply turn left at v_i when i is even and right when i is odd.

If n is odd, the situation is as in Figures 8a and b, so by a similar argument

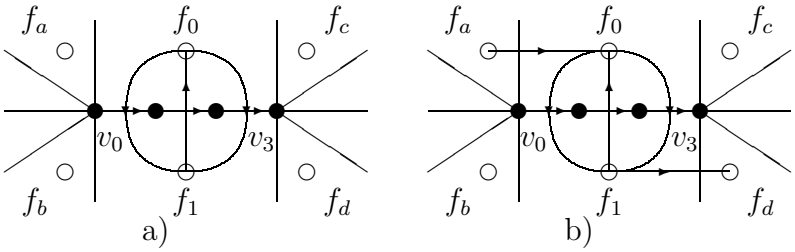
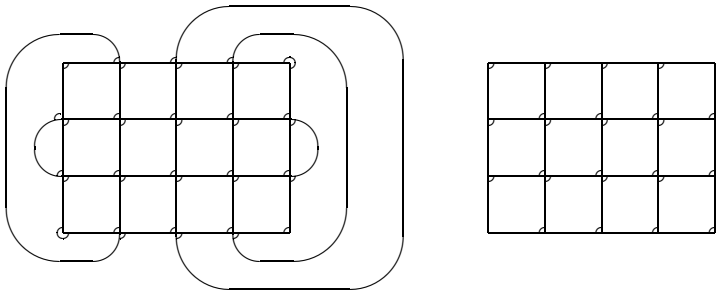


Figure 8:

must turn left at v_0 and right at v_n, and we again turn left at v_i when i is

even and right when i is odd. □

If a 2-connected graph has an Euler circuit, then of course, the reverse circuit it also a petrie circuit. It may also happen that, starting at the same edge, the petrie circuit generated by making the opposite first turn is also eulerian. This is the case in Figure 9a, since left and right are equivalent



a) b)

Figure 9:

by symmetry, with Figure 9b exhibiting the same phenomenon on the torus. We have the following.

COROLLARY 1 *A plane 2-connected graph has at most 4 dual-eulerian circuits.*

If G is connected but not 2-connected, then its blocks are 2-connected, and we can use Theorem 3 and the following.

THEOREM 4 *Let G be a plane graph G with Eulerian path (circuit) w. Then w is dual-eulerian if and only if the restriction w_B of w to any block B of G is an Euler petrie path (circuit) for B, with the walk turning, at each vertex of attachment, along the faces of attachment, and, for the case of a path, having at most two endpoints which are not at vertices of attachment with dual path ending at its face of attachment.*

PROOF: Sufficiency: If G is 2-connected we are done, so let v be a vertex of G and let f be a face whose boundary meets v more than once, so v is a cut vertex. The boundary p of f factors as into segments $p = p_1 \dots p_n$, with $p_i = e_{i,1}, e_{i,k_i}$ such that each starts and ends at v but does not meets v in its interior, see Figure 10, where f is drawn as the exterior face. As the dual-eulerian walk w passes through the cutvertex v of G, crossing between

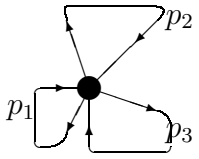


Figure 10:

the leaves of v with respect to f, the dual circuit must pass through the cutvertex f of G^*, and this can only happen along the edges $e_{i,1}$ and e_{i,k_i}, since they are the only edges along the boundary of f which are incident with v.

If the dual-eulerian path crosses v twice, once into and once out of L_i, then one segment of w is an dual eulerian walk of w_i of L_i, beginning and ending at $e_{i,1}$ and e_{i,k_i}, so adding a turn there completes it to a circuit.

If the dual-eulerian path crosses v just once once into L_i, then w is a path with, say, the initial endpoint in L_i, an initial segment forming a dual-eulerian walk for L_i ending at v whose dual walk ends at f.

The result now follows by induction on the size of the block cutpont tree of G.

Necessity: Again consider the leaves of a vertex v with respect to a face f. By induction, each has a dual eulerian walk (circuit) which turns or ends at f, which may be concatenated to form a dual-eulerian walk (circuit) for G. □

The proof of Theorem 2 is now clear, since at the end of the previous proof, in the case of a circuit, we may concatenate the paths or their reverses in any order to form a dual eulerian circuit for G. Thus we chose each passage through v to be a turn along f which is compatible with the euler-petrie circuits of the L_i which exist by induction. Moreover, since all these choices are independent, we may count the number of dual-eulerian circuits of a dual eulerian plane graph. By Corollary 1 we may assume that G is not 2-connected. Let G be a dual-eulerian plane graph which is not 2-connected. Let $\{c_1, \ldots c_p\}$ be the cutpoints of G, and for each c_i let f_i denote the numbed of faces of G which meet c_i more than once, and $\{l_1, \ldots l_{f_i}\}$ be the number of leaves of G at c_i with respect to those faces, so if $\delta(c_i)$ is the valence of c_i in the block cutpoint tree of G, $\delta(c_i) = \sum l_{f_i}$.

THEOREM 5 *The number $de(G)$ of dual-eulerian paths of G is*

$$de(G) = \prod_{i=1}^{p}(\prod_{j=1}^{f_i} 2^{l_i}(l_i - 1)!) \leq \prod_{i=1}^{p} 2^{\delta(c_i)}(\delta(c_i) - 1)!$$

with exactly two of them being euler petrie circuits, one the reverse of the other.

3 Connectedness of dual-eulerian graphs.

A consequence of Euler's theorem its that a plane graph with an euler walk or circuit must have low connectivity.

THEOREM 6 *No 3-connected plane graph has a dual eulerian walk or circuit.*

PROOF: Let v_i be the number of vertices of valence i, and f_i be the number of faces whose boundary contains i edges. So, if G is 3-connected then $v_2 = f_2 = 0$ and a simple calculation involving the euler characteristic gives

$$v_3 + f_3 = 8 + \sum_{i=5}^{\infty}(i - 4)(v_i + f_i),$$

so $v_3 + f_3 \geq 8$, so either G or G^* has 4 vertices of valence 3, and so has no eulerian path or circuit. □

The proof shows in fact that, like for the case of dual-eulerian circuits, the graph must have vertices of valence 2 or parallel edges. It is possible for a dual eulerian graph to 3-connected except for the presence of parallel edges and vertices of valence 2, in other words, a series parallel extension of a 3-connected graph, see for example Figure 9a.

THEOREM 7 *Every connected plane graph has a dual-eulerian series-parallel extension with at most $4|E|$ edges.*

PROOF: Let G be a plane graph, and choose a maximal tree T. Form G' by doubling the edges of T and then adding a vertex of valence 2 to the interior of each, and then subdivide each edges of G not in T with a vertex of valence 2 and double both halves, see Figure 11. Thus each edge of G has been series-parallel extended to 4 edges of G'. Considering T and T' alone, the

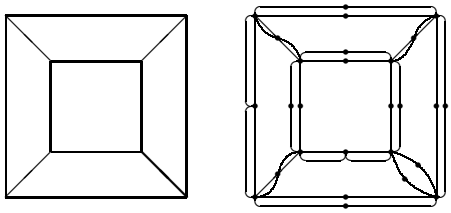


Figure 11: A dual-Eulerian series parallel extension of the cube.

boundary of the exterior face touches every edge of T twice, and so for T' the boundary of the exterior face is an euler petrie path since every second vertex is of valence 2. We may now form G' from T' by attaching doubled paths of length 2 one by one. Each time we are adding a new doubled chord of length 2 to a face at two vertices where the petrie path turns along that face, see Figure 12. This addition allows us to extend the petrie path by splicing in

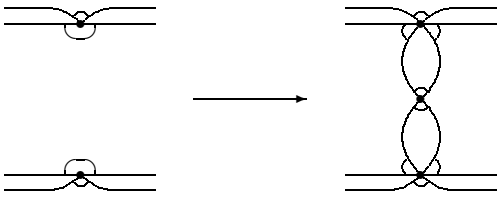


Figure 12:

a spur of length 2 to each section of the petrie path. Moreover, the petrie path turns at the two vertices of attachment along the newly created faces, so the process may continue. □

The bound of $4|E|$ edges is very rough. The examples we have looked at all required at most $|E|$. If a relatively few new edges would be required to make G dual-eulerian, then it may be possible to use the series parallel dual eulerian extension to achieve a fairly optimal cmos layout of G, so finding a better bound is an important open question.

4 Higher genus surfaces.

If we consider the dual eulerian property for graphs embedded in other surfaces then, as we have seen, the situation is more difficult since, even for 2-connected graphs, we cannot check for the dual-eulerian property by simply looking for eulerian petrie paths. One solution is to restrict ourselves to

strongly regular embeddings, that is, embeddings such that every closed face is homeomorphic to a closed disk. In the plane this is equivalent to requiring 2-connectivity of the graph. For a strongly regular embedding, each vertex occurs only once as we read around the boundary of a face, so the proof of Theorem 3 works and we have the following.

THEOREM 8 *If a graph G, strongly regularly embedded in an orientable surface, has a dual eulerian walk or circuit w, then w is also an euler petrie walk or circuit.*

It is well known that every finite graph embeds in a surface of high enough genus.

THEOREM 9 *Given a graph G having euler walk (circuit) w, G has an embedding on an orientable surface such that c is a dual-eulerian walk (circuit).*

PROOF: If G has euler circuit c, then c defines an orientation on the edges of G by taking the cyclic order of edges around a vertex to to be the order induced from the circuit. Label and orient the edges of G so that the euler circuit is $(e_1, e_2, \ldots, e_{2n})$. We need only find a rotation system for G such that w satisfies equations $e_{2i+1} = e_{2i}\mathcal{F}$ and $e_{2i} = e_{2i-1}\mathcal{E}\mathcal{F}^{-1}\mathcal{E}$, or equivalently, $\bar{e}_{2i+1}V = e_{2i}$ and $\bar{e}_{2i} = e_{2i-1}V$. Because of our choice of labels, for every vertex v the signed edges incident with v come in pairs of the form $\{e_i, \bar{e}_{i+1}\}$. We may thus chose a cyclic permutation of those signed edges in which e_i is the predecessor of $\bar{e}_{i+1}$ if i is odd, the successor if i is even, and the equations above are satisfied. □

Figure 13 shows an Euler circuit on the octahedron graph, and the dual-eulerian embedding of that graph into the two-holed torus that results.

In fact, for each vertex v, we may cyclicly order the adjacent pairs any way we wish, so, if $\alpha(G)$ is the number of euler circuits of G, we have the following.

THEOREM 10 *Up to homeomorphism, there are*

$$\frac{1}{2}\alpha(G)\prod_{v\in V}\frac{(\delta(v)-1)!}{2}$$

embeddings of G which are dual eulerian.

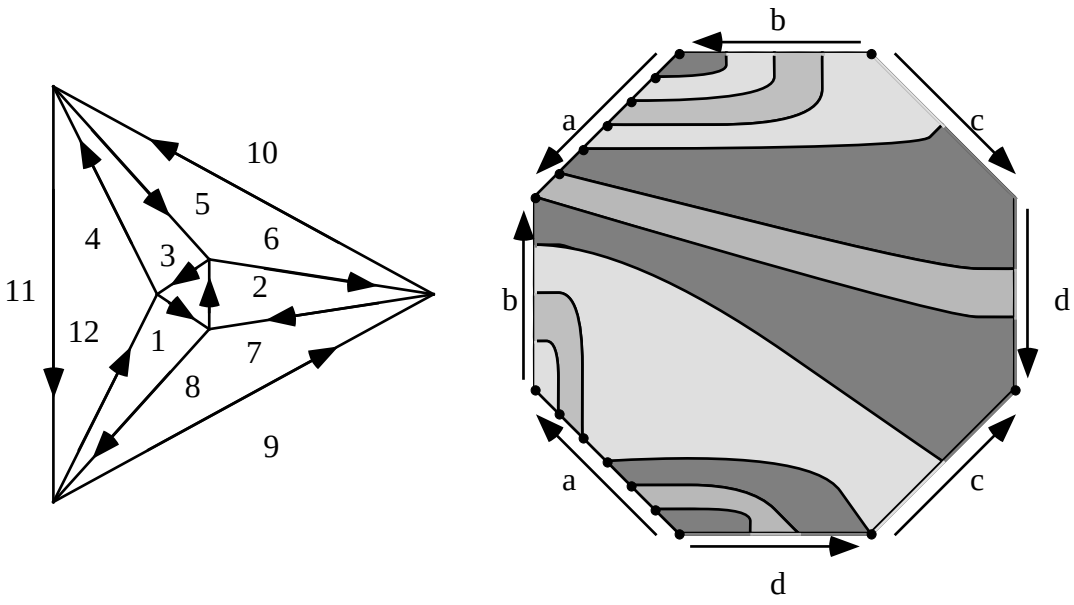


Figure 13:

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