Project Assignment # 2

Solution

1. Assuming we have n loops:

   (a)

   $$CPI_5 = \lim_{n\to\infty} \frac{n + 4 + \frac{1}{5} \cdot n}{n} = 1.2$$

   Alternatively:

   $$CPI_5 = \text{Ideal CPI} + \text{stall clock cycles per instruction} = 1 + \frac{1}{5} = 1.2$$

   $$CPI_{14} = \lim_{n\to\infty} \frac{n + 13 + \frac{3}{8} \cdot n}{n} = 1.375$$

   $$speedup = \frac{Clock_5 \cdot CPI_5}{Clock_{14} \cdot CPI_{14}} = \frac{1.2 \times 1}{1.375 \times 0.5} \approx 1.75$$

   (b)

   $$CPI_5 = \lim_{n\to\infty} \frac{n + 4 + \frac{1}{5} \cdot n + 2 \cdot 15\% \cdot 20\% \cdot n}{n} = 1.26$$

   $$CPI_{14} = \lim_{n\to\infty} \frac{n + 13 + \frac{3}{8} \cdot n + 5 \cdot 15\% \cdot 20\% \cdot n}{n} = 1.525$$

2. (a) Speedup $= \dfrac{CPI_{nonpipeline}}{CPI_{pipeline}} = \dfrac{5}{\frac{10 \text{ cycles}}{4 \text{ instr.}}} = 2$

	Clock cycle number										
Instruction	1	2	3	4	5	6	7	8	9	10	11
LD R1, 24(R5)	IF	ID	EX	MEM	WB						
DADD R2, R4, R1		IF	ID	stall	EX	MEM	WB				
BEQ R2, R6, Dest			IF	stall	stall	ID	EX	MEM	WB		
DADD R3, R2, R4						IF	ID	EX	MEM	WB	

(b) Speedup $= \dfrac{CPI_{nonpipeline}}{CPI_{pipeline}} = \dfrac{5}{\frac{14 \text{ cycles}}{6 \text{ instr.}}} = 2.14$

	Clock cycle number													
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14
LD R1, 24(R5)	IF	ID	EX	MEM	WB									
DADD R2, R4, R1		IF	ID	stall	EX	MEM	WB							
BEQ R2, R6, Dest			IF	stall	stall	ID	EX	MEM	WB					
DADD R3, R2, R4						IF	idle	idle	idle	idle				
DADDUI R1, R1, #1							IF	ID	EX	MEM	WB			
LD R4, 4(R5)								IF	ID	EX	MEM	WB		
DADD R3, R2, R4									IF	ID	stall	EX	MEM	WB

3. (a) Loop length: 18, next iteration starts at cycle 17

	Clock cycle number																	
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Loop LD R3, 0(R5)	IF	ID	EX	MEM	MEM	MEM	WB											
LD R1, 0(R3)		IF	ID	stall	stall	stall	EX	MEM	MEM	MEM	WB							
DADDI R1, R1, #1			IF	stall	stall	stall	ID	stall	stall	stall	EX	MEM	WB					
DSUB R4, R3, R2							IF	stall	stall	stall	ID	EX	MEM	WB				
SD R1, 0(R3)											IF	ID	EX	MEM	MEM	MEM	WB	
BNZ R4, Loop												IF	ID	EX	EX	stall	MEM	WB
LD R3, 0(R5) ; loop																	IF	

(b) Loop length: 18, next iteration starts at cycle 14

	Clock cycle number																	
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Loop LD R3, 0(R5)	IF	ID	EX	MEM	MEM	MEM	WB											
LD R1, 0(R3)		IF	ID	stall	stall	stall	EX	MEM	MEM	MEM	WB							
DADDI R1, R1, #1			IF	stall	stall	stall	ID	stall	stall	stall	EX	MEM	WB					
DSUB R4, R3, R2							IF	stall	stall	stall	ID	EX	MEM	WB				
SD R1, 0(R3)											IF	ID	EX	MEM	MEM	MEM	WB	
BNZ R4, Loop												IF	ID	EX	EX	stall	MEM	WB
LD R3, 0(R5) ; loop														IF				

(c) Loop length: 18, next iteration starts at cycle 13

	Clock cycle number																	
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Loop LD R3, 0(R5)	IF	ID	EX	MEM	MEM	MEM	WB											
LD R1, 0(R3)		IF	ID	stall	stall	stall	EX	MEM	MEM	MEM	WB							
DADDI R1, R1, #1			IF	stall	stall	stall	ID	stall	stall	stall	EX	MEM	WB					
DSUB R4, R3, R2							IF	stall	stall	stall	ID	EX	MEM	WB				
SD R1, 0(R3)											IF	ID	EX	MEM	MEM	MEM	WB	
BNZ R4, Loop												IF	ID	EX	EX	stall	MEM	WB
LD R3, 0(R5) ; loop													IF					

4. (a) 18 cycles

	Clock cycle number																	
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
L.D F2, 0(R1)	IF	ID	EX	MEM	WB													
L.D F4, -8(R1)		IF	ID	EX	MEM	WB												
MUL.D F6, F2, F4			IF	ID	stall	EX	EX	EX	EX	EX	EX	EX	MEM	WB				
S.D F6, 0(R2)				IF	stall	ID	stall	stall	stall	stall	stall	stall	EX	MEM	WB			
DADDUI R1, R1, #-16						IF	stall	stall	stall	stall	stall	stall	ID	EX	MEM	WB		
DADDUI R2, R2, #-8													IF	ID	EX	MEM	WB	
BNE R1, R3, Loop														IF	ID	EX	MEM	WB

(b) 16 cycles

	Clock cycle number															
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
L.D F2, 0(R1)	IF	ID	EX	MEM	WB											
L.D F4, -8(R1)		IF	ID	EX	MEM	WB										
DADDUI R1, R1, #-16			IF	ID	EX	MEM	WB									
MUL.D F6, F2, F4				IF	ID	EX	EX	EX	EX	EX	EX	EX	MEM	WB		
DADDUI R2, R2, #-8					IF	ID	EX	MEM	WB							
S.D F6, 8(R2)						IF	ID	EX	stall	stall	stall	stall	stall	MEM	WB	
BNE R1, R3, Loop							IF	ID	stall	stall	stall	stall	stall	EX	MEM	WB

(c) 5 loops. 20+3=23 cycles. 12 new registers.

Instruction	CC
L.D F2, 0(R1)	1
L.D F4, -8(R1)	2
L.D F8, -16(R1)	3
L.D F10, -24(R1)	4
L.D F14, -32(R1)	5
L.D F16, -40(R1)	6
L.D F20, -48(R1)	7
L.D F22, -56(R1)	8
L.D F26, -64(R1)	9
L.D F28, -72(R1)	10
MUL.D F6, F2, F4	11

MUL.D F12, F8, F10	12
MUL.D F18, F14, F16	13
MUL.D F24, F20, F22	14
MUL.D F30, F26, F28	15
DADDUI R1, R1, #-80	16
DADDUI R2, R2, #-40	17
S.D F6, 40(R2)	18
S.D F12, 32(R2)	19
S.D F18, 24(R2)	20
S.D F24, 16(R2)	21
S.D F30, 8(R2)	22
BNE R1, R3, Loop	23

(d) Assuming we have n loops, total number of clocks is: $(4 \cdot n + 3)$. Thus, number of clocks per loop is

$$\lim_{n \to \infty} \frac{(4 \cdot n + 3)}{n} = 4$$

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