Midterm Exam Solution

Solution

1. Basics

   (a) $2 \times 2^5 = 64$ bits, 5 bits can address 32 entries in the buffer, each entry has 2 bits.

   (b) Single issue and one CDB result per clock cycle, throughput is 1.

   (c) $N = 1, 2$ *or* 4. When $N = 4$, it is 4-way set associative, which is fully associative

   (d) $2^{16-6\times2} = 16$, 12 bits are for addresses, so that 4 bits are for opcode.

   (e) $\frac{\texttt{\#L2 hits}\cdot(\texttt{L2 hit}-\texttt{L1 hit})+\texttt{\#L2 hits}\cdot\texttt{L2 miss penalty}}{\texttt{\#L1 misses}} = \frac{(60-30)\times(8-2)+30\times50}{60} = 28$

2. Multiple pipeline with hazards and forwarding
   Forwarding is shown in bold.

   (a) Execution clock cycles of the loop: 14 cycles

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
LD F2,0(R1)	F	D	E	***M***	W														
DIV F8, F2, F0		F	D	S	***E***	E	E	E	E	***E***	M	W							
MULT F2, F6, F2			F	S	D	E	E	E	M	W									
LD F4, 0(R2)				S	F	D	E	***M***	W										
ADD F4, F0, F4						F	D	S	***E***	M	W								
ADD F10, F8, F2							F	S	D	S	***E***	M	W						
ADDI R1, R1, 8								S	F	S	D	E	M	W					
ADDI R2, R2, 8										S	F	D	***E***	M	W				
SD F4, 0(R2)												F	D	***E***	M	W			
SUB R20, R4, R1													F	D	***E***	M	W		
BNZ R20, Loop														F	S	***D***	E	M	W

   (b) Execution clock cycles of the loop: 14 cycles
   Speedup of b over a is: $speedup = \frac{T_a}{T_b} = \frac{14\times1}{14\times(1-10\%)} \approx 1.11$

Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
LD F2,0(R1)	F	D	E	***M***	W														
DIV F8, F2, F0		F	D	S	***E***	E	M	W											
MULT F2, F6, F2			F	S	D	S	E	E	M	W									
LD F4, 0(R2)				S	F	S	D	E	***M***	W									
ADD F4, F0, F4						S	F	D	S	***E***	M	W							
ADD F10, F8, F2								F	S	D	E	M	W						
ADDI R1, R1, 8									S	F	D	E	M	W					
ADDI R2, R2, 8											F	D	***E***	M	W				
SD F4, 0(R2)												F	D	***E***	M	W			
SUB R20, R4, R1													F	D	***E***	M	W		
BNZ R20, Loop														F	S	***D***	E	M	W

3. Single Issue vs. Multiple Issue Processor

   (a) 23 cycles

   (b) 15 cycles

   (c) 13 cycles

	Problem A	Problem B	Problem C	
Cycle	Pipeline	Pipeline	Pipeline A	Pipeline B
1	LD F6, 0(R2)	LD F6, 0(R2)	LD F6, 0(R2)	LD F2, 8(R2)
2	stall	LD F2, 8(R2)	stall	stall
3	stall	stall	stall	stall
4	stall	stall	stall	stall
5	LD F2, 8(R2)	stall	MULTD F8, F2, F6	LD F4, 8(R2)
6	stall	MULTD F8, F2, F6	ADD F10, F0, F6	stall
7	stall	LD F4, 8(R2)	stall	stall
8	stall	ADD F10, F0, F6	stall	stall
9	MULTD F8, F2, F6	stall	stall	stall
10	stall	stall	stall	stall
11	stall	stall	ADD F6, F8, F4	ADDI R2, R2, -16
12	stall	ADD F6, F8, F4	BNE R2, R3, Loop	stall
13	stall	ADDI R2, R2, -16	stall (the end)	stall
14	stall	BNE R2, R3, Loop		
15	LD F4, 8(R2)	stall (the end)		
16	stall			
17	stall			
18	stall			
19	ADD F10, F0, F6			
20	ADD F6, F8, F4			
21	ADDI R2, R2, -16			
22	BNE R2, R3, Loop			
23	stall (the end)			

4. Scoreboard Algorithm

Instruction	Issue	Read Ops	Execute Complete	Write Result	Assigned FU	Reason to Stall
LD F0, 0(R0)	1	2	3	4	Integer 1	
MUL.D F1, F0, F1	2	5	10	11	FP Mul 1	RAW(F0)
ADD.D F0, F0, F2	3	5	8	9	FP Add 1	RAW(F0)
SD F1, 0(R1)	4	12	13	14	Integer 1	RAW(F1)
LD F2, 4(R0)	5	6	7	8	Integer 2	
MUL.D F3, F2, F1	6	12	17	18	FP Mul 2	RAW(F1)
ADD.D F4, F1, F2	7	12	15	16	FP Add 2	RAW(F1)
SD F3, 4(R3)	8	19	20	21	Integer 2	RAW(F3)
ADDI R3, R3, 1	9	10	11	12	Integer 3	
ADD.D F0, F4, F1	10	17	20	22	FP Add 1	RAW(F4), CDB

Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer 1	Y	SD	R1	F1		FP Mul 1		N	
Integer 2	Y	LD	F2	R0				N	
Integer 3	N								
FP Add 1	Y	ADD.D	F0	F0	F2			N	N
FP Add 2	Y	ADD.D	F4	F1	F2	FP Mul 1	Integer 2	N	N
FP Mul 1	Y	MUL.D	F1	F0	F1			N	N
FP Mul 2	Y	MUL.D	F3	F2	F1	Integer 2	FP Mul 1	N	N

Name	FU	Name	FU
F0	FP Add 1	R0	
F1	FP Mul 1	R1	
F2	Integer 2	R2	
F3	FP Mul 2	R3	
F4	FP Add 2	R4	