Assignment # 1

1. When making changes to optimize part of a processor, it is often the case that speeding up one type of instruction comes at the cost of slowing down something else. For example, a faster floating point unit might be larger, forcing another component to be moved further away from the middle, which adds an extra cycle in delay to to reach that unit.

   (a) If the new fast floating point unit speeds up floating point operations by a factor of 2 on average, and floating point operations make 20% of the original program's execution time, what is the overall speedup?

   (b) Now assume that speeding up the floating-point unit slowed down data cache accesses, resulting in a 1.25x slowdown (or 4/5 speedup). Data cache accesses consume 10% of the original execution time. What is the speedup now?

   (c) Taking both these changes into account, what percentage of execution time is spent on floating point operations, what percentage is spent on data cache accesses?

2. Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 100 MHz and M2 has a clock rate of 150 MHz. The average number of cycles for each instruction class and their frequencies (for a typical program) are as follows:

Instruction Class	Machine M1 (cycles)	Machine M2 (cycles)	Frequency
A	1	2	55
B	2	3	25
C	4	4	20

   (a) Calculate the average CPI for each machine, M1, and M2.

   (b) Calculate the average MIPS ratings for each machine, M1 and M2.

   (c) Which machine has a smaller MIPS rating? Which individual instruction class CPI do you need to change, and by how much, to have this machine have the same or better performance as the machine with the higher MIPS rating (you can only change the CPI for one of the instruction classes on the slower machine)?

3. Compute the effective CPI for MIPS using Figure A.27 from the book. Assume the following measurements of average CPI have been made for the following instruction types:

Instruction	Average CPI
All ALU instructions	1.0
Loads-stores	1.6
Conditional branches	
Taken	2.3
Not taken	1.6
Jumps, calls, returns	1.1

Assume that 60% of the conditional branches are taken and that all instructions in the *other* category of figure A.27 are ALU instructions. Average the instruction frequencies of gap and gzip to obtain the instruction mix.

4. For the following we consider instruction encoding for instruction set architectures. *Explain your answers.*

   (a) Consider the case of a processor with an instruction length of 12 bits and with 32 general purpose registers so the size of the address fields is 5 bits. Is it possible to have instruction encodings for the following?

   - 3 two-address instructions
   - 30 one-address instructions
   - 52 zero-address instructions

   (b) Assuming the same instruction length and address field sizes, how many zero-address instructions are possible if 2 two-address instructions and 61 one-address instructions must be encoded?

5. Let α be the percentage of a program code which can be executed simultaneously by n processors of a multiprocessor system. Assume that the remaining code must be executed sequentially on a single processor. Each processor has an execution rate of x MIPS, and all of the processors are equally capable.

   (a) Derive an expression for the effective MIPS rate when using the system to execute this program, in terms of the parameters n, x, and α.

   (b) Let consider the synchronization overhead. When adding an additional processor, the total number of instructions will be increased by β per cent. These added instructions are for synchronization only and they can be executed in parallel. What will be the speedup of the multiprocessor system?