Using Vivado to create a simple Test Bench in VHDL

In this tutorial we will create a simple combinational circuit and then create a test bench (test fixture) to simulate and test the correct operation of the circuit.

Truth table of simple combinational circuit (a, b, and c are inputs. J and k are outputs)

a	b	c	j	k
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	0

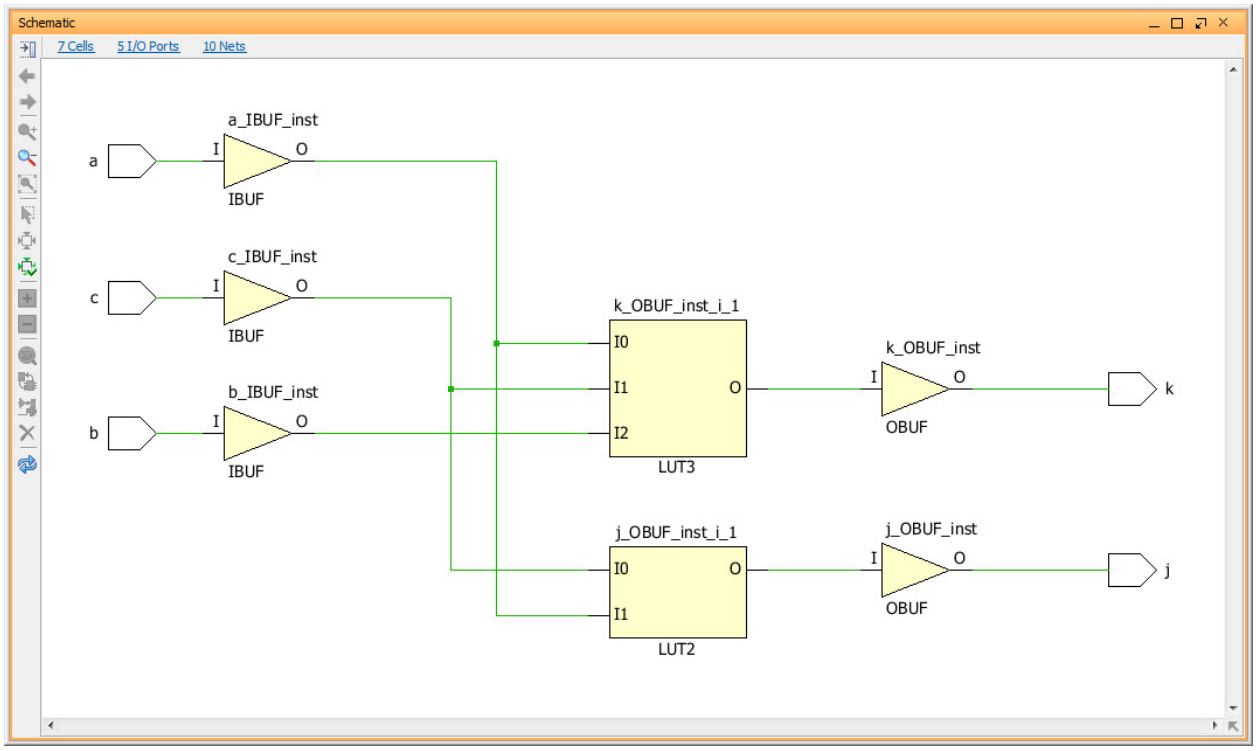
Create a new project and create a VHDL source file describing the behavior of this circuit. For example:

comb.vhd

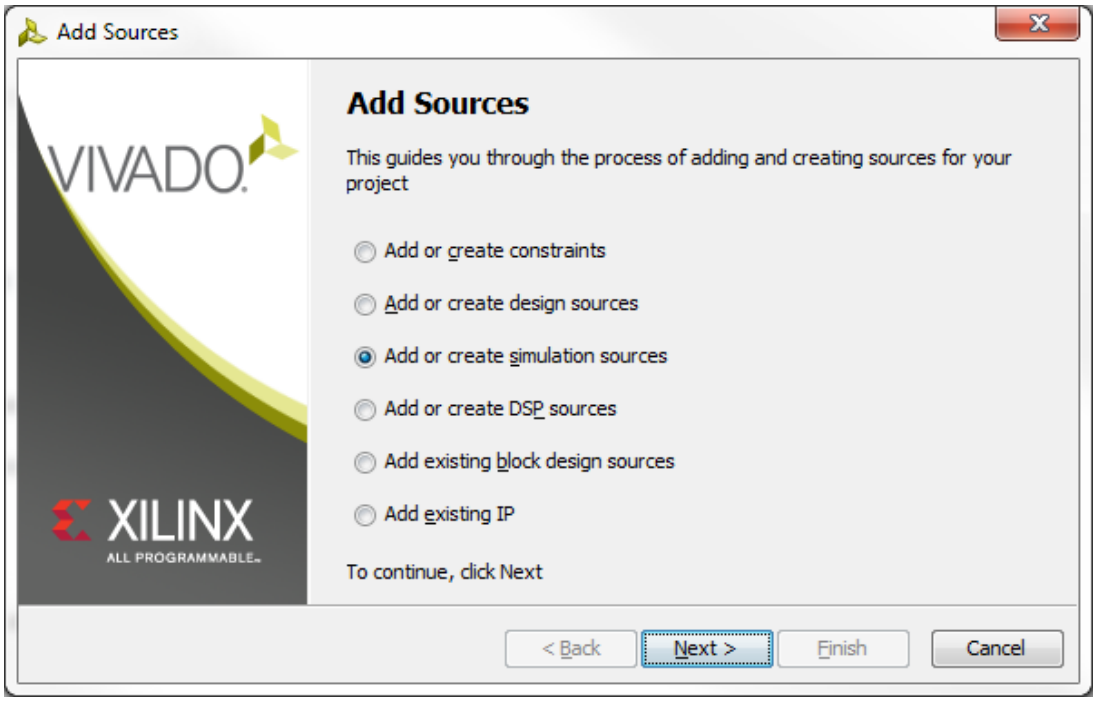
C:/ECE3829/vivado/test_bench/test_bench.srcs/sources_1/new/comb.vhd

```
33
34 entity comb is
35     Port ( a : in STD_LOGIC;
36            b : in STD_LOGIC;
37            c : in STD_LOGIC;
38            j : out STD_LOGIC;
39            k : out STD_LOGIC);
40 end comb;
41
42 architecture Behavioral of comb is
43     signal abc : std_logic_vector(2 downto 0);     -- create internal bus
44 begin
45
46     abc <= a & b & c;    -- combine signals together
47
48     -- example - use conditional signal assignment statement for output j
49     j <= '1' when abc = "001" OR abc = "011" else
50         '0';
51
52     -- example - use process statement for output k
53     process(abc)
54     begin
55         case(abc) is
56             when "000" | "001" | "011" | "100" | "101" =>
57                 k <= '1';
58             when OTHERS =>
59                 k <= '0';
60         end case;
61     end process;
62
63 end Behavioral;
64
```

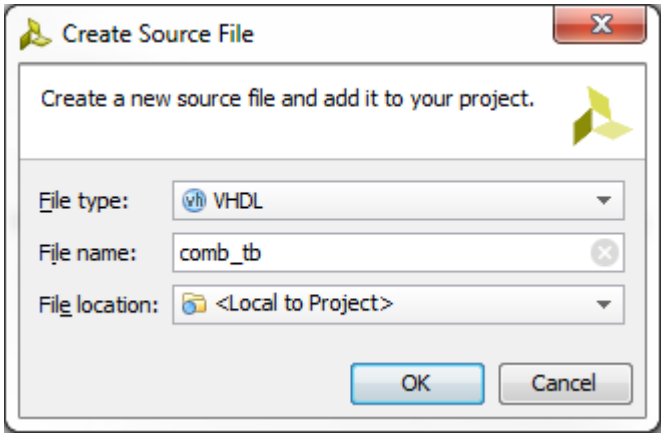
Note: In the Flow Navigator, under Open Synthesized Design you can view a schematic representation of the design:



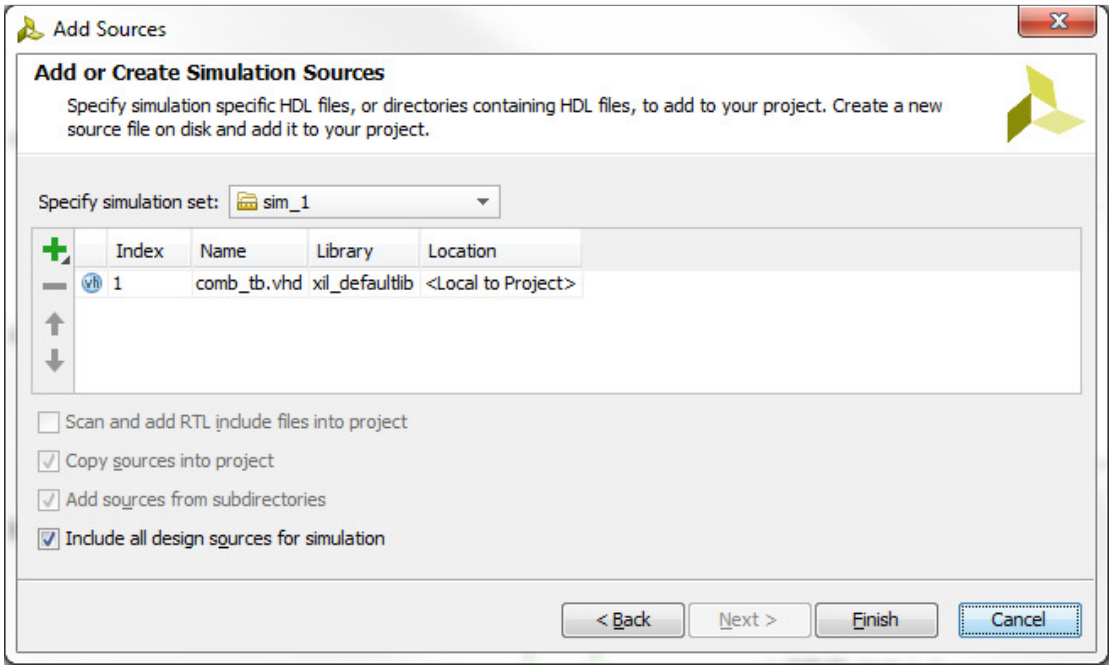
We will now create a simple test bench to test the operation of this combinational circuit. Create a simulation source:



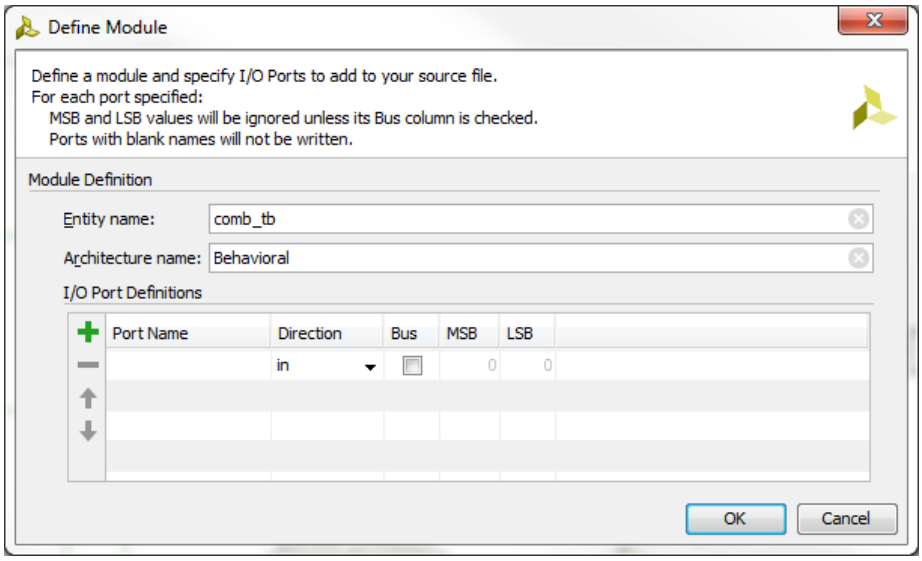
Create a new source file – called comb_tb:



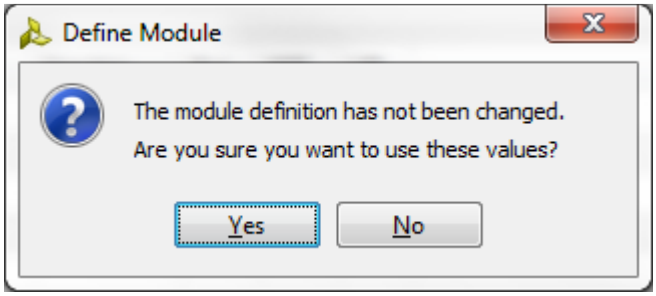
Click **OK**



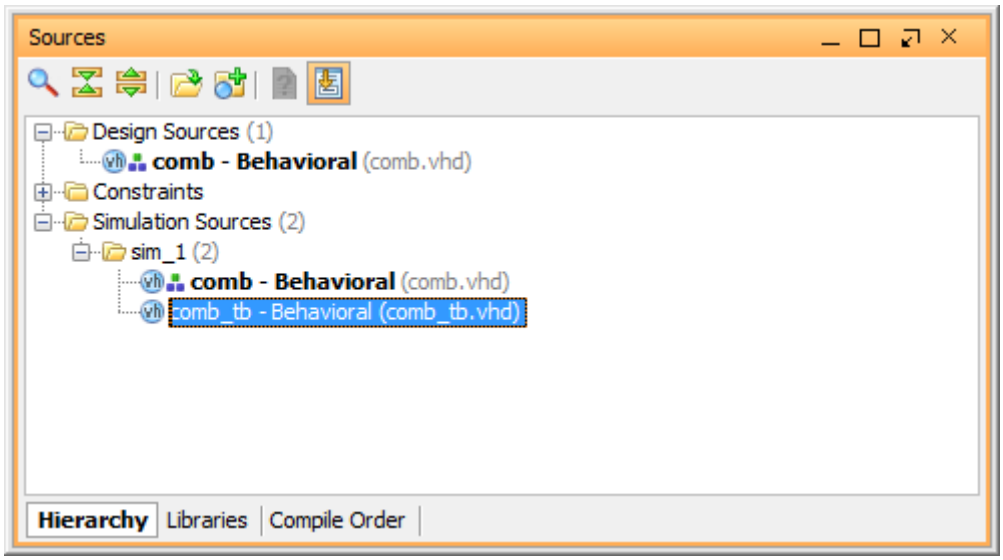
Click **Finish**



A Test Bench does not need any inputs and outputs so just click OK.



Click **Yes,** the text fixture file is added to the simulation sources:



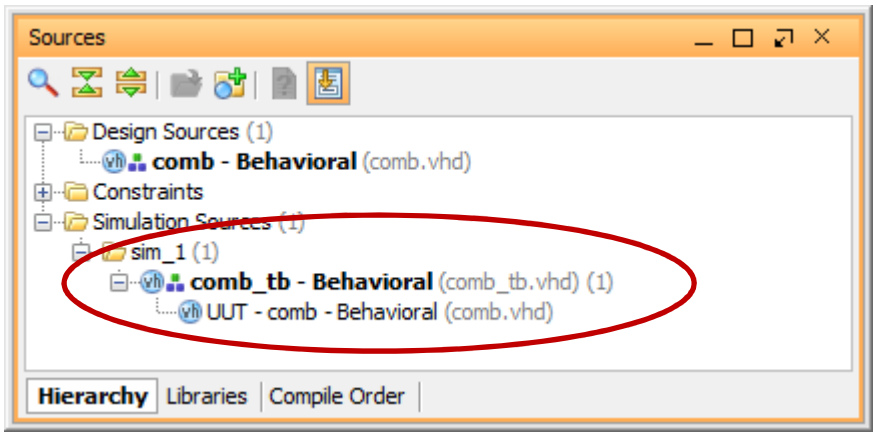
Open up the nearly created *comb.tb* file and add the following VHDL statements to instantiate a copy of the *comb* module and create a simple test bench:

comb_tb.vhd

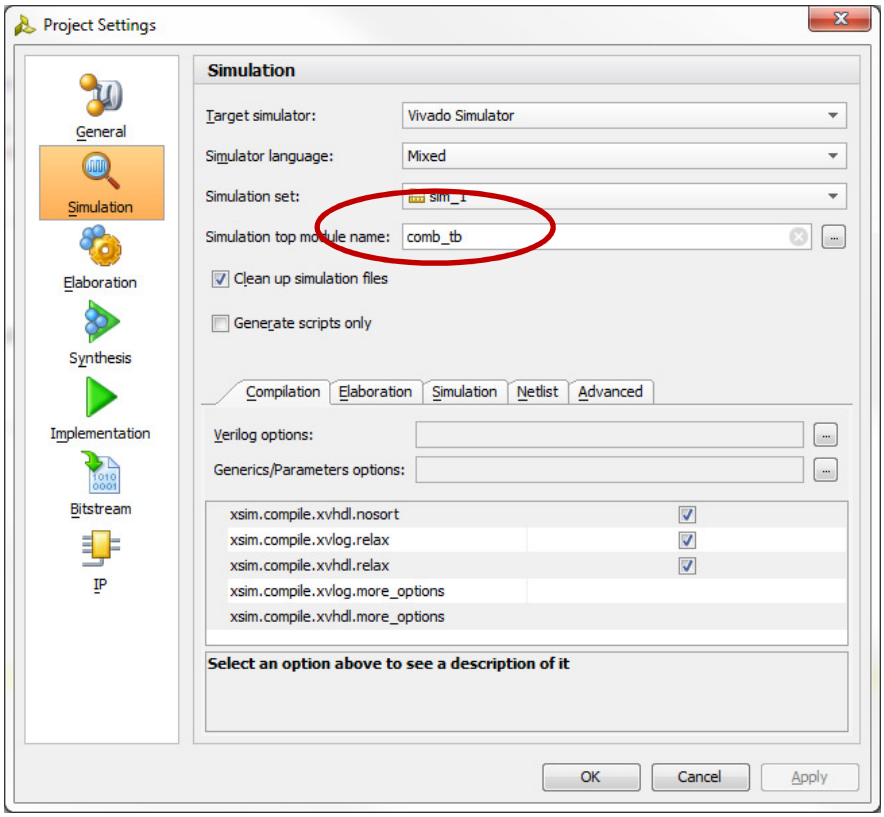
C:/ECE3829/vivado/test_bench/test_bench.srcs/sim_1/new/comb_tb.vhd

```
33
34 entity comb_tb is
35 --  Port ( );
36 end comb_tb;
37
38 architecture Behavioral of comb_tb is
39     component comb                                -- declare component to test
40         port (a, b, c : in std_logic;
41               j, k    : out std_logic);
42     end component;
43
44     signal abc : std_logic_vector (2 downto 0); -- create internal signals
45     signal j, k : std_logic;
46
47 begin
48
49     -- instantiate component for test, connect ports to internal signals
50     UUT: comb port map (a => abc(2), b => abc(1), c => abc(0), j => j, k => k);
51
52     process
53     begin
54         abc <= "000";        -- apply input stimulus, check each input combination
55         wait for 100 ns;
56         abc <= "001";
57         wait for 100 ns;
58         abc <= "010";
59         wait for 100 ns;
60         abc <= "011";
61         wait for 100 ns;
62         abc <= "100";
63         wait for 100 ns;
64         abc <= "101";
65         wait for 100 ns;
66         abc <= "110";
67         wait for 100 ns;
68         abc <= "111";
69         wait;
70     end process;
71
72 end Behavioral;
73
```

Click **save** and you will the Simulation Sources hierarchy is now updated:



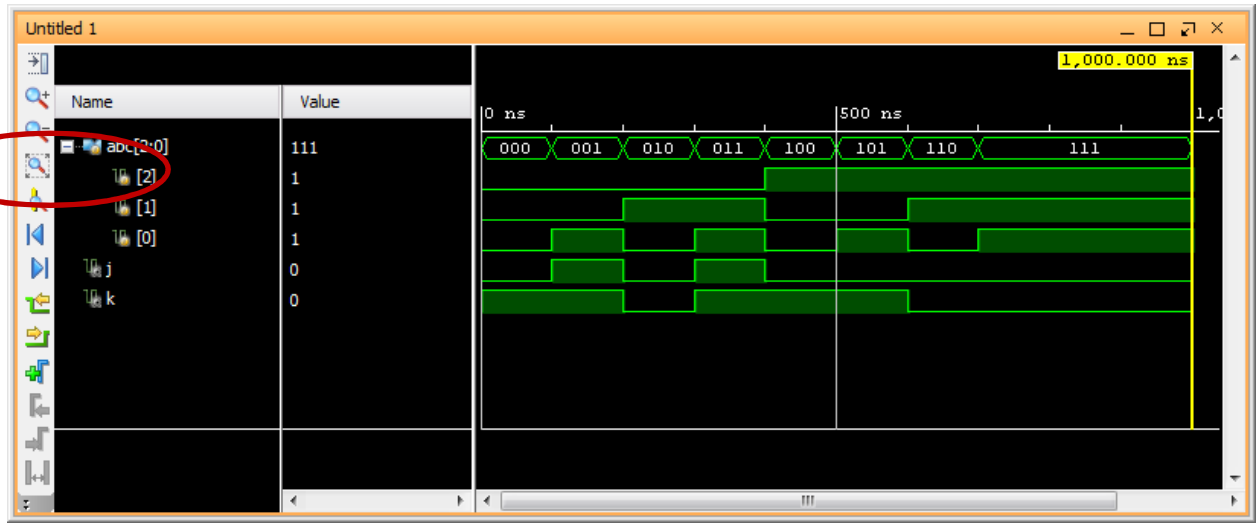
In the Flow navigator select Simulation Settings and verify the Simulation top module name is comb_tb:



In the Flow Navigator select **Run Simulation** => **Run Behavioral Simulation**

A simulation window will open.

Select the Zoom Fit option on the left and you will see the simulation results:



You can visually check the j and k outputs and verify they match the truth table.