Encoder (VHDL and Verilog) – Xilinx Implementation and Simulation (updated by Kahraman Akdemir, September 2006)

Start Project Navigator. Select File => New Project

Enter name and location, select device.

Select New Source. Select VHDL Module and provide name:

📧 New Source Wizard - Select Source Type	_
 IP (Coregen & Architecture Wizard) Schematic State Diagram Test Bench WaveForm User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Library VHDL Package VHDL Test Bench Embedded Processor 	Eile name: encoder Logation: C:\Documents and Settings\Kahraman\Desktop\en
More Info	< Back Next > Cancel

Click Next.

Enter required inputs and Outputs:

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<i>,</i>	Architecture Name Behav	vioral				
	Port Name	Direction	Bus	MSB	LSB	
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Click Next, etc.

A	skeleton	of your	VHDL	file	is	created:
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- 🐂 🐂 encoder - Behavioral (encoder.vhd)	6	Unc	omment t	he foll	owing library declaration if	instantiating
	7	any	Xilinx	primiti	ves in this code.	
	8	librar	y UNISIN	1;		
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	11	entity e	ncoder i			
	12	Port	(i0 :	in STD	LOGIC:	
	13		i1 :	in STD	LOGIC;	
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	15		i3 :	in STD	LOGIC;	
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Enter the architecture statements.

Double-click on the Synthesize-XST in the process window.

Note the	warning	message	(this is	valid).



Double-click View RTL schematic:



Double-click on the symbol to go down a level:



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Go back to the process window

Functional Simulation using automatically created VHDL test bench file.

Select **Project => New source**

Select Test Bench Waveform and provide a file name

🔤 New Source Wizard - Select Source Type	
Image: Second	Eile name: encoder_waveform Logation: C:\Documents and Settings\Kahraman\Desktop\en
More Info	< Back Next > Cancel

Click on **Next**, etc until you see the Initialize Timing window:

📧 Initial Timing and Clock Wizard - Initialize	Timing 📃 🗌 🗙
Assign C	Check Assign
Inputs O	outputs Inputs
Wait To	Wait To
Check	Assign
Clock Timing Information	Clock Information
Inputs are assigned at "Input Setup Time" and	Clock Information
outputs are checked at "Output Valid Delay".	Multiple Clocks
C Rising Edge C Falling Edge	Combinatorial (or internal clock)
Dual Edge (DDR or DET)	Combinatorial Timing Information
Clock High Time 100 ns	Inputs are assigned, outputs are decoded then
Clock Low Time 100 ns	checked. A delay between inputs and outputs avoids
Input Setup Time 15 ns	assignment/checking conflicts.
Output Valid Delay 15 ns	Check Outputs 50 ns After Inputs are Assigned
Offset 0 ns	Assign Inputs 50 ns After Outputs are Checked
Global Signals	Initial Length of Test Bench: \$\\$000 ns
F PRLD (CPLD) F GSR (FPGA)	Time Scale: ns \$\scales\$
High for Initial: 100 ns	Add Asynchronous Signal Support
More Info	< Back Einish Cancel

Click on FINISH

A default set of waveforms for the inputs are created. **IMPORTANT:** You need to select **"Behavioral Simulation"** in the **Sources For** section on the left to be able to run the simulations. Click on the blue parts of the input lines to toggle the level to set up an appropriate set of input combinations. Then click File-Save all. Next you need to select the **"Processes"** section under **"Processes"** tab on the left.



Go back to the Project Navigator. You can either use ModelSim or ISE simulators as described in the following sections. The ISE simulator is probably the easiest to use for quick checks on your designs. Modelsim is far more powerful and flexible and we will use this when we work with test benches.

a) MODELSIM Simulator

Double-click on the *Simulate Behavioral VHDL Model* process to launch the ModelSim Simulator – ModelSim starts and displays many windows!

Go to the *Waveform Viewer* window and zoom back out to see the results of your simulation:

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b) ISE Simulator

Double-click on the *Generate Expected Simulation Results* process to launch the ISE Simulator.

Click Yes

🎫 Test I	Bench Waveform Editor
?	Only one instance of encoder_waveform.tbw can be active at once. Would you like to close the current encoder_waveform.tbw and open a new one?
	<u>Yes</u> <u>N</u> o Cancel

Click Yes

🚾 Ехрес	ted Results
?	Replace outputs with expected values? Selecting No adds the expected values as signals to the display for comparison.
	<u>Yes</u> <u>N</u> o Cancel

And you get the outputs as shown in the following window.

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Alternative Verilog Design

NOTE: As you would expect, an equivalent Verilog Design will result in exactly the same logic being produced and the same simulation results.

Start Project Navigator. Select **File => New Project** Enter name and location, select device. Select **New Source**. Select *Verilog Module* and provide name:

New Source	
Schematic Schematic	Ele Name: encodel Logation: c:\verilog\encoder_ver
< <u>B</u> ack <u>N</u> ext> Cancel Help	

A Verilog skeleton is produced, add behavioral statements:



The rest of the steps are equivalent to the VHDL example.