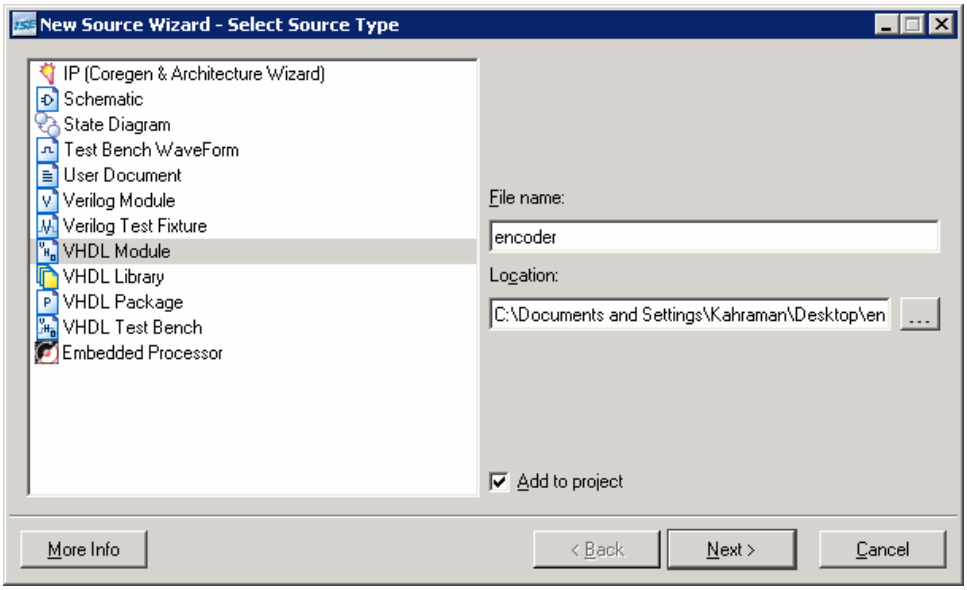
Encoder (VHDL and Verilog) – Xilinx Implementation and Simulation
(updated by Kahraman Akdemir, September 2006)

Start Project Navigator. Select **File => New Project**

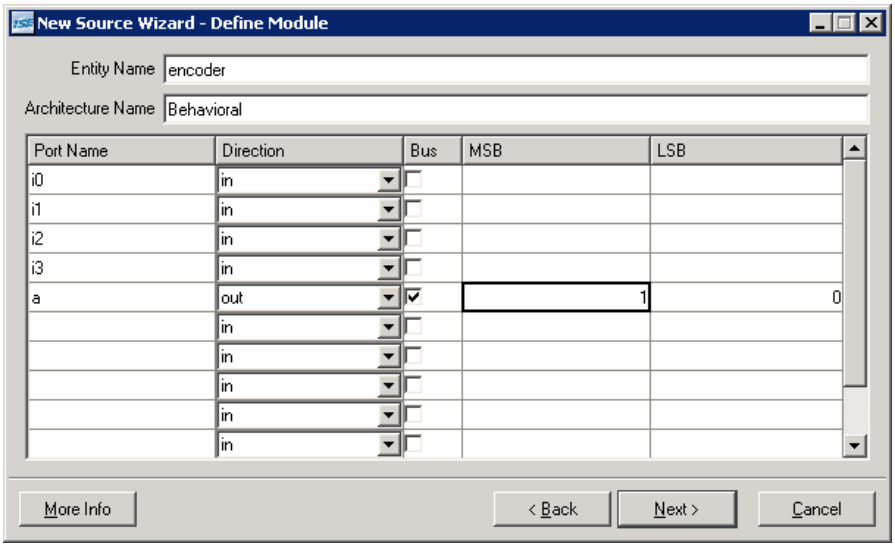
Enter name and location, select device.

Select **New Source**. Select *VHDL Module* and provide name:



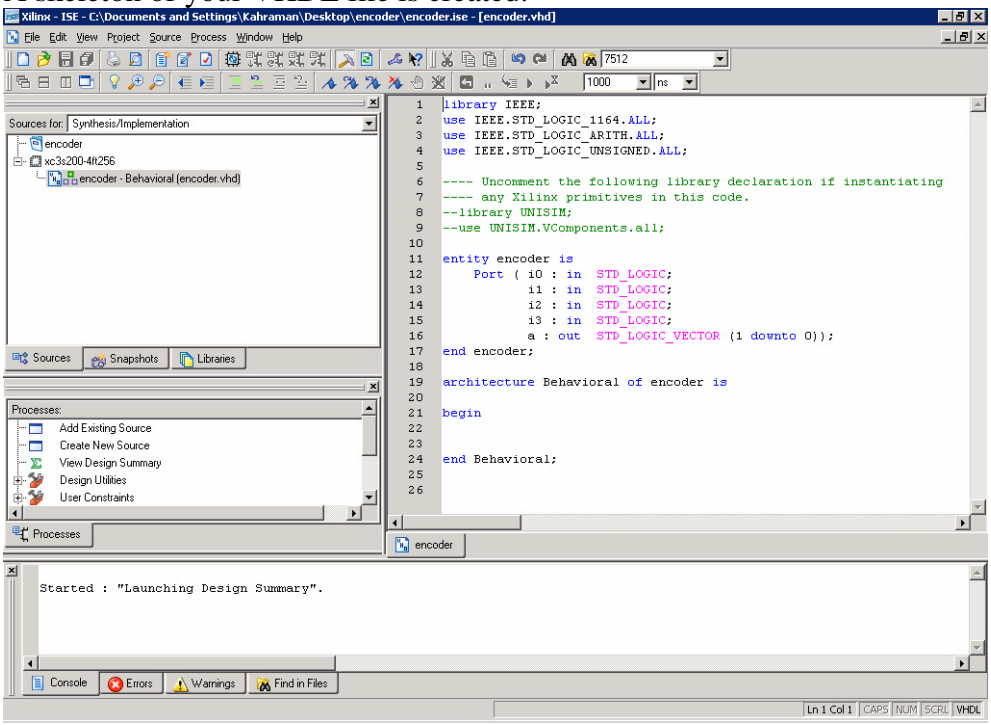
Click **Next**.

Enter required inputs and Outputs:



Click **Next, etc.**

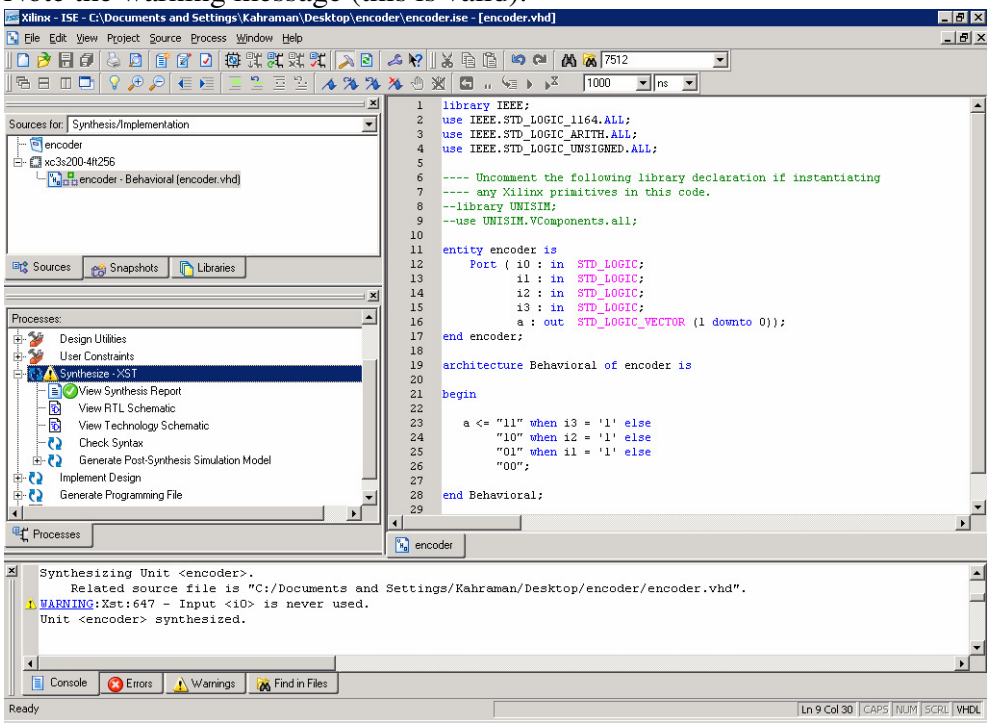
A skeleton of your VHDL file is created:



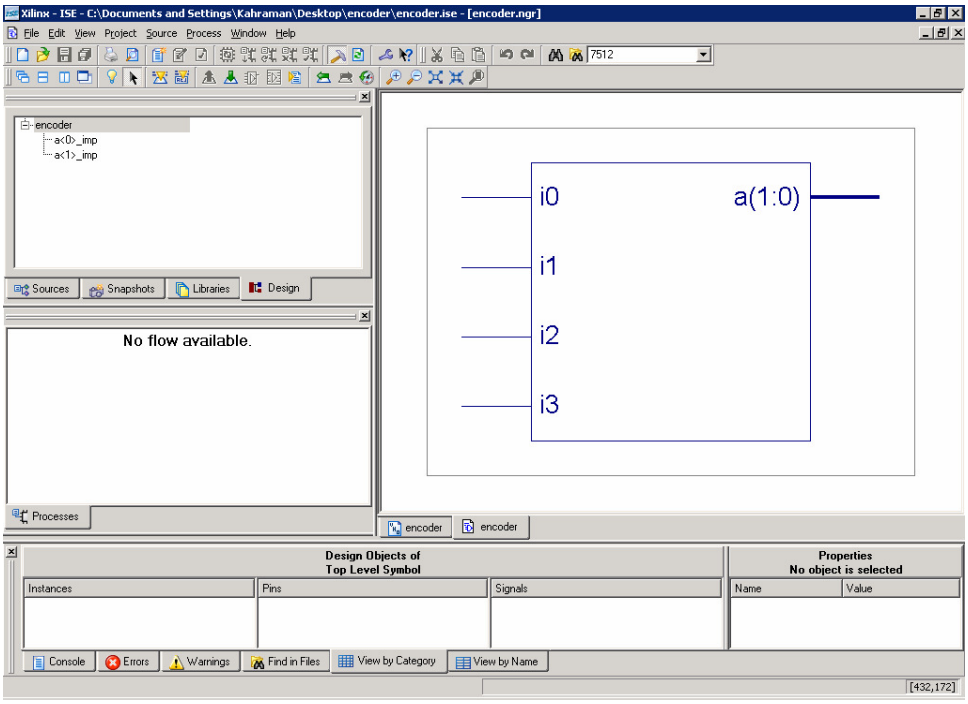
Enter the architecture statements.

Double-click on the *Synthesize-XST* in the process window.

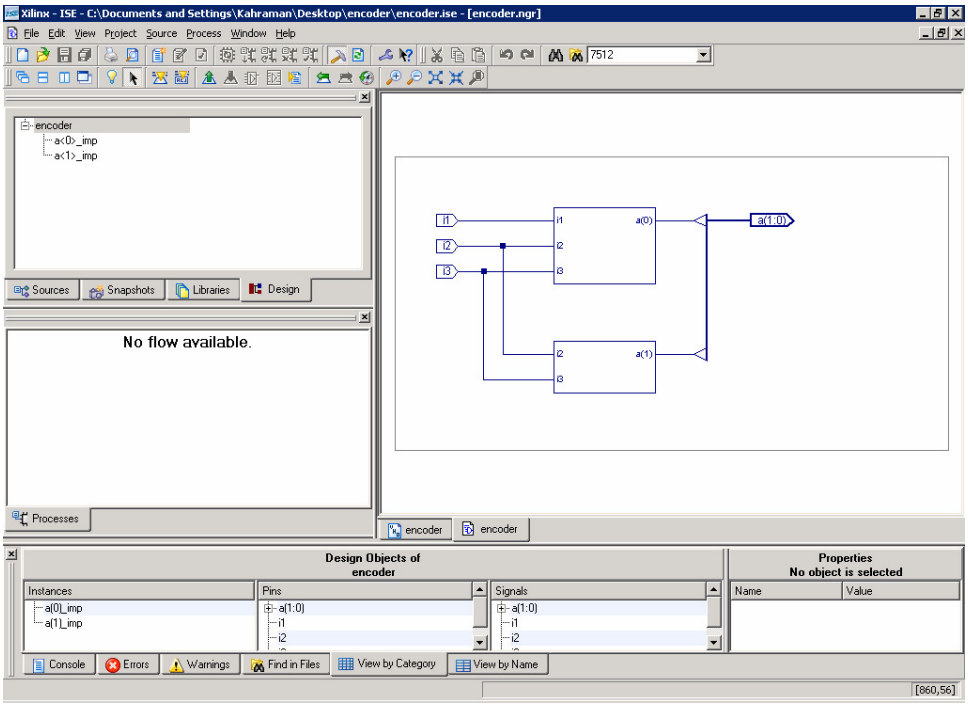
Note the warning message (this is valid).

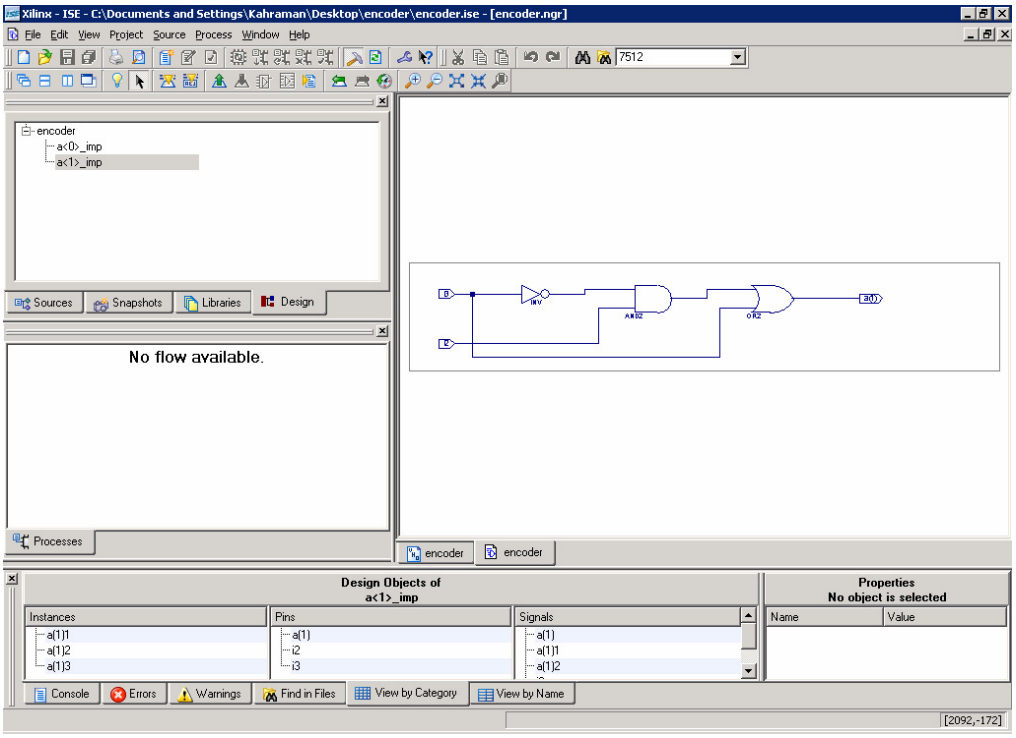


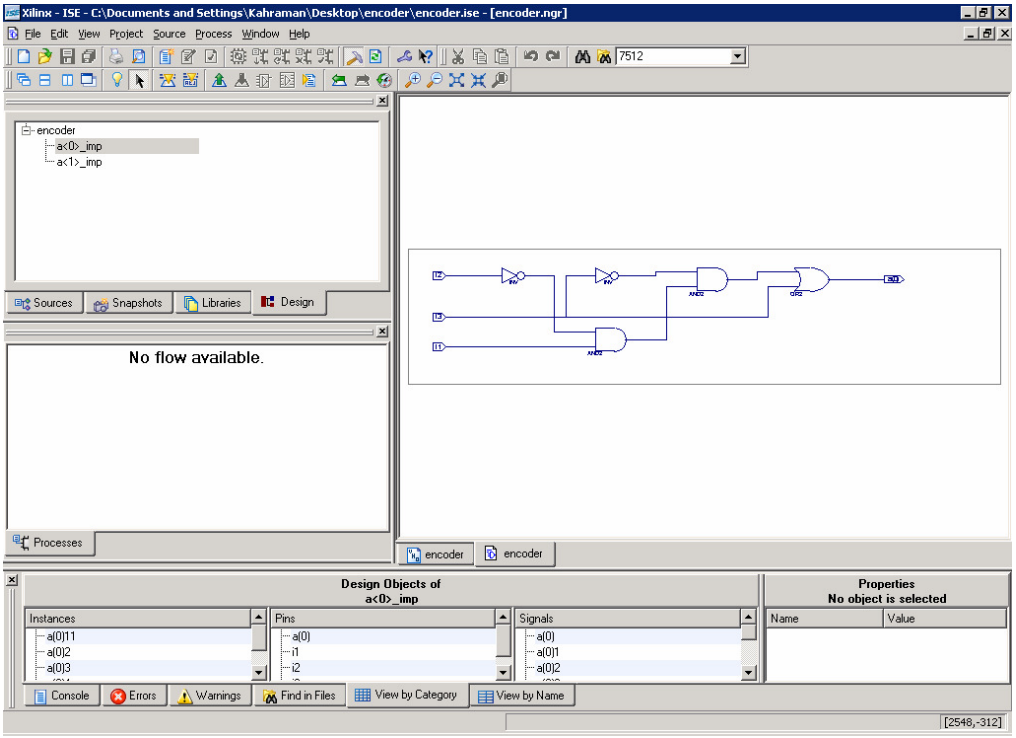
Double-click *View RTL schematic*:



Double-click on the symbol to go down a level:





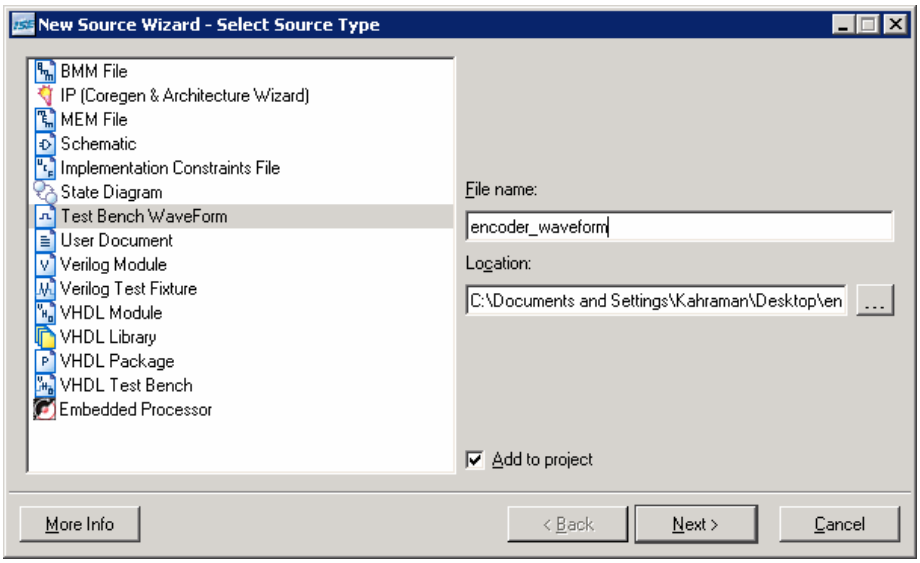


Go back to the process window

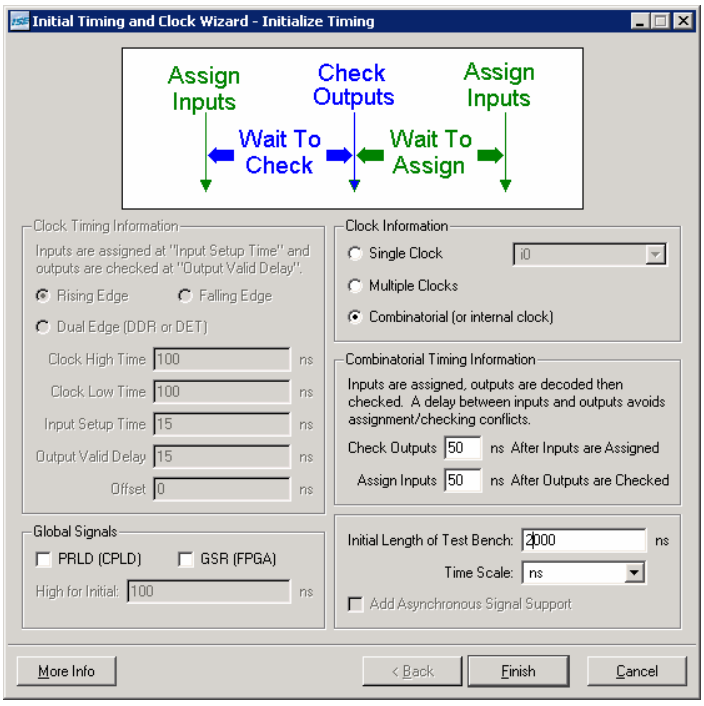
Functional Simulation using automatically created VHDL test bench file.

Select **Project => New source**

Select *Test Bench Waveform* and provide a file name

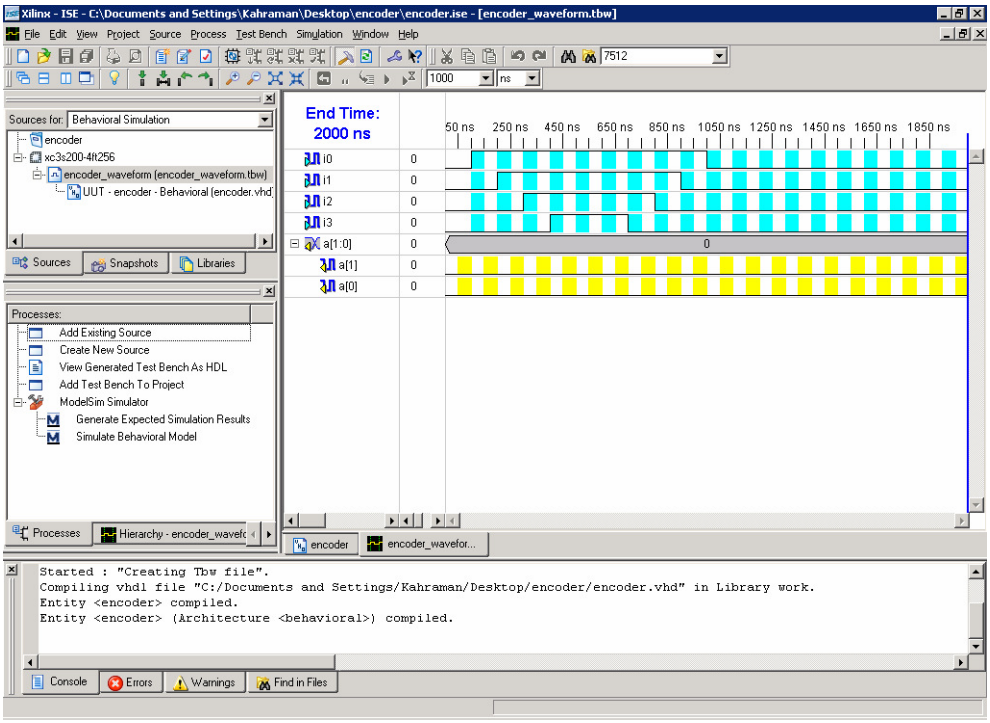


Click on **Next**, etc until you see the Initialize Timing window:



Click on **FINISH**

A default set of waveforms for the inputs are created. **IMPORTANT:** You need to select **"Behavioral Simulation"** in the **Sources For** section on the left to be able to run the simulations. Click on the blue parts of the input lines to toggle the level to set up an appropriate set of input combinations. Then click File-Save all. Next you need to select the **"Processes"** section under **"Processes"** tab on the left.

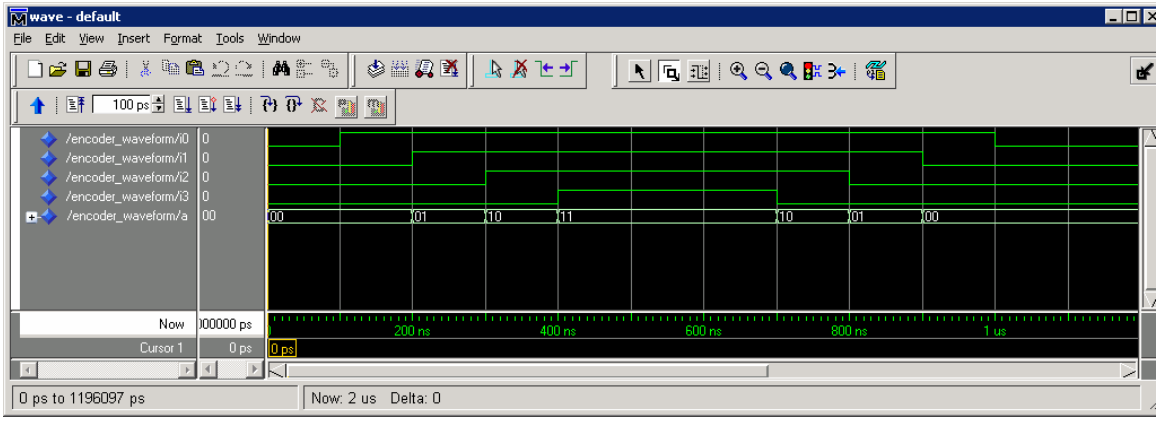


Go back to the Project Navigator. You can either use ModelSim or ISE simulators as described in the following sections. The ISE simulator is probably the easiest to use for quick checks on your designs. Modelsim is far more powerful and flexible and we will use this when we work with test benches.

a) MODELSIM Simulator

Double-click on the *Simulate Behavioral VHDL Model* process to launch the ModelSim Simulator – ModelSim starts and displays many windows!

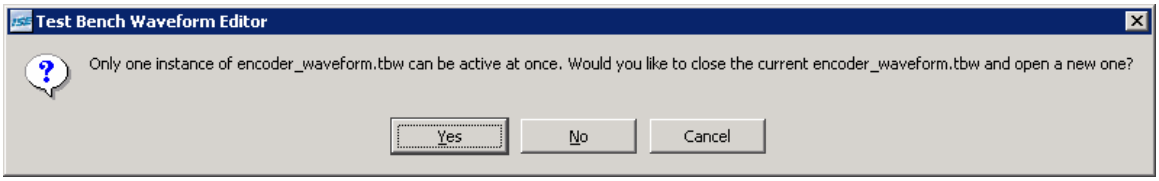
Go to the *Waveform Viewer* window and zoom back out to see the results of your simulation:



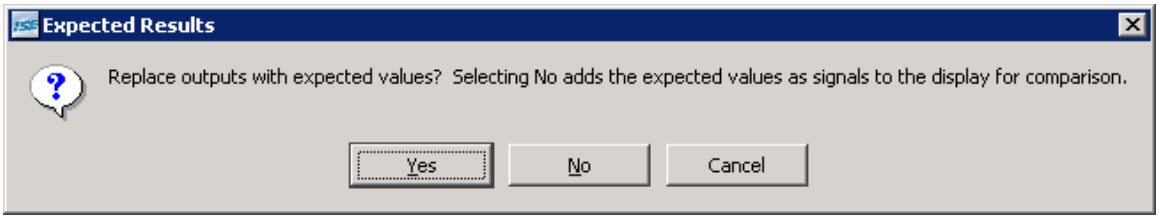
b) ISE Simulator

Double-click on the *Generate Expected Simulation Results* process to launch the ISE Simulator.

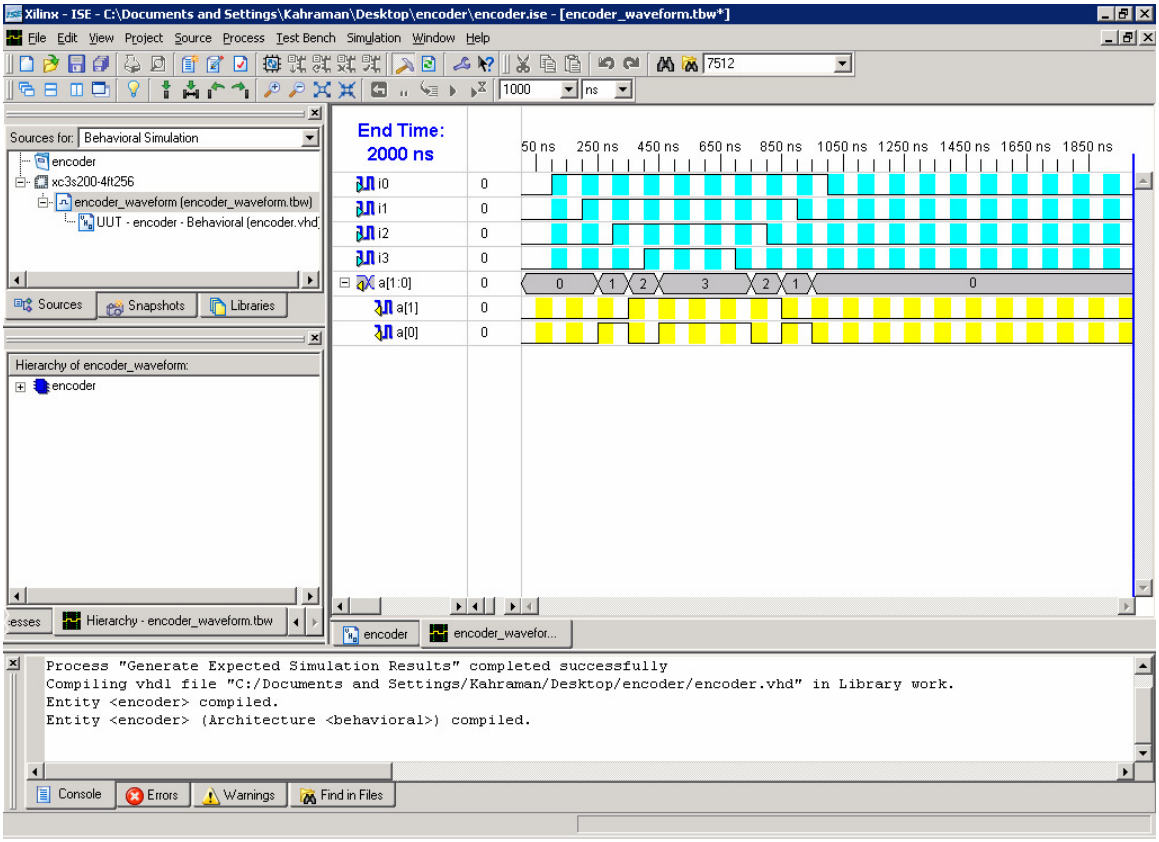
Click **Yes**



Click **Yes**



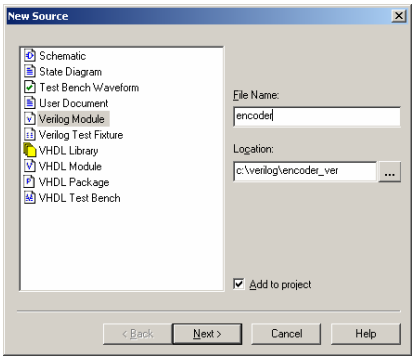
And you get the outputs as shown in the following window.


Xilinx - ISE - C:\Documents and Settings\Kahraman\Desktop\encoder\encoder.ise - [encoder_waveform.tbw*]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
encoder
xc3s200-4ft256
encoder_waveform (encoder_waveform.tbw)
UUT - encoder - Behavioral (encoder.vhd
Sources
Snapshots
Libraries
Hierarchy of encoder_waveform:
encoder
Hierarchy - encoder_waveform.tbw
End Time:
2000 ns
50 ns
250 ns
450 ns
650 ns
850 ns
1050 ns
1250 ns
1450 ns
1650 ns
1850 ns
i0
i1
i2
i3
a[1:0]
a[1]
a[0]
encoder
encoder_wavefor...
Process "Generate Expected Simulation Results" completed successfully
Compiling vhdl file "C:/Documents and Settings/Kahraman/Desktop/encoder/encoder.vhd" in Library work.
Entity <encoder> compiled.
Entity <encoder> (Architecture <behavioral>) compiled.
Console
Errors
Warnings
Find in Files

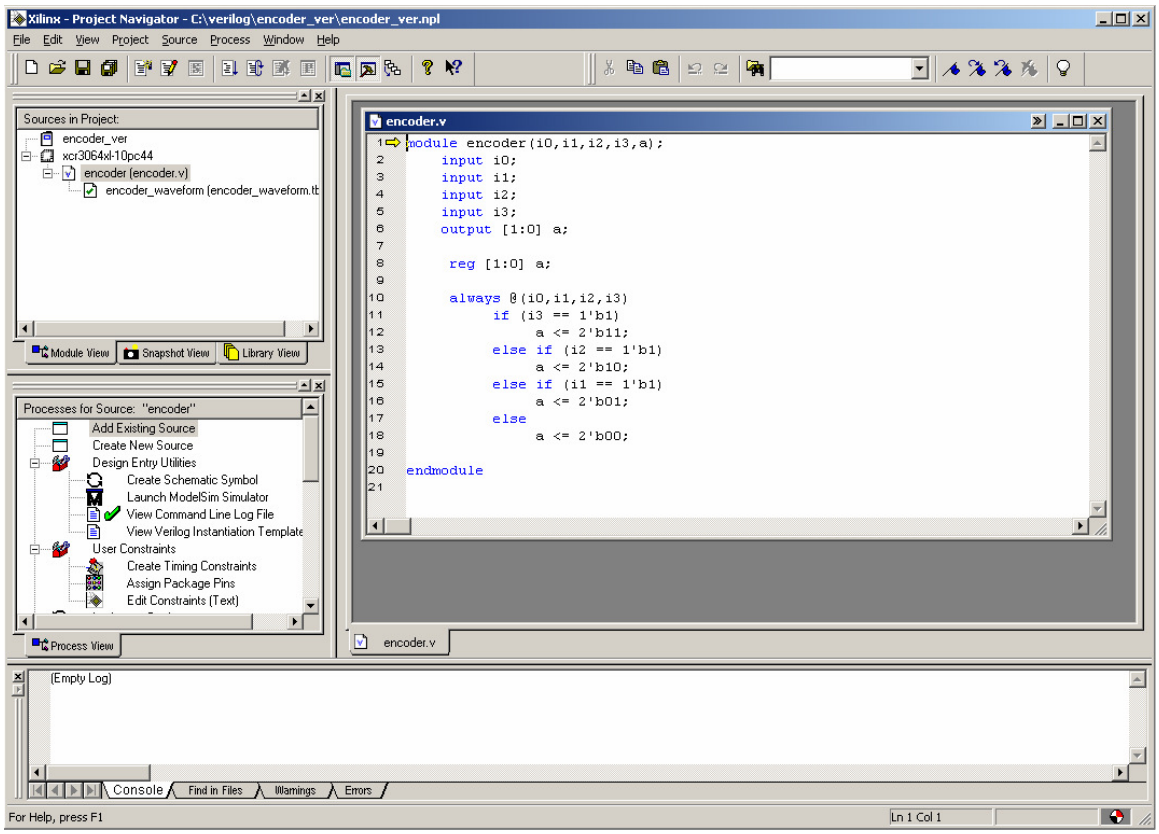
Alternative Verilog Design

NOTE: As you would expect, an equivalent Verilog Design will result in exactly the same logic being produced and the same simulation results.

Start Project Navigator. Select **File => New Project**
Enter name and location, select device.
Select **New Source**. Select *Verilog Module* and provide name:



A Verilog skeleton is produced, add behavioral statements:



The rest of the steps are equivalent to the VHDL example.