A Novel Architecture for Fast Self-Calibration of High-Speed High-Accuracy ADCs

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Outline

• Background
  – Goals
  – Cyclic ADC Review
  – Previous Self-Calibration Techniques

• "Split ADC" Architecture
  – Design Details
  – Measured Results

• Conclusion
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Goals

General: Take advantage of CMOS scaling

• Digital
  – Relax requirements on analog precision
  – All calibration / complexity in digital domain

• Background
  – Calibration continuous in background

• Deterministic
  – Short time constant for adaptation
  – No requirements on input signal behavior

Specific Implementation:
16b 1MS/s Cyclic ADC
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Cyclic ADC Review

1) Sample input, compare to threshold
   → digital decision $d$
2) Amplify input by factor $G$
3) Subtract $dV_{REF}$ → residue voltage $v_{RES}$
4) Repeat cycle with $v_{RES}$ as input
   Result: sequence of decisions $d_k$
Cyclic ADC Review

Residue amplifier:

Residue plot:

Input-Output Relationship:

\[ v_{RES(O)} = G \cdot v_{RES(I)} - d \cdot V_{REF} \]

Multiply input by cyclic gain \( G \), subtract \( d \cdot V_{REF} \)
Example: 3-Cycle ADC

• Follow residues; start ...
  \[ \nu_{IN} \]
  \[ \downarrow \]

• Cycle 1 residue:
  \[ \nu_{RES(1)} = G\nu_{IN} - d_1V_{REF} \]
  \[ \downarrow \]
  \[ \nu_{RES(1)} \]

• Cycle 2:
  \[ \nu_{RES(2)} = G\left[ G\nu_{IN} - d_1V_{REF} \right] - d_2V_{REF} \]
  \[ \downarrow \]
  \[ \nu_{RES(2)} \]

• Cycle 3:
  \[ \nu_{RES(3)} = G\left[ G\left[ G\nu_{IN} - d_1V_{REF} \right] - d_2V_{REF} \right] - d_3V_{REF} \]

• Rearrange:
  \[ \nu_{RES(3)} = G^3\nu_{IN} - \left[ G^2d_1 + Gd_2 + G^0d_3 \right]V_{REF} \]
1: Cyclic ADC as Negative Feedback Loop

\[ v_{RES(3)} = G^3 v_{IN} - \left[ G^2 d_1 + G^1 d_2 + G^0 d_3 \right] V_{REF} \]

- Cyclic amplifier trying to "blow up" \( v_{IN} \)
- DAC trying to drive residue to zero

• Residue voltages bounded if \( G \) isn't "too big"
Residue plots for $G$

- **$G < 2$**
  - $v_{\text{MAX}} > V_{\text{REF}}$: OK
- **$G = 2$**
  - $v_{\text{MAX}} = V_{\text{REF}}$: OK (just barely)
- **$G > 2$**
  - $v_{\text{MAX}} < V_{\text{REF}}$: TROUBLE!

- Maximum allowable residue voltage: $v_{\text{MAX}} = \left(\frac{1}{G - 1}\right)V_{\text{REF}}$
- Safety margin: Choose $G < 2$
- Bonus: Redundancy
Redundancy

• Key: Multiple valid decision paths to output code
  
  \(-1\) or \(+1\) OK
2: Digital Correction

• Divide both sides by $G^3 V_{REF}$ and rearrange

$$\frac{v_{IN}}{V_{REF}} = \frac{1}{G} d_1 + \frac{1}{G^2} d_2 + \frac{1}{G^3} d_3 - \frac{1}{G^3} \frac{v_{RES(3)}}{V_{REF}}$$

Output code $x$ (radix $G$)  Quantization error

• Digital reconstruction from comparator decisions $d_k$: Use estimated gain $G_{(EST)}$ to calculate output code $x :$

$$x_{(EST)} = \left( \frac{1}{G_{(EST)}} \right) d_1 + \left( \frac{1}{G_{(EST)}} \right)^2 d_2 + \left( \frac{1}{G_{(EST)}} \right)^3 d_3$$

• Only $G$ needed to digitally correct ADC linearity
• Calibration: $G_{(EST)} = G$ to within converter accuracy
Outline

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### Previous Calibration Techniques

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</table>

• No previous technique has all desired features

2. Murmann ..., "A 12b 75MS/s Pipelined ADC using open-loop residue amplification," ISSCC2003
3. Liu .., "A 15b 20MS/s CMOS Pipelined ADC with Digital Background Calibration," ISSCC2004
5. Ryu ..., "A 14b-Linear Capacitor Self-Trimming Pipelined ADC," ISSCC2004
7. Chiu ..., "Least mean square adaptive digital background calibration of pipelined ADCs," TCAS-I, Jan. 2004
### Deterministic Digital Techniques

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- Require calibration mode of operation, taking ADC off line
- Substitute known signal for input
### Deterministic Background Techniques

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- Requires added analog complexity:
  - Queue-based: additional S/H stage, insert known signal for calibration [6]
  - Slow-but-accurate ADC in parallel [7]
Digital Background Techniques

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- Statistical methods; examples:
  - PRN modulation of DAC segment selection [1]
  - PRN choice of two residue modes [2]
- About $2^{2N}$ samples needed to decorrelate calibration signal from unknown ADC input
Previous Digital Background Calibration

CONVERSIONS REQUIRED FOR CALIBRATION

$2^{2N}$

10^9
10^8
10^7
10^6
10^5
10^4

N

CONVERSIONS

12 14 16

RESOLUTION

10^4
10^5
10^6
10^7
10^8
10^9

N

BITS

1
2
3
4
5

Statistical Techniques Problem

How long to calibrate with $2^{2N}$ samples?

<table>
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<tr>
<th>12 bits, 75 MS/s [2]</th>
<th>16 bits, 1 MS/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{2^{2\cdot12}}{75\text{Msps}} \approx 200\text{ms}$</td>
<td>$\frac{2^{2\cdot16}}{1\text{Msps}} \approx 1\text{ hour}$</td>
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⇒ Deterministic approach needed

The problem: How to do a …
– deterministic calibration procedure
– in background
– without a known input?
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Split ADC Architecture

- Average of A, B results is ADC output code
- Calibration signal developed from difference

\[ x = \frac{x_A + x_B}{2} \]

\[ \Delta x = x_B - x_A \]
Intuitive View of Split ADC

- Different paths to (ideally) same answer
- Estimate errors from "disagreements"
- Only way for A, B to always agree is for both to be correctly calibrated
Robert Frost: “New Hampshire”

“... a figure of the way
the strong of mind
and strong of arm
should fit together,
One thick where one is thin
and vice versa. ”

• Key idea: two “partners”
  trying to do the same thing
  in different ways
### Same Area, Noise, Speed, Power

**ANALOG**

- $v_{IN}$
- $C$
- $g_m$

**DIGITAL**

- $x$

**SPLIT**

- $v_{IN}$
- $x$

**ANALOG**

- $C/2$
- $g_m/2$

**DIGITAL**

- $x_A + x_B$

### Speed

- $f_T = b \frac{g_m}{C}$
- $b \frac{g_m/2}{C/2} = \frac{b}{2} \frac{g_m}{C}$

### Power

- $P = p \cdot g_m$
- $p \cdot \frac{g_m}{2} + p \cdot \frac{g_m}{2} = p \cdot g_m$

### Noise

- $\sigma_x = n \sqrt{\frac{kT}{C}}$
- $\sqrt{\left(\frac{1}{2} n \sqrt{\frac{kT}{C/2}}\right)^2 + \left(\frac{1}{2} n \sqrt{\frac{kT}{C/2}}\right)^2} = n \sqrt{\frac{kT}{C}}$

- Negligible impact on analog complexity
Outline

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• Conclusion
• Test chip mostly analog
• Digital on FPGA (code "synthesis-ready" for product)
ADC Block Diagram

S/H

$G_A$

DAC

COMPS

PATH A

$v_{IN}$

$\hat{G}_A$

$\frac{1}{\hat{G}_A}$

$\sum$

$x_A$

$\mu$

$\hat{\mu}$

ERROR

COEFF

L.U.T.

$\frac{k}{1/G}$

$\sum$

$\Delta x$

ERROR EST.

$\hat{\varepsilon}_A$

$\hat{\varepsilon}_B$

$\sum$

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ADC Digital Correction

\[v_{IN}\]

\[\Sigma\]

\[d_{kA}\]

\[G_A\]

\[S/H\]

\[\Sigma\]

\[d_{kB}\]

\[G_B\]

\[S/H\]

\[\Sigma\]

\[\hat{G}_A\]

\[\hat{G}_B\]

\[\Sigma\]

\[\Delta x\]

\[\Sigma\]

\[\epsilon_A\]

\[\epsilon_B\]

\[x_A\]

\[x_B\]

\[x\]

\[\Sigma\]

CYCLIC RESIDUE AMPLIFIERS

OFF-CHIP DIGITAL PROCESSOR (FPGA)

ERROR COEFF L.U.T.

"A" L.U.T.

"B" L.U.T.

ERROR EST.
ADC Digital Correction

- Decision weight L.U.T.
  - Periodically recalculated in background
  - Separate L.U.T.s for A, B output codes
Error Estimation

OFF-CHIP DIGITAL PROCESSOR (FPGA)

CYCLIC RESIDUE AMPLIFIERS
Error Estimation

A, B Outputs

\[
\begin{align*}
  x_A & = x + [SDK_A] \varepsilon_A \\
  x_B & = x + [SDK_B] \varepsilon_B 
\end{align*}
\]

Difference

\[
\Delta x = [SDK_B] \varepsilon_B - [SDK_A] \varepsilon_A
\]

- Ideal \( x \) cancelled from estimation signal path
- No need for long decorrelation times
  - Deterministic: solve for \( \varepsilon_A, \varepsilon_B \) from a few \( \Delta x \) observations
Error Estimation

Difference:

\[ \Delta x = \left[ SDK_B \right] \varepsilon_B - \left[ SDK_A \right] \varepsilon_A \]

\( SDK_A, SDK_B \)

Error coefficients

\( \varepsilon_A, \varepsilon_B \)

Fractional errors in \( G_A, G_B \) estimates

\( d_{kA} \) → \( \times \) → \( \Sigma \) → \( SDK_A \)

\( k \left( \frac{1}{G} \right)^k \)

ERROR COEFF L.U.T.

\[ k \left( \frac{1}{G} \right)^k \]

\( \Rightarrow \) Need different \( d_{kA}, d_{kB} \) for “visibility” to errors
Multiple Residue Mode Amplifier

\[ \hat{G}_A \]

\[ \hat{G}_B \]

ERROR COEFF
L.U.T.

CYCLIC RESIDUE AMPLIFIERS

OFF-CHIP DIGITAL PROCESSOR (FPGA)

\[ v_{IN} \]

\[ d_{kA} \]

\[ d_{kB} \]

\[ x_A \]

\[ x_B \]

\[ x \]

\[ \Delta x \]

\[ \hat{\varepsilon}_A \]

\[ \hat{\varepsilon}_B \]

\[ \mu \]

\[ \Sigma \]

\[ + \]

\[ S/H \]

\[ \Sigma \]

\[ - \]

\[ \Sigma \]

\[ + \]

\[ S/H \]

\[ \Sigma \]
Multiple Residue Mode Amplifier

PATH: 00 “CYCLIC”  01 “HIGH”  10 “LOW”  11 “WIDE”

DECISION $d$: -1  +1  -1 0 +1  -1 0 +1  -1 0 +1

• 2b PATH sets residue mode entirely in digital domain
S/H, 1.5b DAC, G=1.92 Cyclic Amplifier

- 2b PATH sets residue mode entirely in digital domain

PATH: 00 “CYCLIC”  01 “HIGH”  10 “LOW”  11 “WIDE”

DECISION d: -1  +1  -1 0 +1  -1 0 +1  -1 0 +1
Cyclic Amplifier: 3-Capacitor?

- **Advantages**
  - Easier to do signal-independent reference current
  - Decouple reference, cyclic gain paths (CM!)
- **Disadvantages**
  - Extra capacitor area
  - Extra noise gain (killer!)
  - Output only valid on one phase (1/2 cycle)
    - Less time for comparator

P. Ferguson, “Practical Aspects of Delta-Sigma Data Converter Design,” MEAD Microelectronics
Cyclic Amplifier: 2-Capacitor

• Advantages
  – Less cap area
  – Lower noise gain
  – Output valid both phases
  • Easier on comparator

• Disadvantages
  – Signal-dependent reference current
  – Reference, cyclic gain paths constrained (CM!)
Cyclic Amplifier: 2-Capacitor

- 2-Cap chosen:
  - Lower total capacitance for a given noise performance
- Different feedback $\beta$ in DAC, sample modes
  - Changes effect of amplifier noise

"DAC mode" $\beta \sim 1/2$

"Sample mode" $\beta \sim 1$
S/H, 1.5b DAC, G=1.92 Cyclic Amplifier

- kT/C noise limited
  ⇒ large C
Op-Amp

- kT/C noise limited ⇒ large C
# Op-Amp Requirements

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<th>Spec</th>
<th>Comments</th>
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<td>$C_L$</td>
<td>20-30pF</td>
<td>Required by $kT/C$ noise limit</td>
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<tr>
<td>$I_{DD}$</td>
<td>33mA</td>
<td>80% of total IC power goal (100mW)</td>
</tr>
<tr>
<td>$f_T$</td>
<td>150 MHz</td>
<td>16 bit settling, 30 ns, 1st half cycle</td>
</tr>
<tr>
<td>$A_{OL}$</td>
<td>100 dB</td>
<td>Maintain over full signal range</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>+/- 1.8V</td>
<td>Trade SNR, linearity</td>
</tr>
<tr>
<td>SR</td>
<td>500 V/us</td>
<td>Trade with $f_T$, settling time</td>
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</table>
SNR $\rightarrow \pm 2\text{Vpp swing}$ $\rightarrow$ Output not cascoded
16b linear $\rightarrow \sim 100\text{dB } A_{OL} \rightarrow$ 2-stage
$\Rightarrow$ First stage $\rightarrow$ Gain boosted cascode

Bult & Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," JSSC, Dec 1990
Pan et. al., "A 3.3-V 12-b 50-MS/s A/D converter in 0.6-µm CMOS with over 80-dB SFDR," JSSC, Dec. 2000
Op-Amp: Design for 90dB SNR

- Noise contributors:
  - Sample cap $kT/C$
  - Op-amp $g_m$

- Plot SNR, total current as function of $C_F$, $I_{BIAS}$
Op-Amp: $I_{\text{BIAS}}$ $C_F$ Optimization

DIFF PAIR
$I_{\text{BIAS}}$ [A]

TOTAL OP-AMP CURRENT [mA]

SNR [dB]

SAMPLE CAPACITANCE $C_F$ [F]
Op-Amp: $I_{\text{BIAS}}$ $C_F$ Optimization

**TOTAL CURRENT [mA]**

$\text{SNR [dB]}$

- **Radix**: 1.9
- **Internal FSR**: 1.8 V
- **nSlew**: $6\tau$
- **$\tau$**: 1.25 ns
- **Input $I_d/g_m$**: 0.15789 \$
- **$R_{SL}/R_{SD}$**: 5

**DESIGN POINT 1**
- $C_F = 26.0$ pF
- $I_B = 8.00$ mA

**DESIGN POINT 2**
- $C_F = 29.0$ pF
- $I_B = 6.50$ mA

$C_F$ limited

$g_m$ limited

$\text{SNR} \rightarrow 90\text{dB} \rightarrow \text{Bias current, sample cap tradeoff}$
Outline

• Background
  – Goals
  – Cyclic ADC Review
  – Previous Self-Calibration Techniques

• "Split ADC" Architecture
  – Design Details
    – Measured Results

• Conclusion
Measured INL

- --- uncalibrated
- --- calibrated

INL [LSB]

Code

0 32768 65535
Temperature Performance

$T = +85 \degree C$, calibrated

$T = -40 \degree C$, using $+85 \degree C$ gain parameters

$T = -40 \degree C$, calibrated
Calibration Convergence

Gain Estimate Parameter

Conversion Index

"A" gain

"B" gain
Comparison with Previous Work

• Long decorrelation times not necessary

CONVERSIONS REQUIRED FOR CALIBRATION

\[ 2^{2N} \]


N

THIS WORK

• Long decorrelation times not necessary
Die Photo
## Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25μm 1P4M CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 b</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>1 MS/s</td>
</tr>
<tr>
<td>SNR</td>
<td>89 dB</td>
</tr>
<tr>
<td>INL</td>
<td>+2.1 / -4.8 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>+0.66 / −0.47 LSB</td>
</tr>
<tr>
<td>Power Consumption *</td>
<td>105mW</td>
</tr>
<tr>
<td>Die Area *</td>
<td>1.16mm x 1.38mm</td>
</tr>
</tbody>
</table>

* Excludes digital on FPGA
Outline

• Background
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• "Split ADC" Architecture
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Conclusion

• "Split ADC" architecture
  – Average: Output code
  – Difference: Drive to zero to correct errors
  – Deterministic: Rapid self-calibration
    • Suitable for high resolution ADCs
  – Complexity moved into digital domain

• 16b 1MSps Cyclic ADC
  – Self-calibration in ~ 10,000 conversions
Acknowledgments

• Analog Devices
  – Precision Nyquist Converters group
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  – Larry Singer

• Stanford University
  – Boris Murmann
INL Shapes Vary by Residue Mode

INL shape same as $SDK_A$, $SDK_B$ error coefficients